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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832 Email & Skype: info@chipsmall.com Web: www.chipsmall.com Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# transphorm

# **TPH3202P Series**

# 600V Cascode GaN FET TO-220 Series

# Description

The TPH3202P Series 600V,  $290m\Omega$  gallium nitride (GaN) FETs are normally-off devices. Transphorm GaN FETs offer better efficiency through lower gate charge, faster switching speeds, and smaller reverse recovery charge, delivering significant advantages over traditional silicon (Si) devices.

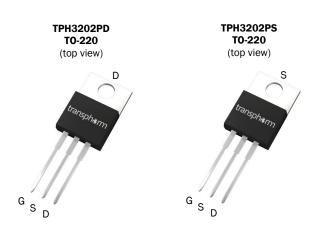
Transphorm is a leading-edge wide band gap supplier with world-class innovation and a portfolio of fully-qualified GaN transistors that enables increased performance and reduced overall system size and cost.

# **Related Literature**

- AN0003: Printed Circuit Board Layout and Probing
- AN0002: Characteristics of GaN Power Switches

# **Product Series and Ordering Information**

Part Number	Package	Package Configuration
TPH3202PD	3 Lead TO-220	Common Drain
TPH3202PS	3 Lead TO-220	Common Source



### **Features**

- Easy to drive—compatible with standard gate drivers
- Low conduction and switching losses
- Low Qrr of 29nC-no free-wheeling diode required
- GSD pin layout improves high speed design
- JEDEC-qualified GaN technology
- RoHS compliant and Halogen-free

### **Benefits**

- · Increased efficiency through fast switching
- Increased power density
- Reduced system size and weight
- Enables more efficient topologies—easy to implement bridgeless totem-pole designs
- Lower BOM cost

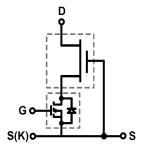
# **Applications**

- Renewable energy
- Industrial
- Automotive
- Telecom and datacom
- Servo motors

# **Key Specifications**

, ,	
V <sub>DS</sub> (V) min	600
V <sub>TDS</sub> (V) max	750
$R_{DS(on)}(m\Omega)$ max*	350
Q <sub>rr</sub> (nC) typ	29
Qg (nC) typ	6.2

\* Dynamic R<sub>(on)</sub>



**Cascode Device Structure** 

# Absolute Maximum Ratings (Tc=25 °C unless otherwise stated)

Symbol	Parameter		Limit Value	Unit
I <sub>D25°C</sub>	Continuous drain current @Tc	=25°C	9	А
ID100°C	Continuous drain current @Tc	=100°C	6	А
I <sub>DM</sub>	Pulsed drain current (pulse w	idth: 100µs)	35	А
V <sub>DSS</sub>	Drain to source voltage		600	V
V <sub>TDS</sub>	Transient drain to source volt	age <sup>a</sup>	750	V
V <sub>GSS</sub>	Gate to source voltage		±18	V
P <sub>D25</sub> ∘c	Maximum power dissipation	Maximum power dissipation		W
Tc	Operating temperature	Case		°C
Tر		Junction	-55 to +175	°C
Ts	Storage temperature	Storage temperature		°C
T <sub>CSOLD</sub>	Soldering peak temperature		260	°C

## **Thermal Resistance**

Symbol	Parameter	Typical	Unit
R <sub>0JC</sub>	Junction-to-case	2.3	°C/W
R <sub>ØJA</sub>	Junction-to-ambient	62	°C/W

Notes:

a. In off-state, spike duty cycle D<0.1, spike duration <1 $\mu$ s b. For 10 sec., 1.6mm from the case

# Electrical Parameters (Tc=25 °C unless otherwise stated)

Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions	
Forward	Device Characteristics		1	1			
V <sub>DSS-MAX</sub>	Maximum drain-source voltage	600	_	_	V	V <sub>GS</sub> =0V	
$V_{\text{GS}(\text{th})}$	Gate threshold voltage	1.6	2	2.5	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250µA	
<b>D</b>	Drain-source on-resistance (T_=25°C) a	_	290	350		V <sub>GS</sub> =8V, I <sub>D</sub> =5.5A, T <sub>J</sub> =25°C	
$R_{DS(on)}$	Drain-source on-resistance (T_=175°C) a	_	670	_	mΩ	V <sub>GS</sub> =8V, I <sub>D</sub> =5.5A, T <sub>J</sub> =175°C	
I <sub>DSS</sub>	Drain-to-source leakage current (Tj=25°C)	_	2.5	30	μA	V <sub>DS</sub> =600V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	
	Drain-to-source leakage current (Tj=150°C)	-	8	-		V <sub>DS</sub> =600V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C	
	Gate-to-source forward leakage current	_	-	100	nA	V <sub>GS</sub> =18V	
I <sub>GSS</sub>	Gate-to-source reverse leakage current	_	-	-100	IIA	V <sub>GS</sub> =-18V	
CISS	Input capacitance	_	760	_			
Coss	Output capacitance	_	26	_	pF	V <sub>GS</sub> =0V, V <sub>DS</sub> =480V, <i>f</i> =1MHz	
C <sub>RSS</sub>	Reverse transfer capacitance	_	3.5	-			
$C_{O(er)}$	Output capacitance, energy related <sup>b</sup>	_	36	-	pF	$V_{GS}=0V$ , $V_{DS}=0V$ to 480V	
C <sub>O(tr)</sub>	Output capacitance, time related <sup>c</sup>	_	57	-	р	$v_{\rm GS} = 0 v, v_{\rm DS} = 0 v (0.480 v)$	
Qg	Total gate charge d	_	6.2	9.3			
$Q_{gs}$	Gate-source charge	—	2.1	-	nC	$V_{DS}$ =100V a, $V_{GS}$ =0V to 4.5V, I <sub>D</sub> =5.5A	
$\mathbf{Q}_{gd}$	Gate-drain charge	—	2.2	_			
t <sub>d(on)</sub>	Turn-on delay	_	6.2	-			
tr	Rise time	_	4.5	-	nc	$V_{DS}$ =400V, $V_{GS}$ =0V to 10V,	
$T_{d(off)}$	Turn-off delay	_	9.7	-	ns	I <sub>D</sub> =5.5A, R <sub>G</sub> =2Ω	
t <sub>f</sub>	Fall time	_	5	_			
Reverse	Device Characteristics						
ls	Reverse current	_	_	6	A	$V_{GS}$ =0V, T <sub>C</sub> =100°C $\leq$ 50% Duty Cycle	
V <sub>SD</sub> R		_	2.9	_		V <sub>GS</sub> =0V, I <sub>S</sub> =6A, T <sub>J</sub> =25°C	
	Reverse voltage <sup>a</sup>	_	4.8	-	V	V <sub>GS</sub> =0V, I <sub>S</sub> =6A, T <sub>J</sub> =175°C	
		_	2.2	_		V <sub>GS</sub> =0V, I <sub>S</sub> =3A, T <sub>J</sub> =25°C	
t <sub>rr</sub>	Reverse recovery time	_	11.5	-	ns	I <sub>S</sub> =5.5A, V <sub>DD</sub> =480V,	
Q <sub>rr</sub>	Reverse recovery charge	_	29	_	nC	di/dt=1500A/µs, Tj=25°C	

Notes:

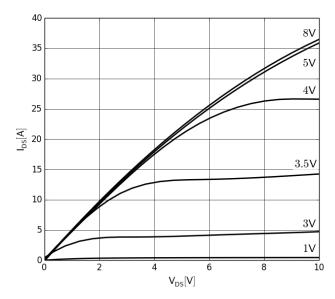
a. Dynamic value

Equivalent capacitance to give same stored energy from OV to 480V b.

Equivalent capacitance to give same charging time from OV to 480V  $Q_g$  does not change for  $V_{\text{DS}}{>}100\text{V}$ c.

d.







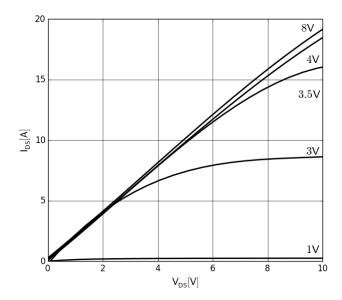
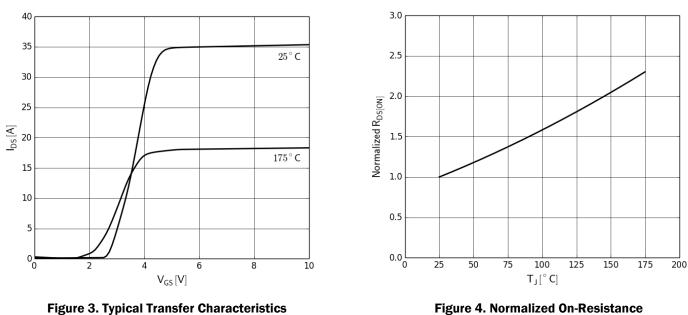


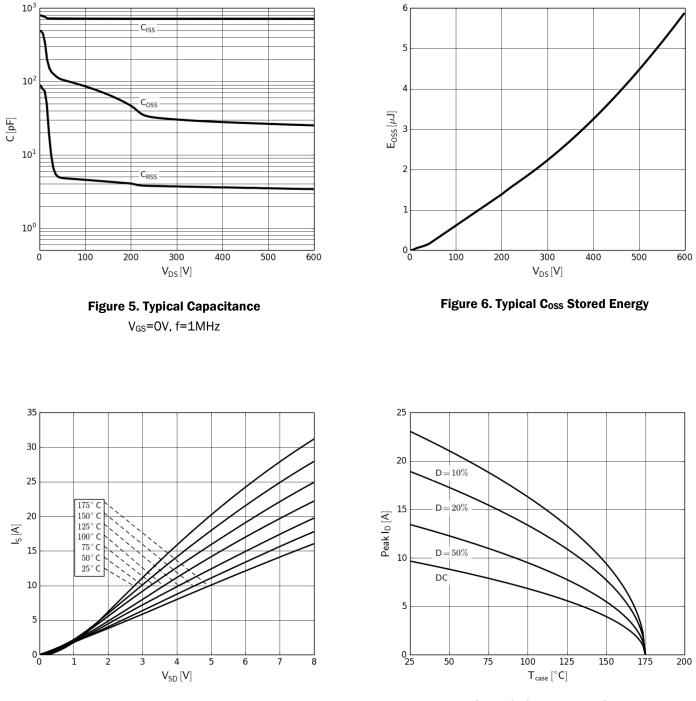
Figure 2. Typical Output Characteristics TJ=175°C Parameter: V<sub>GS</sub>



 $V_{DS}$ =10V, parameter: T<sub>J</sub>







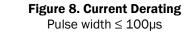


Figure 7. Forward Characteristics of Rev. Diode

 $I_{S}=f(V_{SD})$ , parameter:  $T_{J}$ 



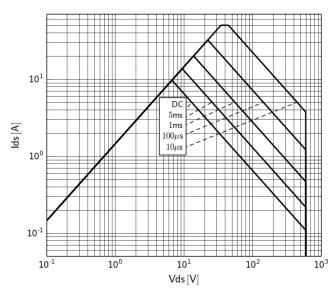


Figure 9. Safe Operating Area Tc=25°C (calculated based on thermal limit)

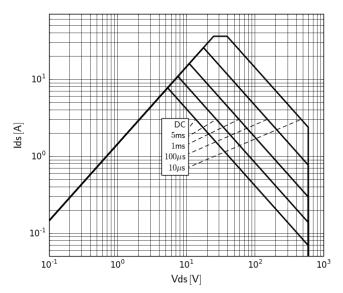


Figure 10. Safe Operating Area Tc=80°C (calculated based on thermal limit)

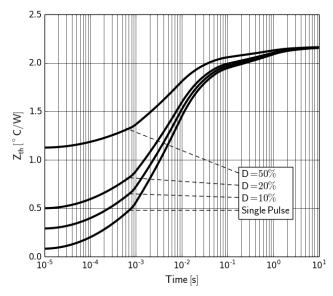


Figure 11. Transient Thermal Resistance

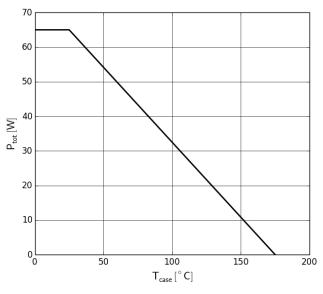


Figure 12. Power Dissipation

# **Test Circuits and Waveforms**

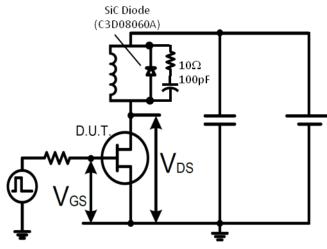


Figure 13. Switching Time Test Circuit

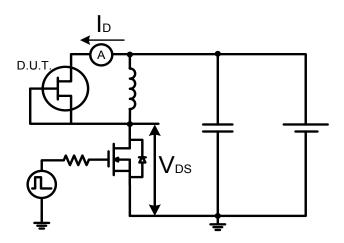


Figure 15. Test Circuit for Diode Characteristics

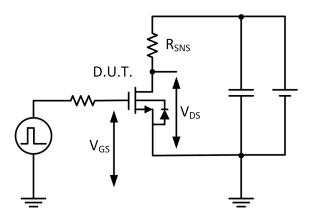


Figure 17. Test Circuit for Dynamic R<sub>DS(on)</sub>

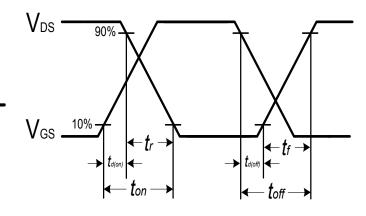
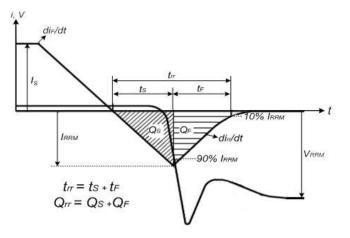
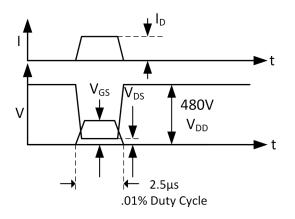


Figure 14. Switching Time Waveform





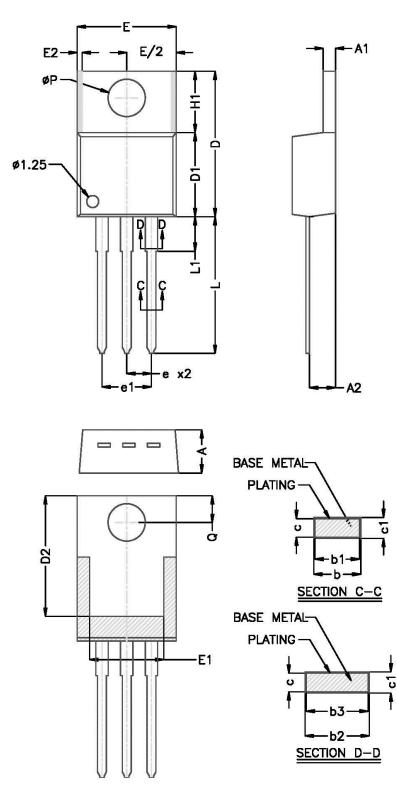




# Mechanical

# 3 Lead TO-220 (PD) Package

Pin 1: Gate; Pin 2: Source; Pin 3: Drain, Tab: Drain



	N	ILLIMETER	S	INCHES		
SYMBOL	MINIMUM	NOMINAL	MAXIMUM	MINIMUM	NOMINAL	MAXIMUM
A	3.56	4.45	4.83	0.140	0.175	0.190
A1	0.51	1.27	1.40	0.020	0.050	0.055
A2	2.03	-	2.92	0.080		0.115
b	0.38		1.01	0.015	Ţ	0.040
b1	0.38	-	0.97	0.015	-	0.038
b2	1.14		1.78	0.045	-	0.070
b3	1.14	1.27	1.73	0.045	0.050	0.068
C	0.36	-	0.61	0.014	Ţ	0.024
c1	0.36	0.38	0.56	0.014	0.015	0.022
D	14.22	-	16.51	0.560	-	0.650
D1	8.38	8.64	9.02	0.330	0.340	0.355
D2	11.68	-	12.88	0.460	1	0.507
E	9.65	10.19	10.67	0.380	0.401	0.420
E1	6.86	-	8.89	0.270	1	0.350
E2	-	_	0.76	-	-	0.030
0		2.54 BSC		(	0.100 BS(	3
e1		5.08 BSC	1	(	0.200 BS	3
H1	5.84	6.30	6.66	0.230	0.248	0.270
L	12.70	14.05	14.73	0.500	0.553	0.580
L1	-	7 <u>—</u> 1	6.35	-		0.250
øP	3.54	3.84	4.08	0.139	0.151	0.161
0	2.54	-	3.42	0.100	-	0.135

### NOTES:

1. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 MM (0.005") PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.

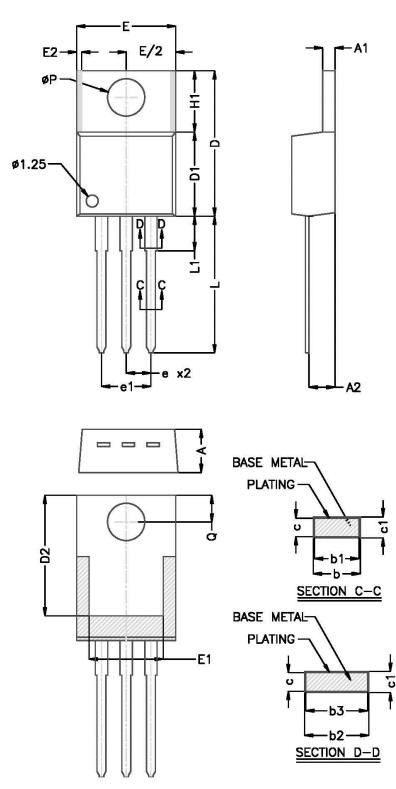
2. DIMENSIONS E2 & H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.

3. OUTLINE CONFORMS TO JEDEC TO-220AB.

# Mechanical

# 3 Lead TO-220 (PS) Package

Pin 1: Gate; Pin 2: Source; Pin 3: Drain, Tab: Source



-	N	ILLIMETER	S	INCHES		
SYMBOL	MINIMUM	NOMINAL	MAXIMUM	MINIMUM	NOMINAL	MAXIMUM
A	3.56	4.45	4.83	0.140	0.175	0.190
A1	0.51	1.27	1.40	0.020	0.050	0.055
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Ь	0.38	-	1.01	0.015	-	0.040
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b2	1.14	-	1.78	0.045	-	0.070
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C	0.36	-	0.61	0.014	-	0.024
c1	0.36	0.38	0.56	0.014	0.015	0.022
D	14.22	-	18.51	0.560	-	0.650
D1	8.38	8.64	9.02	0.330	0.340	0.355
D2	11.68	-	12.88	0.460	-	0.507
E	9.65	10.19	10.67	0.380	0.401	0.420
E1	6.86	-	8.89	0.270	-	0.350
E2	-	-	0.76	<u> </u>	-	0.030
		2.54 BSC		(	0.100 BS	5
e1		5.08 BSC	1	(	0.200 BS	3
H1	5.84	6.30	6.86	0.230	0.248	0.270
Ľs	12.70	14.05	14.73	0.500	0.553	0.580
L1	-		6.35	-	-	0.250
øP	3.54	3.84	4.08	0.139	0.151	0.161
0	2.54		3.42	0.100	-	0.135

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2. DIMENSIONS E2 & H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.

3. OUTLINE CONFORMS TO JEDEC TO-220AB.

# **Design Considerations**

The fast switching of GaN devices reduces current-voltage cross-over losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note <u>Printed Circuit Board Layout and Probing for GaN Power</u> <u>Switches</u>. The table below provides some practical rules that should be followed during the evaluation.

# When Evaluating Transphorm GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See AN0003: Printed Circuit Board Layout and Probing	

## **Application Notes**

- AN0002: Characteristics of Transphorm GaN Power Switches
- AN0003: Printed Circuit Board Layout and Probing
- <u>AN0004</u>: Designing Hard-switched Bridges with GaN
- AN0008: Drain Voltage and Avalanche Ratings for GaN FETs

# **Evaluation Boards**

• TDPS250E2D2-KIT: 250W all-in-one power supply evaluation platform

# **Revision History**

Version	Date	Change(s)
0	11/14/2016	Release P series datasheet
1	12/12/2016	Formatting Changes to p. 3, revision of dynamic measurement verbiage