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transphorm

# TPH3207WS

## 650V Cascode GaN FET in TO-247 (source tab)

### Description

The TPH3207WS 650V, 35mΩ gallium nitride (GaN) FET is a normally-off device. Transphorm GaN FETs offer better efficiency through lower gate charge, faster switching speeds, and smaller reverse recovery charge, delivering significant advantages over traditional silicon (Si) devices.

Transphorm is a leading-edge wide band gap supplier with world-class innovation and a portfolio of fully-qualified GaN transistors that enables increased performance and reduced overall system size and cost.

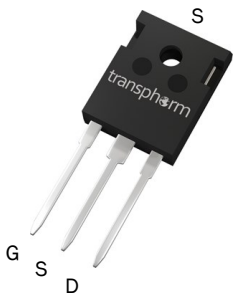
### Related Literature

- AN0009: Recommended External Circuitry for GaN FETs
- AN0003: Printed Circuit Board Layout and Probing

### Ordering Information

| Part Number | Package | Package Configuration |
|---|---|---|
| TPH3207WS | 3 Lead TO-247 | Common Source |

**TPH3207WS**
**TO-247**
(top view)




### Features

- Easy to drive—compatible with standard gate drivers
- Low conduction and switching losses
- Low Qrr of 175nC—no free-wheeling diode required
- GSD pin layout improves high speed design
- JEDEC-qualified GaN technology
- RoHS compliant and Halogen-free

### Benefits

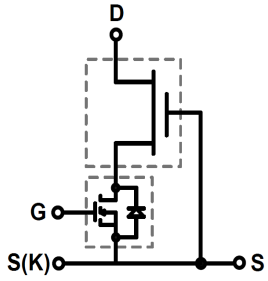
- Increased efficiency through fast switching
- Increased power density
- Reduced system size and weight
- Enables more efficient topologies—easy to implement bridgeless totem-pole designs
- Lower BOM cost

### Applications

- Renewable energy
- Industrial
- Automotive
- Telecom and datacom
- Servo motors

| Key Specifications | |
|---|---|
| $V_{DS}$ (V) min | 650 |
| $V_{TDS}$ (V) max | 800 |
| $R_{DS(on)}$ (mΩ) max* | 41 |
| $Q_{rr}$ (nC) typ | 175 |
| Qg (nC) typ | 28 |

* Dynamic $R_{(on)}$




**Cascode Device Structure**

## Absolute Maximum Ratings ($T_C$=25°C unless otherwise stated)

| Symbol | Parameter | Limit Value | Unit |
|---|---|---|---|
| $I_{D25°C}$ | Continuous drain current @$T_C$=25°C [a] | 50 | A |
| $I_{D100°C}$ | Continuous drain current @$T_C$=100°C [a] | 31.5 | A |
| $I_{DM}$ | Pulsed drain current (pulse width: 10µs) | 240 | A |
| $V_{DSS}$ | Drain to source voltage | 650 | V |
| $V_{TDS}$ | Transient drain to source voltage [b] | 800 | V |
| $V_{GSS}$ | Gate to source voltage | ±18 | V |
| $P_{D25°C}$ | Maximum power dissipation | 178 | W |
| $T_J$ | Operating junction temperature | -55 to +150 | °C |
| $T_S$ | Storage temperature | -55 to +150 | °C |
| $T_{CSOLD}$ | Soldering peak temperature [c] | 260 | °C |

## Thermal Resistance

| Symbol | Parameter | Typical | Unit |
|---|---|---|---|
| $R_{\Theta JC}$ | Junction-to-case | 0.7 | °C/W |
| $R_{\Theta JA}$ | Junction-to-ambient | 40 | °C/W |

Notes:
a. For high current operation, see application note AN0009
b. In off-state, spike duty cycle D<0.01, spike duration <1µs
c. For 10 sec., 1.6mm from the case

**Electrical Parameters** ($T_C$=25°C unless otherwise stated)

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| **Forward Device Characteristics** | | | | | | |
| $V_{DSS-MAX}$ | Maximum drain-source voltage | 650 | — | — | V | $V_{GS}$=0V |
| $V_{GS(th)}$ | Gate threshold voltage | 1.65 | 2.1 | 2.65 | V | $V_{DS}$=$V_{GS}$, $I_D$=0.7mA |
| $R_{DS(on)}$ | Drain-source on-resistance ($T_J$=25°C) [a] | — | 35 | 41 | mΩ | $V_{GS}$=8V, $I_D$=32A, $T_J$=25°C |
| | Drain-source on-resistance ($T_J$=150°C) [a] | — | 72 | — | | $V_{GS}$=8V, $I_D$=32A, $T_J$=150°C |
| $I_{DSS}$ | Drain-to-source leakage current ($T_J$=25°C) | — | 5 | 50 | μA | $V_{DS}$=650V, $V_{GS}$=0V, $T_J$=25°C |
| | Drain-to-source leakage current ($T_J$=150°C) | — | 15 | — | | $V_{DS}$=650V, $V_{GS}$=0V, $T_J$=150°C |
| $I_{GSS}$ | Gate-to-source forward leakage current | — | — | 100 | nA | $V_{GS}$=18V |
| | Gate-to-source reverse leakage current | — | — | -100 | | $V_{GS}$=-18V |
| $C_{ISS}$ | Input capacitance | — | 2200 | — | pF | $V_{GS}$=0V, $V_{DS}$=400V, *f*=1MHz |
| $C_{OSS}$ | Output capacitance | — | 202 | — | | |
| $C_{RSS}$ | Reverse transfer capacitance | — | 27 | — | | |
| $C_{O(er)}$ | Output capacitance, energy related [b] | — | 280 | — | pF | $V_{GS}$=0V, $V_{DS}$=0V to 400V |
| $C_{O(tr)}$ | Output capacitance, time related [c] | — | 404 | — | | |
| $Q_g$ | Total gate charge | — | 28 | 42 | nC | $V_{DS}$=400V, $V_{GS}$=0V to 8V, $I_D$=32A |
| $Q_{gs}$ | Gate-source charge | — | 10 | — | | |
| $Q_{gd}$ | Gate-drain charge | — | 6 | — | | |
| $t_{d(on)}$ | Turn-on delay | — | 56 | — | ns | $V_{DS}$=400V, $V_{GS}$=0V to 10V, $I_D$=32A, 0.5A gate drive, test circuit as in Figure 13 |
| $t_r$ | Rise time | — | 12 | — | | |
| $T_{d(off)}$ | Turn-off delay | — | 79 | — | | |
| $t_f$ | Fall time | — | 9 | — | | |
| **Reverse Device Characteristics** | | | | | | |
| $I_S$ | Reverse current | — | — | 31.5 | A | $V_{GS}$=0V, $T_C$=100°C ≤50% Duty Cycle |
| $V_{SD}$ | Reverse voltage [a] | — | 1.9 | — | V | $V_{GS}$=0V, $I_S$=32A, $T_J$=25°C |
| | | — | 1.4 | — | | $V_{GS}$=0V, $I_S$=16A, $T_J$=25°C |
| $t_{rr}$ | Reverse recovery time | — | 42 | — | ns | $I_S$=32A, $V_{DD}$=400V, di/dt=1000A/μs, $T_J$=25°C |
| $Q_{rr}$ | Reverse recovery charge | — | 175 | — | nC | |

Notes:
a. Dynamic value
b. Equivalent capacitance to give same stored energy from 0V to 400V
c. Equivalent capacitance to give same charging time from 0V to 400V

**Typical Characteristics** (25 °C unless otherwise stated)

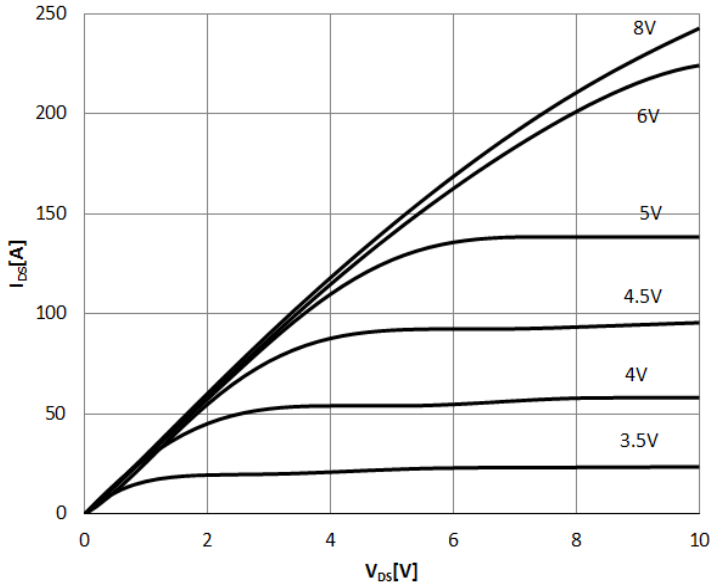



**Figure 1. Typical Output Characteristics $T_J$=25 °C**
Parameter: $V_{GS}$

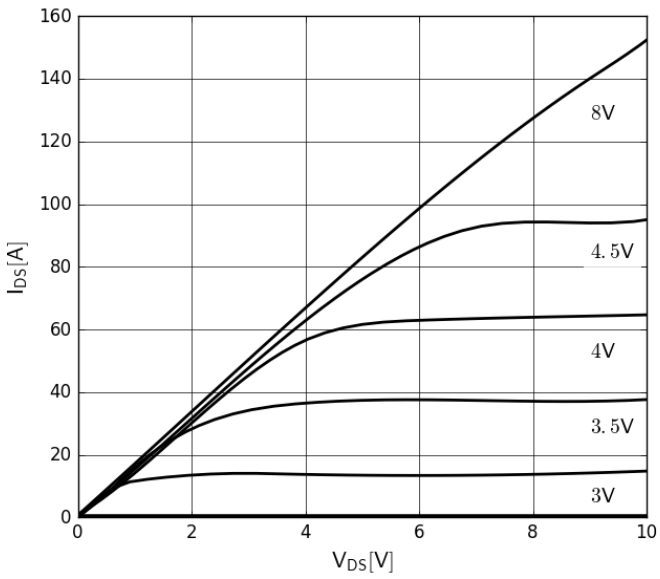



**Figure 2. Typical Output Characteristics $T_J$=150 °C**
Parameter: $V_{GS}$

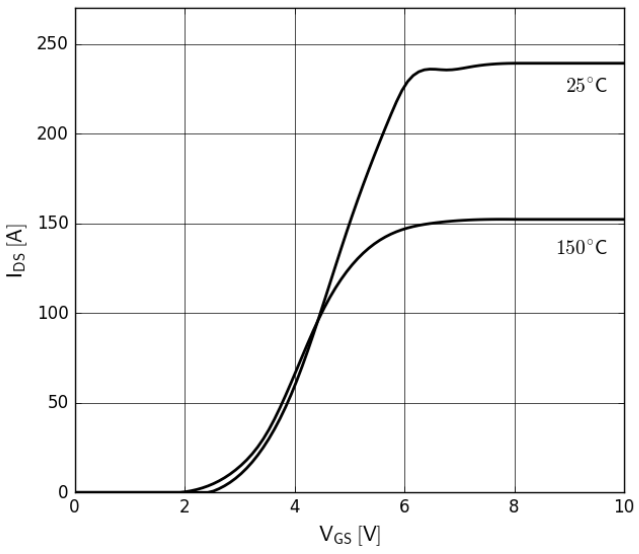



**Figure 3. Typical Transfer Characteristics**
$V_{DS}$=10V, parameter: $T_J$

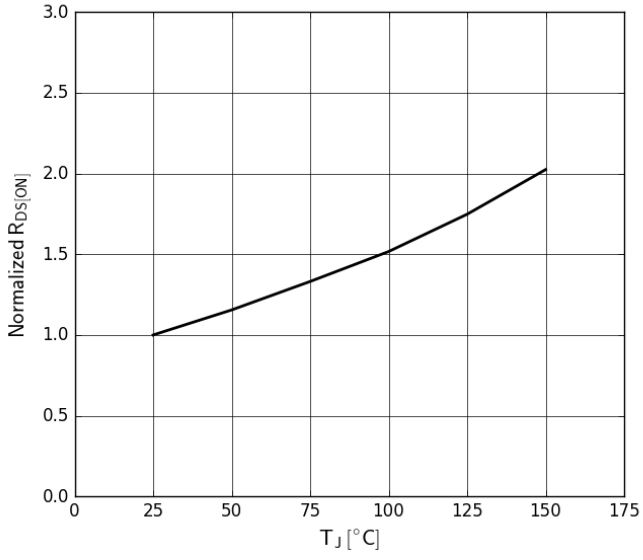



**Figure 4. Normalized On-Resistance**
$I_D$=32A, $V_{GS}$=8V

**Typical Characteristics** (25 °C unless otherwise stated)

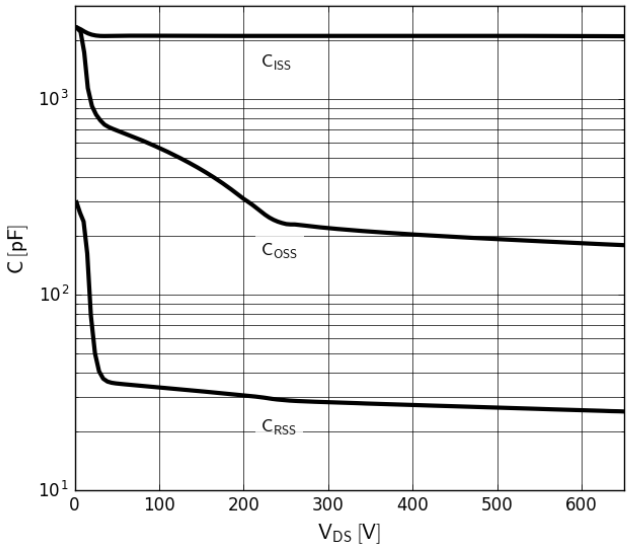



**Figure 5. Typical Capacitance**
$V_{GS}$=0V, f=1MHz

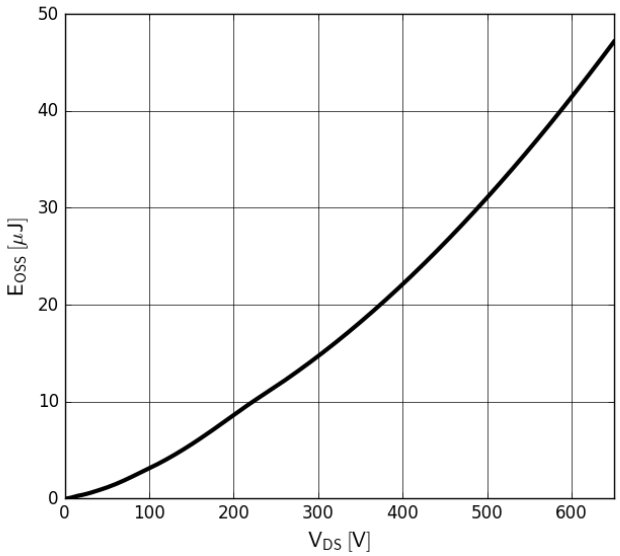



**Figure 6. Typical $C_{oss}$ Stored Energy**

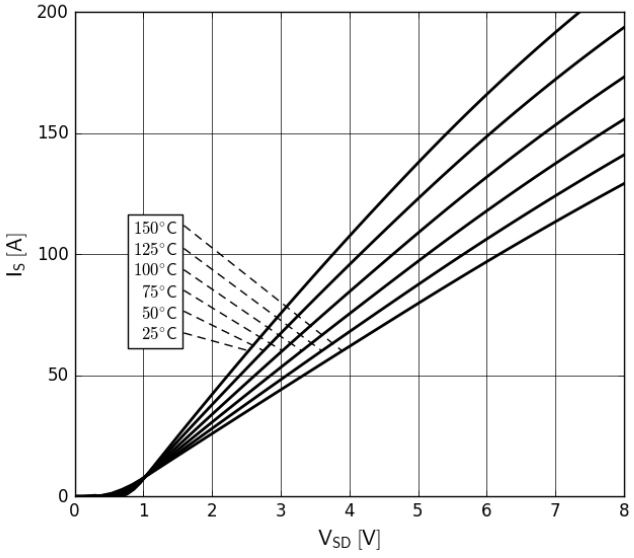



**Figure 7. Forward Characteristics of Rev. Diode**
$I_S=f(V_{SD})$; parameter: $T_J$; pulse width = 20µs

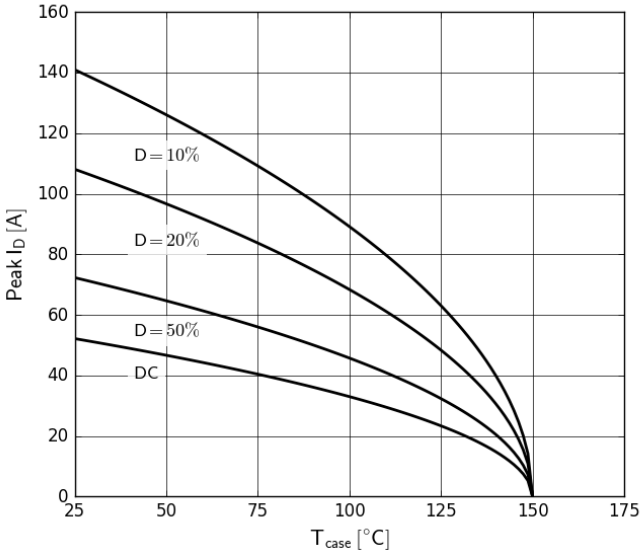



**Figure 8. Current Derating**
Pulse width ≤ 10µs

**Typical Characteristics** (25 °C unless otherwise stated)

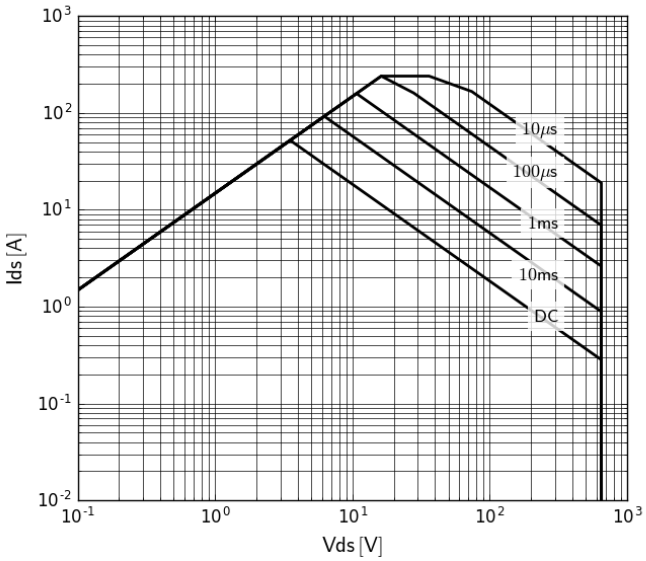



**Figure 9. Safe Operating Area $T_C$=25 °C (calculated based based on thermal limit)**

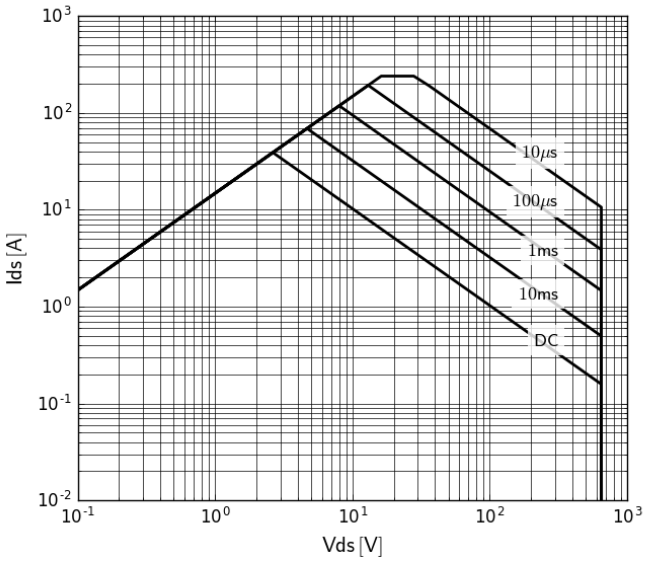



**Figure 10. Safe Operating Area $T_C$=80 °C (calculated based on thermal limit)**

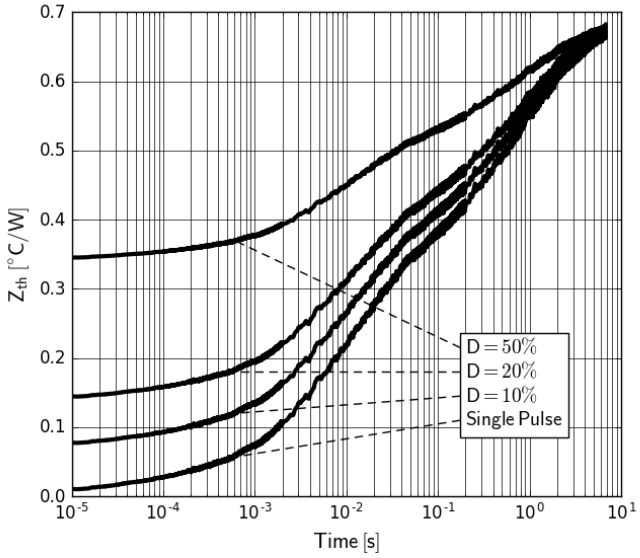



**Figure 11. Transient Thermal Resistance**

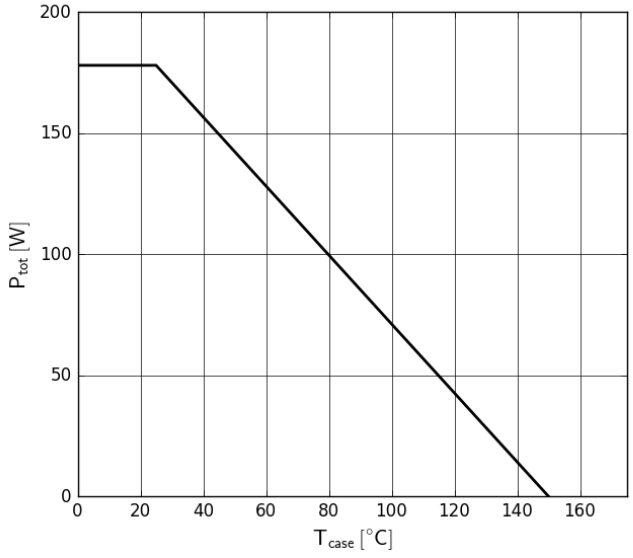



**Figure 12. Power Dissipation**

## Test Circuits and Waveforms

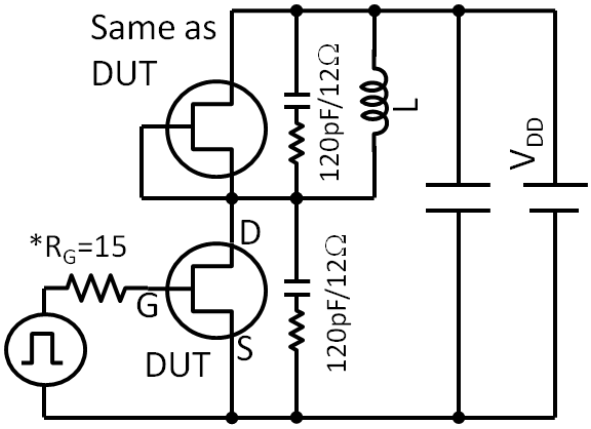



**Figure 13. Switching Time Test Circuit**
***driver internal series resistance**
**(no external gate resistor)**
**(See app note AN0009 for methods to ensure clean switching)**

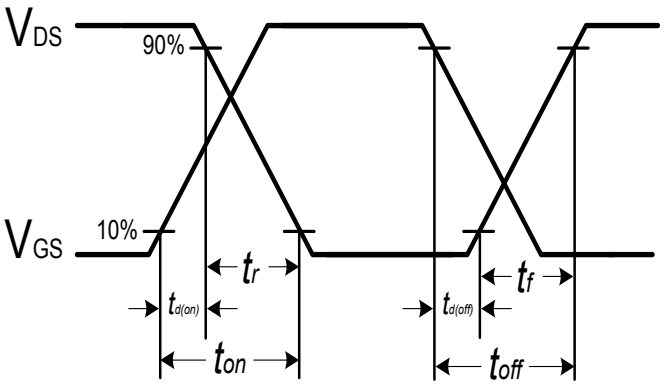



**Figure 14. Switching Time Waveform**

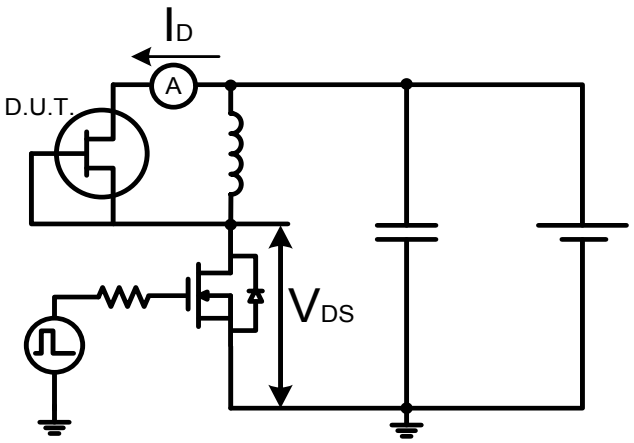



**Figure 15. Test Circuit for Diode Characteristics**

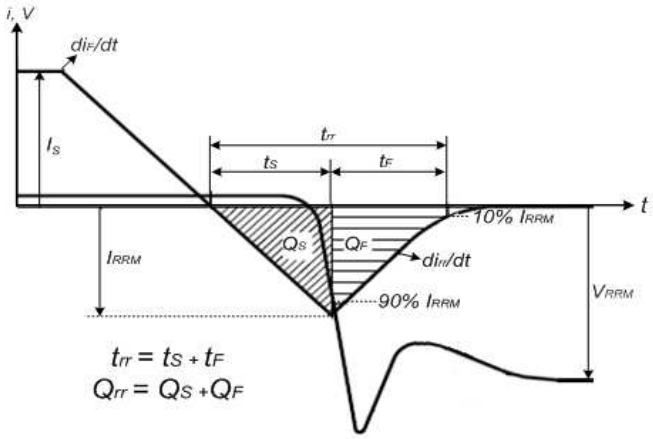



**Figure 16. Diode Recovery Waveform**

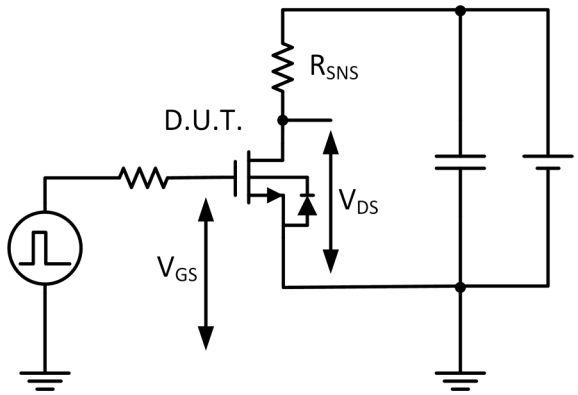



**Figure 17. Test Circuit for Dynamic $R_{DS(on)}$**

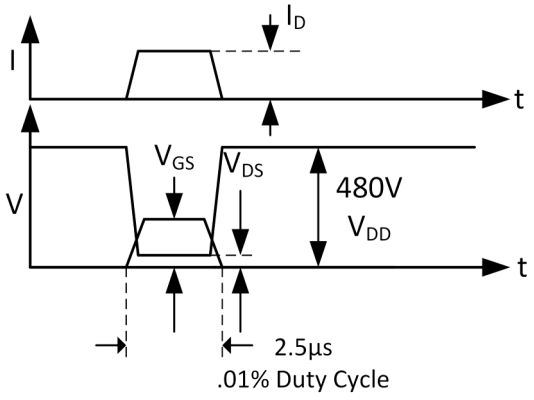
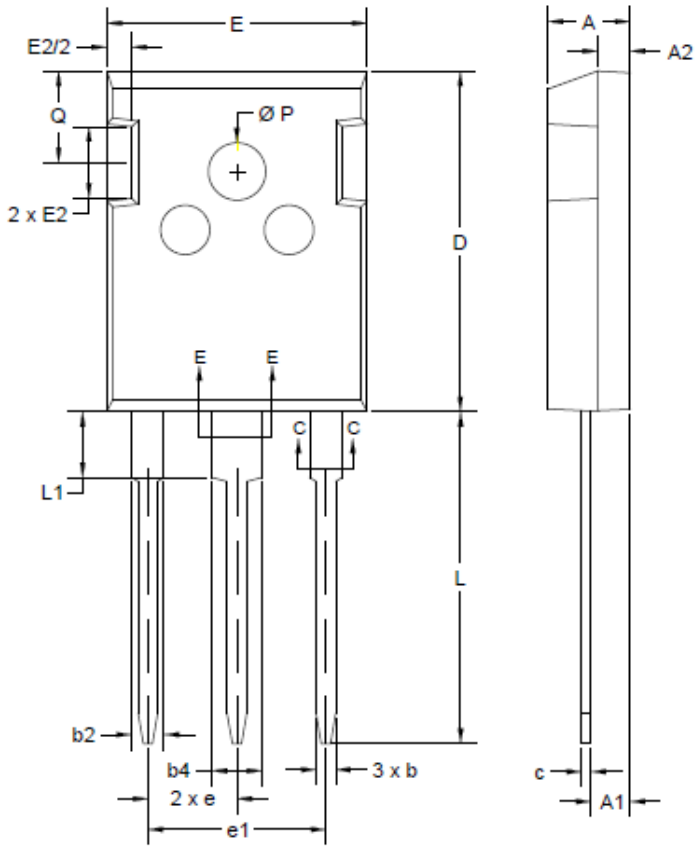


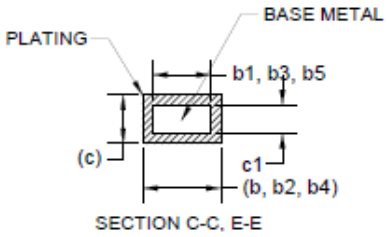

**Figure 18. Dynamic $R_{DS(on)}$ Waveform**

## Mechanical

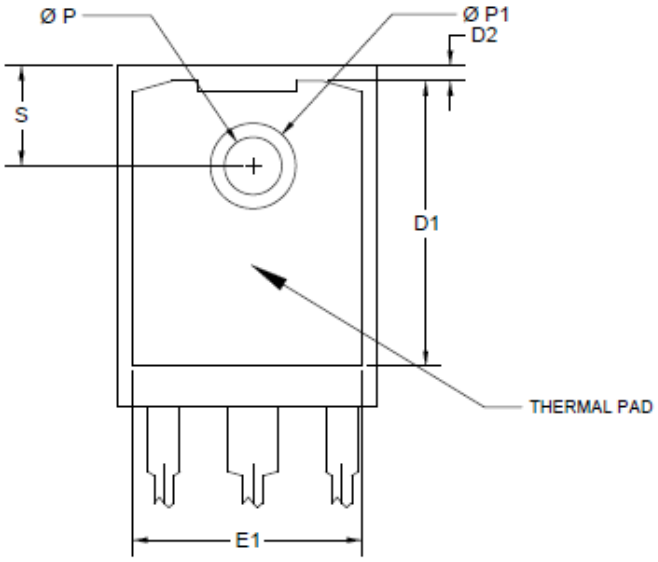
## 3 Lead TO-247 Package




| SYMBOL | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | MINIMUM | NOMINAL | MAXIMUM | MINIMUM | NOMINAL | MAXIMUM |
| A | 4.69 | 5.00 | 5.31 | 0.185 | 0.197 | 0.209 |
| A1 | 2.20 | 2.39 | 2.59 | 0.087 | 0.094 | 0.102 |
| A2 | 1.49 | 2.01 | 2.49 | 0.059 | 0.079 | 0.098 |
| b | 0.99 | - | 1.40 | 0.039 | - | 0.055 |
| b1 | 0.99 | - | 1.35 | 0.039 | - | 0.053 |
| b2 | 1.77 | - | 2.19 | 0.070 | - | 0.086 |
| b3 | 1.77 | - | 2.14 | 0.070 | - | 0.084 |
| b4 | 2.76 | - | 3.33 | 0.109 | - | 0.131 |
| b5 | 2.76 | - | 3.28 | 0.109 | - | 0.129 |
| c | 0.38 | - | 0.89 | 0.015 | - | 0.035 |
| c1 | 0.38 | - | 0.84 | 0.015 | - | 0.033 |
| D | 20.52 | 20.85 | 21.18 | 0.808 | 0.821 | 0.834 |
| D1 | 16.51 | - | - | 0.650 | - | - |
| D2 | 0.50 | - | 1.42 | 0.020 | - | 0.056 |
| E | 15.49 | 15.88 | 16.26 | 0.610 | 0.625 | 0.640 |
| E1 | 13.46 | - | - | 0.530 | - | - |
| E2 | 2.03 | - | 3.56 | 0.080 | - | 0.140 |
| e | 5.46 BSC | | | 0.215 BSC | | |
| e1 | 10.87 BSC | | | 0.428 BSC | | |
| L | 20.01 | 20.27 | 20.52 | 0.788 | 0.798 | 0.808 |
| L1 | - | 4.27 | 4.50 | - | 0.168 | 0.177 |
| ØP | 3.45 | 3.51 | 3.56 | 0.136 | 0.138 | 0.140 |
| ØP1 | - | - | 7.39 | - | - | 0.291 |
| Q | 5.20 | 5.59 | 5.97 | 0.205 | 0.220 | 0.235 |
| S | 6.15 BSC | | | 0.242 BSC | | |




SECTION C-C, E-E




NOTES:

1. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 MM (0.005") PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
2. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS D1 & E1.
3. LEAD FINISH UNCONTROLLED IN L1.
4. OUTLINE CONFORMS TO JEDEC TO-247AD.

| TO-247 3L | | | |
|---|---|---|---|
| transphorm | | | |
| SCALE: 1:1 | SHEET 1/1 | DRAWING NO. 200019 | VER. 2 |

## Design Considerations

The fast switching of GaN devices reduces current-voltage cross-over losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note Printed Circuit Board Layout and Probing for GaN Power Switches. The table below provides some practical rules that should be followed during the evaluation.

### When Evaluating Transphorm GaN Devices:

| DO | DO NOT |
|---|---|
| Minimize circuit inductance by keeping traces short, both in the drive and power loop | Twist the pins of TO-220 or TO-247 to accommodate GDS board layout |
| Minimize lead length of TO-220 and TO-247 package when mounting to the PCB | Use long traces in drive circuit, long lead length of the devices |
| Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points | Use differential mode probe or probe ground clip with long wire |
| See AN0003: Printed Circuit Board Layout and Probing | |

## Application Notes

- AN0002: Characteristics of Transphorm GaN Power Switches
- AN0003: Printed Circuit Board Layout and Probing
- AN0004: Designing Hard-switched Bridges with GaN
- AN0008: Drain Voltage and Avalanche Ratings for GaN FETs
- AN0009: Recommended External Circuitry for GaN FETs

## Evaluation Boards

- TDTTP4000W066-KIT: 4kW totem-pole PFC evaluation platform
- TDINV4500W050-KIT: 4.5kW inverter evaluation platform

## Revision History

| Version | Date | Change(s) |
|---|---|---|
| 9 | 11/14/2016 | Added application note AN0009 |
| 10 | 12/12/2016 | Formatting Changes to p. 3, revision of dynamic measurement verbiage |
| | | |
| | | |
| | | |