Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

650V Cascode GaN FET PQFN88 Series

Description

The TPH3208L Series 650V, 110mΩ gallium nitride (GaN) FETs are normally-off devices. Transphorm GaN FETs offer better efficiency through lower gate charge, faster switching speeds, and smaller reverse recovery charge, delivering significant advantages over traditional silicon (Si) devices.

Transphorm is a leading-edge wide band gap supplier with world-class innovation and a portfolio of fully-qualified GaN transistors that enables increased performance and reduced overall system size and cost.

Related Literature

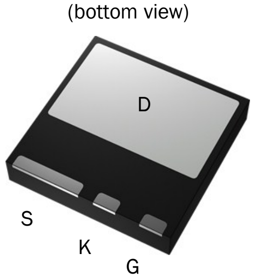
- AN0009: Recommended External Circuitry for GaN FETs
- AN0003: Printed Circuit Board Layout and Probing

Product Series and Ordering Information

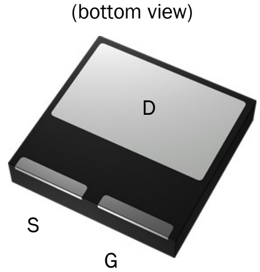
Part Number*	Package	Package Configuration
TPH3208LD	8 x 8mm PQFN	Common Drain
TPH3208LDG**	8 x 8mm PQFN	Common Drain
TPH3208LS	8 x 8mm PQFN	Common Source

* Add "-TR" suffix for tape and reel
** LDG package offers larger gate pad

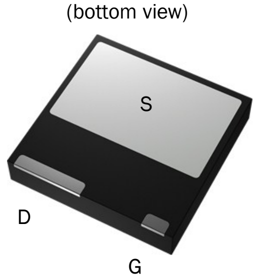
TPH3208LD
8x8 PQFN
(bottom view)



TPH3208LDG
8x8 PQFN
(bottom view)



TPH3208LS
8x8 PQFN
(bottom view)



Features

- Easy to drive—compatible with standard gate drivers
- Low conduction and switching losses
- Low Qrr of 54nC—no free-wheeling diode required
- JEDEC-qualified GaN technology
- RoHS compliant and Halogen-free

Benefits

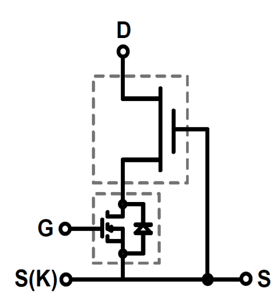
- Increased efficiency through fast switching
- Increased power density
- Reduced system size and weight
- Enables more efficient topologies—easy to implement bridgeless totem-pole designs
- Lower BOM cost

Applications

- Renewable energy
- Industrial
- Automotive
- Telecom and datacom
- Servo motors

Key Specifications	
V_{DS} (V) min	650
V_{TDS} (V) max	800
$R_{DS(on)}$ (mΩ) max*	130
Q_{rr} (nC) typ	54
Qg (nC) typ	10

* Includes dynamic $R_{(on)}$



Cascode Device Structure

Absolute Maximum Ratings (T_C=25°C unless otherwise stated)

Symbol	Parameter		Limit Value	Unit
$I_{D25^\circ C}$	Continuous drain current @T_C=25°C [a]		20	A
$I_{D100^\circ C}$	Continuous drain current @T_C=100°C [a]		13	A
I_{DM}	Pulsed drain current (pulse width: 10µs)		80	A
V_{DSS}	Drain to source voltage		650	V
V_{TDS}	Transient drain to source voltage [b]		800	V
V_{GSS}	Gate to source voltage		±18	V
$P_{D25^\circ C}$	Maximum power dissipation		96	W
T_C	Operating temperature	Case	-55 to +150	°C
T_J		Junction	-55 to +150	°C
T_S	Storage temperature		-55 to +150	°C
T_{CSOLD}	Soldering peak temperature [c]		260	°C

Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\Theta JC}$	Junction-to-case	1.3	°C/W
$R_{\Theta JA}$	Junction-to-ambient [d]	45	°C/W

Notes:

a. For high current operation, see application note AN0009
b. In off-state, spike duty cycle D<0.01, spike duration <1µs
c. For 10 sec., 1.6mm from the case
d. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm^2 copper area and 70µm thickness)

Electrical Characteristics (T_C=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Static						
$V_{DSS-MAX}$	Maximum drain-source voltage	650	—	—	V	V_{GS}=0V
$V_{GS(th)}$	Gate threshold voltage	1.6	2.1	2.6	V	V_{DS}=V_{GS}, I_D=0.3mA
$R_{DS(on)}$	Drain-source on-resistance (T_J=25°C)	—	110	130	mΩ	V_{GS}=8V, I_D=14A, T_J=25°C
	Drain-source on-resistance (T_J=150°C)	—	226	—		V_{GS}=8V, I_D=14A, T_J=150°C
I_{DSS}	Drain-to-source leakage current (T_J=25°C)	—	3	30	μA	V_{DS}=650V, V_{GS}=0V, T_J=25°C
	Drain-to-source leakage current (T_J=150°C)	—	7	—		V_{DS}=650V, V_{GS}=0V, T_J=150°C
I_{GSS}	Drain-to-source forward leakage current	—	—	100	nA	V_{GS}=18V
	Drain-to-source reverse leakage current	—	—	-100		V_{GS}=-18V
Dynamic						
C_{ISS}	Input capacitance	—	760	—	pF	V_{GS}=0V, V_{DS}=400V, *f*=1MHz
C_{OSS}	Output capacitance	—	58	—		
C_{RSS}	Reverse transfer capacitance	—	6	—		
$C_{O(er)}$	Output capacitance, energy related [a]	—	82	—	pF	V_{GS}=0V, V_{DS}=0V to 400V
$C_{O(tr)}$	Output capacitance, time related [b]	—	132	—		
Q_g	Total gate charge	—	10	42	nC	V_{DS}=400V, V_{GS}=0V to 8V, I_D=13A
Q_{gs}	Gate-source charge	—	3.1	—		
Q_{gd}	Gate-drain charge	—	3.4	—		
$t_{d(on)}$	Turn-on delay	—	17	—	ns	V_{DS}=400V, V_{GS}=0V to 10V, I_D=13A, FB=120Ω
t_r	Rise time	—	7	—		
$T_{d(off)}$	Turn-off delay	—	23	—		
t_f	Fall time	—	8	—		
Reverse Operation						
I_S	Reverse current	—	—	13	A	V_{GS}=0V, T_C=100°C
V_{SD}	Reverse voltage	—	1.93	—	V	V_{GS}=0V, I_S=14A, T_J=25°C
		—	1.33	—		V_{GS}=0V, I_S=7A, T_J=25°C
t_{rr}	Reverse recovery time	—	22	—	ns	I_S=0A to 13A, V_{DD}=400V, di/dt=1000A/μs, T_J=25°C
Q_{rr}	Reverse recovery charge	—	54	—	nC	

Notes:
a. Equivalent capacitance to give same stored energy from 0V to 400V
b. Equivalent capacitance to give same charging time from 0V to 400V

Typical Characteristics (25°C unless otherwise stated)

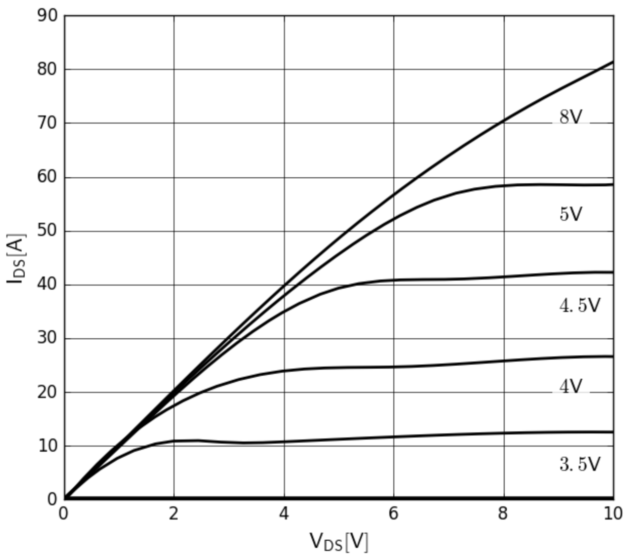


Figure 1. Typical Output Characteristics T_J=25°C
Parameter: V_{GS}

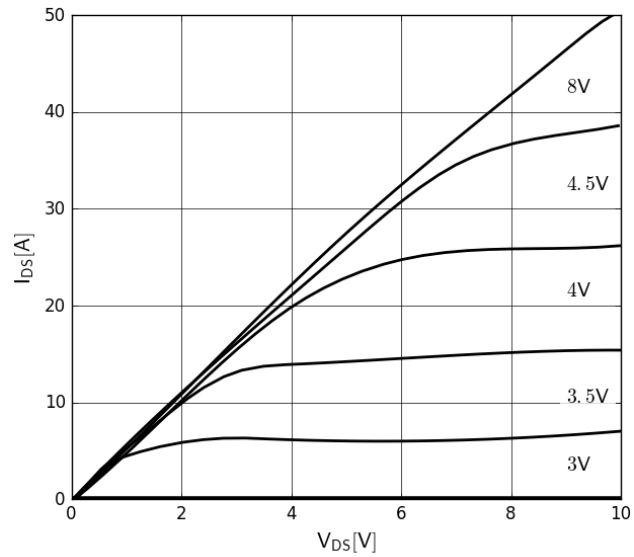


Figure 2. Typical Output Characteristics T_J=150°C
Parameter: V_{GS}

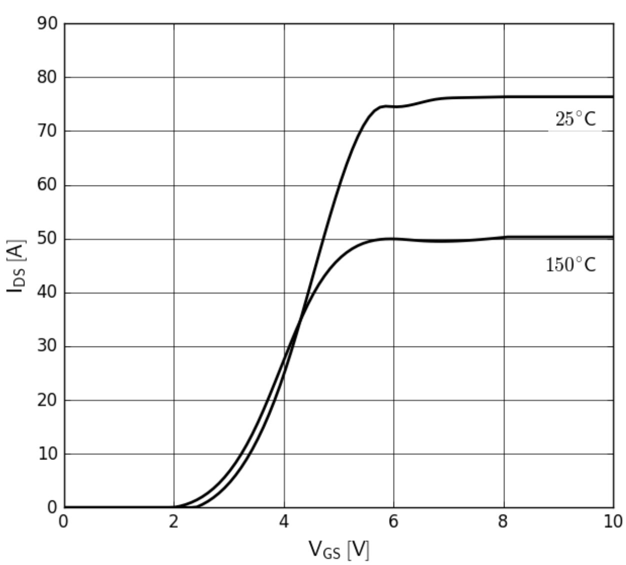


Figure 3. Typical Transfer Characteristics
V_{DS}=10V, parameter: T_J

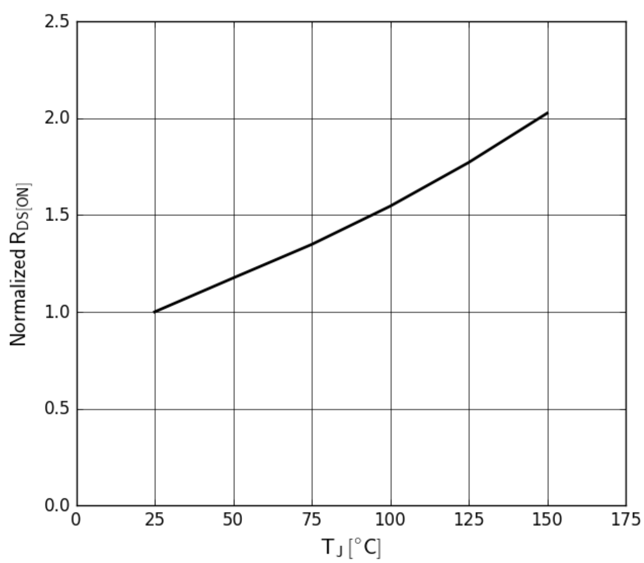


Figure 4. Normalized On-Resistance
I_D=13A, V_{GS}=8V

Typical Characteristics (25°C unless otherwise stated)

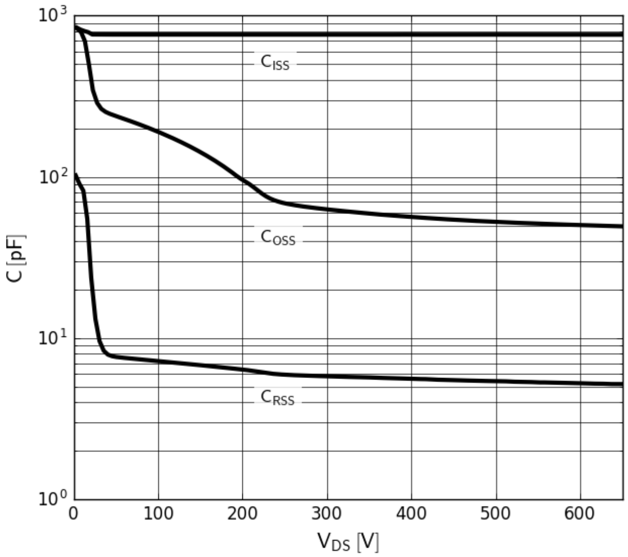


Figure 5. Typical Capacitance

V_{GS}=0V, f=1MHz

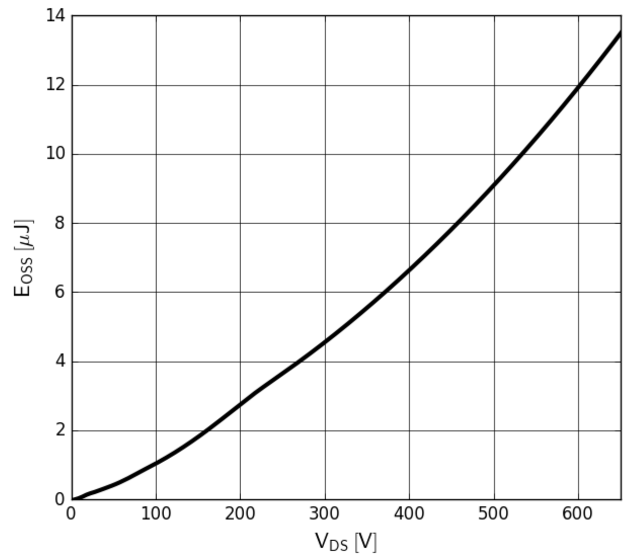


Figure 6. Typical C_{OSS} Stored Energy

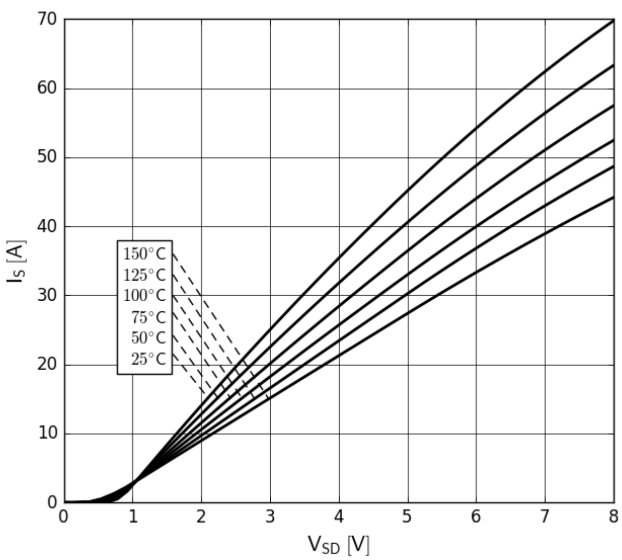


Figure 7. Forward Characteristics of Rev. Diode

I_S=f(V_{SD}), parameter: T_J

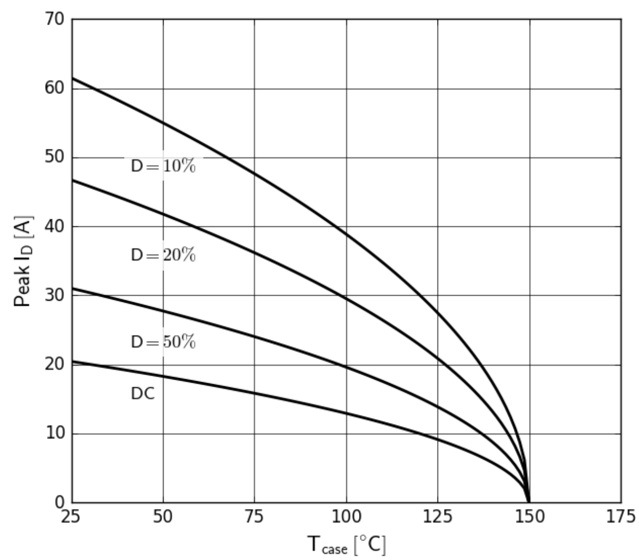


Figure 8. Current Derating

Pulse width ≤ 10μs

Typical Characteristics (25 °C unless otherwise stated)

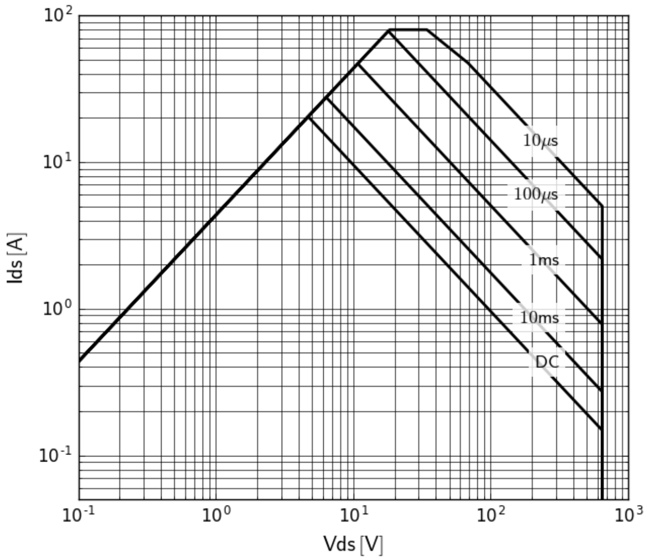


Figure 9. Safe Operating Area T_C=25 °C

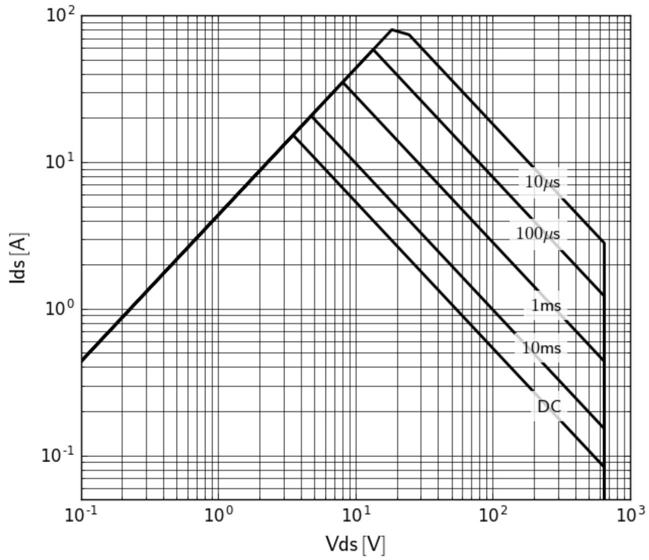


Figure 10. Safe Operating Area T_C=80 °C

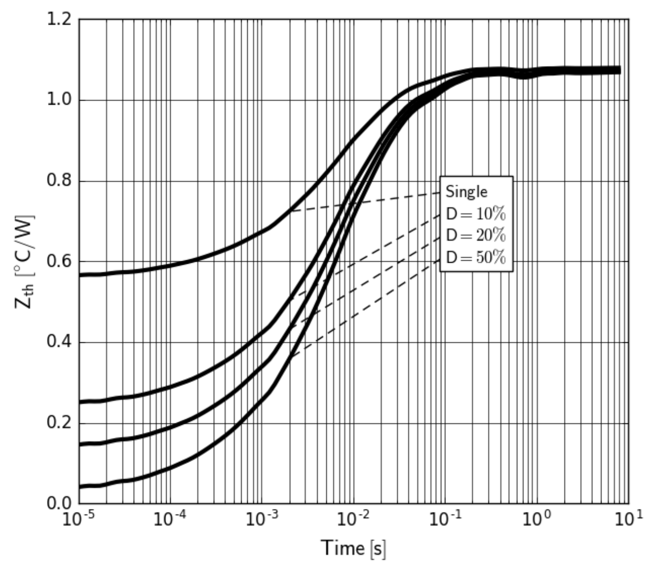


Figure 11. Transient Thermal Resistance

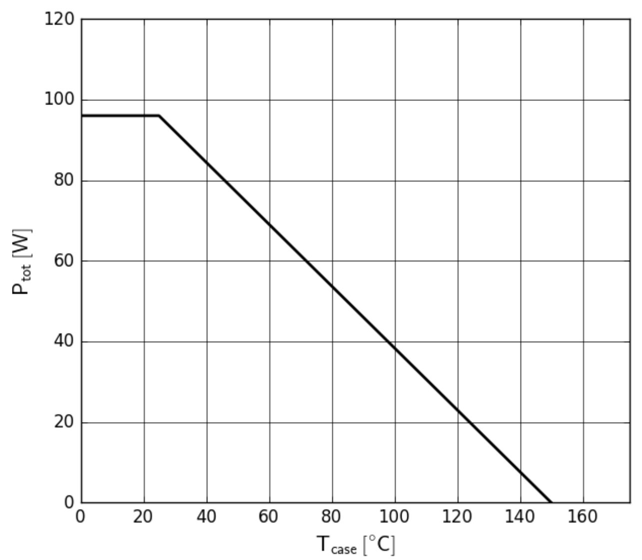


Figure 12. Power Dissipation

Test Circuits and Waveforms

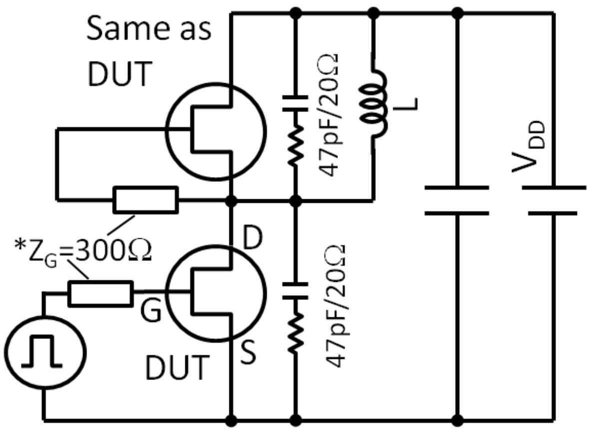


Figure 13. Switching Time Test Circuit
***ferrite bead 300Ω at 100MHz**
(See app note AN0009 for methods to ensure clean switching)

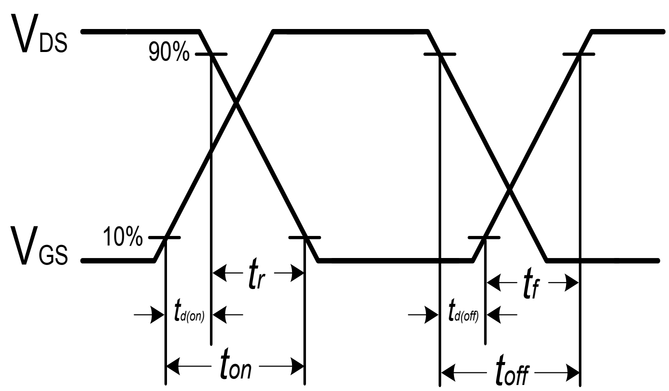


Figure 14. Switching Time Waveform

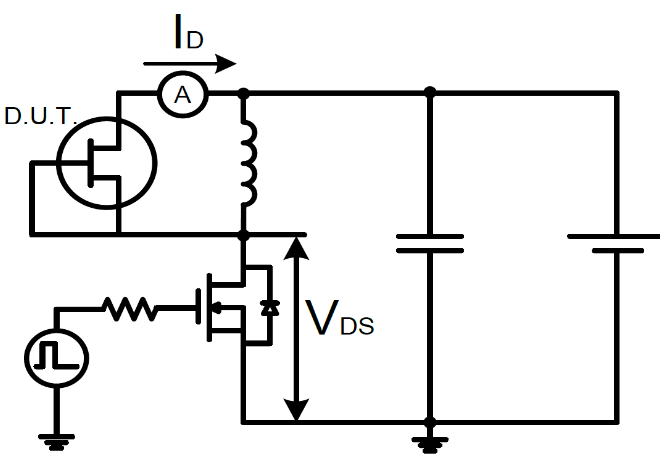


Figure 15. Test Circuit for Reverse Diode Characteristics

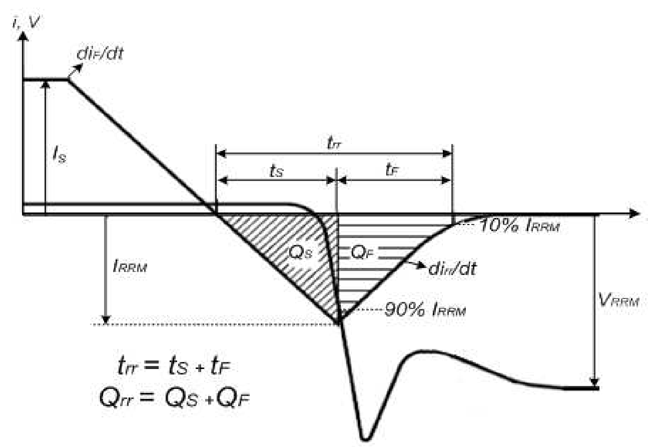
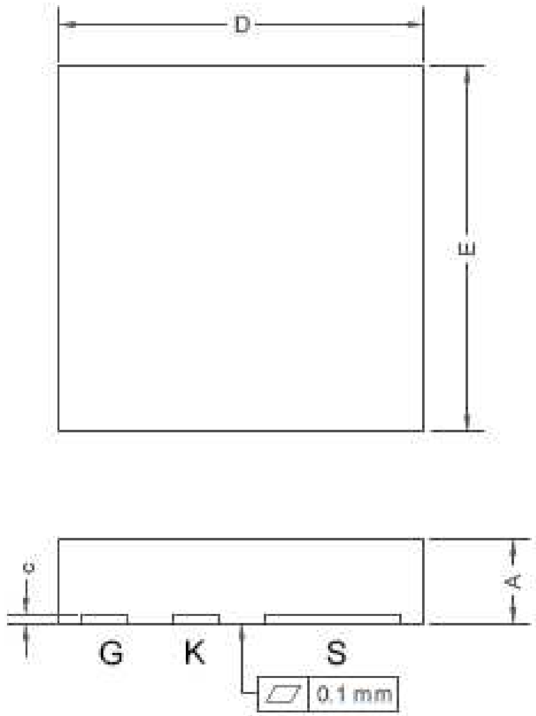
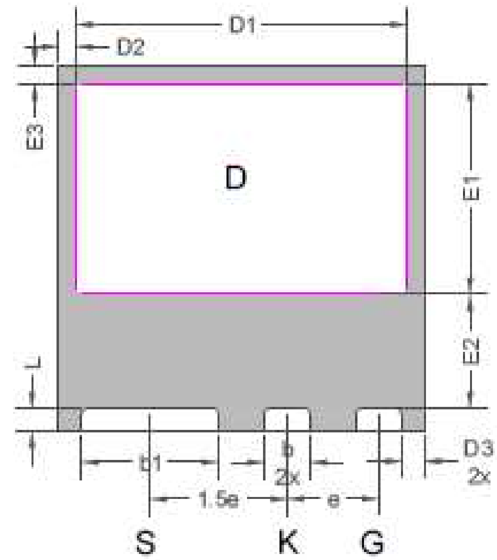


Figure 16. Diode Recovery Waveform

Mechanical

8x8 PQFN (LD) Package





G: Gate
K: Kelvin
S: Source
D: Drain
Lead finish: Sn plating

DIM	mm		inch	
	min	max	min	max
A	1.73	1.97	0.068	0.078
b	0.90	1.10	0.035	0.043
b1	2.90	3.10	0.114	0.122
c	0.10	0.30	0.004	0.012
D	7.90	8.10	0.311	0.319
D1	7.11	7.37	0.280	0.290
E	7.90	8.10	0.311	0.319
E1	4.49	4.75	0.177	0.187
E2	2.40	2.60	0.094	0.102
E3/D2	0.28	0.48	0.011	0.019
D3	0.45	0.55	0.018	0.022
e	2.00 (BSC)		0.079 (BSC)	
L	0.40	0.60	0.016	0.024

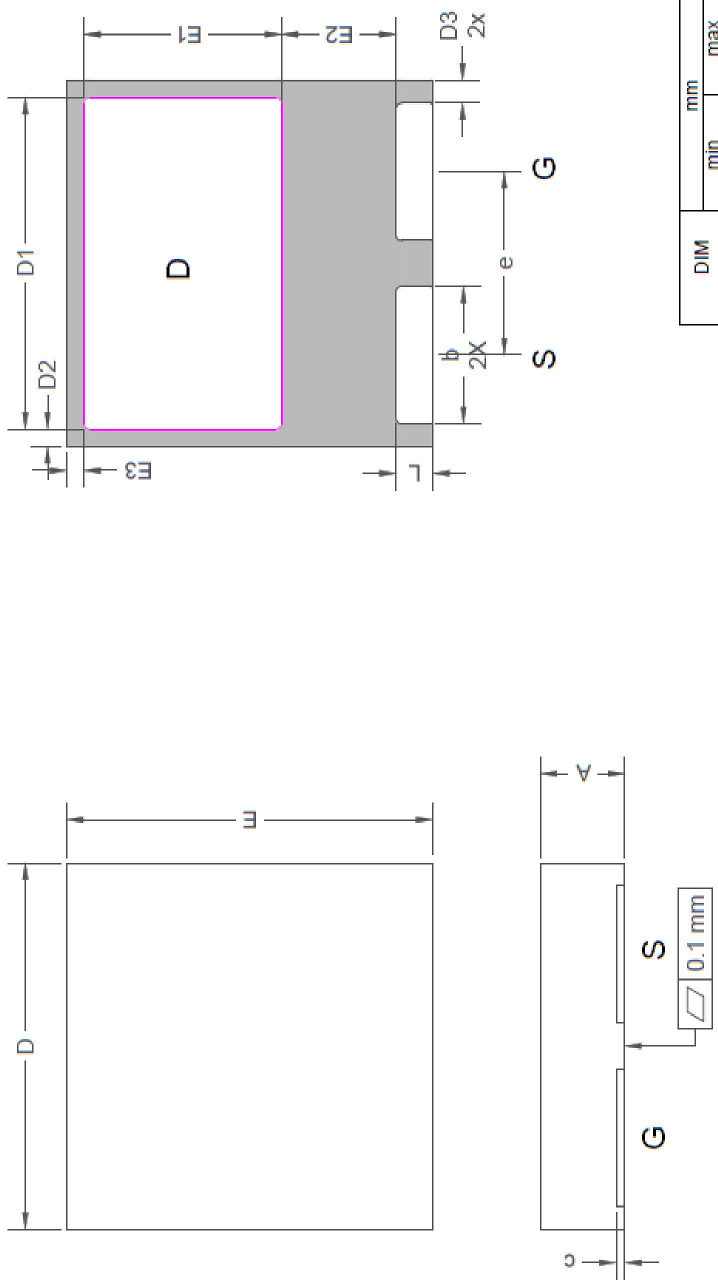
PQFN 8mm x 8mm POD (TPHxxxxLD)

transphorm

SCALE 1:1 | SHEET 1/1 | DRAWING NO. 200072 | VER: 2

8x8 PQFN (LDG) Package

Mechanical



DIM	mm min	mm max	inch min	inch max
A	1.73	1.97	0.068	0.078
b	2.90	3.10	0.114	0.122
c	0.10	0.30	0.004	0.012
D	7.90	8.10	0.311	0.319
D1	7.11	7.37	0.280	0.290
E	7.90	8.10	0.311	0.319
E1	4.18	4.44	0.165	0.175
E2	2.40	2.60	0.094	0.102
E3/D2	0.28	0.48	0.011	0.019
D3	0.45	0.55	0.018	0.022
e	4.00 (BSC)		0.157 (BSC)	
L	0.76	0.86	0.030	0.034

G: Gate
S: Source
D: Drain
Lead finish: Sn plating

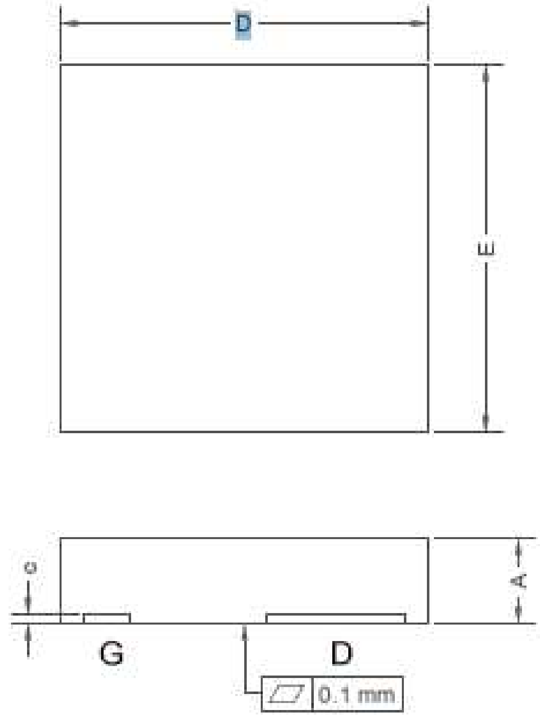
PQFN 8mm x 8mm POD (TPH320xLDG)

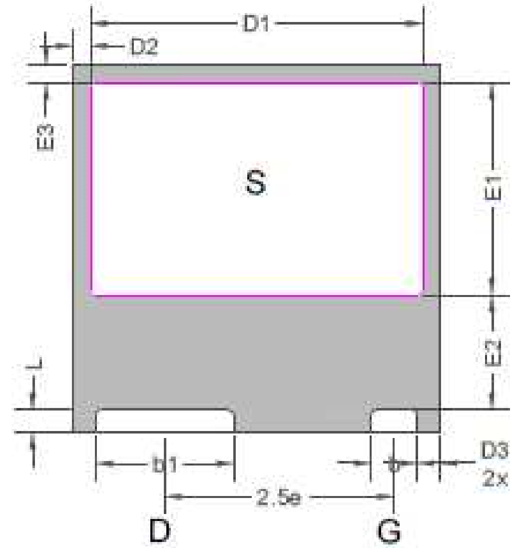
transphorm

SCALE 1:1 | SHEET 1/1 | DRAWING NO. Eng000501 | VER. 2

Mechanical

8x8 PQFN (LS) Package





G: Gate
S: Source
D: Drain
Lead finish: Sn plating

DIM	mm		inch	
	min	max	min	max
A	1.73	1.97	0.068	0.078
b	0.90	1.10	0.035	0.043
b1	2.90	3.10	0.114	0.122
c	0.10	0.30	0.004	0.012
D	7.90	8.10	0.311	0.319
D1	7.11	7.37	0.280	0.290
E	7.90	8.10	0.311	0.319
E1	4.49	4.75	0.177	0.187
E2	2.40	2.60	0.094	0.102
E3/D2	0.28	0.48	0.011	0.019
D3	0.45	0.55	0.018	0.022
e	2.00 (BSC)		0.079 (BSC)	
L	0.40	0.60	0.016	0.024

PQFN 8mm x 8mm POD (TPHxxxxLS)

transphorm

SCALE 1:1 | SHEET 1/1 | DRAWING NO. 200073 | VER. 2

Design Considerations

The fast switching of GaN devices reduces current-voltage cross-over losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note Printed Circuit Board Layout and Probing for GaN Power Switches. The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Transphorm GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See AN0003: Printed Circuit Board Layout and Probing	

Application Notes

- AN0002: Characteristics of Transphorm GaN Power Switches
- AN0003: Printed Circuit Board Layout and Probing
- AN0004: Designing Hard-switched Bridges with GaN
- AN0008: Drain Voltage and Avalanche Ratings for GaN FETs
- AN0009: Recommended External Circuitry for GaN FETs

Evaluation Boards

- TDHBG2500P100-KIT: 2.5KW hard-switched half-bridge, buck or boost evaluation platform

Revision History

Version	Date	Change(s)
0	11/14/2016	Release L series datasheet