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transphorm

TPH3212PS

650V Cascode GaN FET in TO-220 (source tab)

Description

The TPH3212PS 650V, 72mΩ gallium nitride (GaN) FET is a normally-off device. Transphorm GaN FETs offer better efficiency through lower gate charge, faster switching speeds, and smaller reverse recovery charge, delivering significant advantages over traditional silicon (Si) devices.

Transphorm is a leading-edge wide band gap supplier with world-class innovation and a portfolio of fully-qualified GaN transistors that enables increased performance and reduced overall system size and cost.

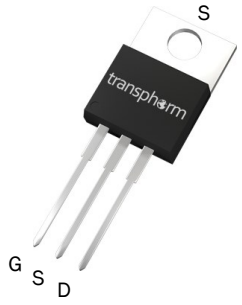
Related Literature

- AN0009: Recommended External Circuitry for GaN FETs
- AN0003: Printed Circuit Board Layout and Probing

Ordering Information

Part Number	Package	Package Configuration
TPH3212PS	3 Lead TO-220	Common Source

TPH3212PS
TO-220
(top view)



Features

- Easy to drive—compatible with standard gate drivers
- Low conduction and switching losses
- Low Qrr of 90nC—no free-wheeling diode required
- GSD pin layout improves high speed design
- JEDEC-qualified GaN technology
- RoHS compliant and Halogen-free

Benefits

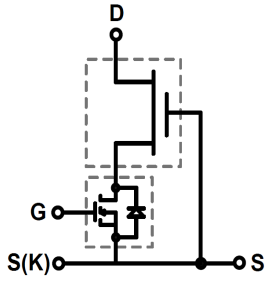
- Increased efficiency through fast switching
- Increased power density
- Reduced system size and weight
- Enables more efficient topologies—easy to implement bridgeless totem-pole designs
- Lower BOM cost

Applications

- Renewable energy
- Industrial
- Automotive
- Telecom and datacom
- Servo motors

Key Specifications	
V_{DS} (V) min	650
V_{TDS} (V) max	800
$R_{DS(on)}$ (mΩ) max*	85
Q_{rr} (nC) typ	90
Qg (nC) typ	14

* Dynamic $R_{(on)}$



Cascode Device Structure

Absolute Maximum Ratings (T_C=25°C unless otherwise stated)

Symbol	Parameter		Limit Value	Unit
$I_{D25°C}$	Continuous drain current @T_C=25°C [a]		26.5	A
$I_{D100°C}$	Continuous drain current @T_C=100°C [a]		16.5	A
I_{DM}	Pulsed drain current (pulse width: 10µs)		120	A
V_{DSS}	Drain to source voltage		650	V
V_{TDS}	Transient drain to source voltage [b]		800	V
V_{GSS}	Gate to source voltage		±18	V
$P_{D25°C}$	Maximum power dissipation		104	W
T_C	Operating temperature	Case	-55 to +150	°C
T_J		Junction	-55 to +150	°C
T_S	Storage temperature		-55 to +150	°C
T_{CSOLD}	Soldering peak temperature [c]		260	°C

Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\Theta JC}$	Junction-to-case	1.2	°C/W
$R_{\Theta JA}$	Junction-to-ambient	62	°C/W

Notes:
a. For high current operation, see application note AN0009
b. In off-state, spike duty cycle D<0.01, spike duration <1µs
c. For 10 sec., 1.6mm from the case

Electrical Parameter (T_C=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{DSS-MAX}$	Maximum drain-source voltage	650	—	—	V	V_{GS}=0V
$V_{GS(th)}$	Gate threshold voltage	1.6	2.1	2.6	V	V_{DS}=V_{GS}, I_D=0.7mA
$R_{DS(on)}$	Drain-source on-resistance (T_J=25°C) [a]	—	72	85	mΩ	V_{GS}=8V, I_D=17A, T_J=25°C
	Drain-source on-resistance (T_J=150°C) [a]	—	148	—		V_{GS}=8V, I_D=17A, T_J=150°C
I_{DSS}	Drain-to-source leakage current (T_J=25°C)	—	3	30	μA	V_{DS}=650V, V_{GS}=0V, T_J=25°C
	Drain-to-source leakage current (T_J=150°C)	—	12	—		V_{DS}=650V, V_{GS}=0V, T_J=150°C
I_{GSS}	Gate-to-source forward leakage current	—	—	100	nA	V_{GS}=18V
	Gate-to-source reverse leakage current	—	—	-100		V_{GS}=-18V
C_{ISS}	Input capacitance	—	1130	—	pF	V_{GS}=0V, V_{DS}=400V, *f*=1MHz
C_{OSS}	Output capacitance	—	102	—		
C_{RSS}	Reverse transfer capacitance	—	13	—		
$C_{O(er)}$	Output capacitance, energy related [b]	—	142	—	pF	V_{GS}=0V, V_{DS}=0V to 400V
$C_{O(tr)}$	Output capacitance, time related [c]	—	225	—		
Q_g	Total gate charge	—	14.6	—	nC	V_{DS}=400V, V_{GS}=0V to 8V, I_D=17A
Q_{gs}	Gate-source charge	—	3.1	—		
Q_{gd}	Gate-drain charge	—	3.4	—		
$t_{d(on)}$	Turn-on delay	—	24	—	ns	V_{DS}=400V, V_{GS}=0V to 10V, I_D=18A, R_G=15Ω (driver internal series resistance), Z_{FB}=300Ω @100MHz (see Fig. 13)
t_r	Rise time	—	7.5	—		
$T_{d(off)}$	Turn-off delay	—	55.5	—		
t_f	Fall time	—	5	—		
Reverse Device Characteristics						
I_S	Reverse current	—	—	16.5	A	V_{GS}=0V, T_C=100°C ≤50% Duty Cycle
V_{SD}	Reverse voltage [a]	—	2.0	—	V	V_{GS}=0V, I_S=17A, T_J=25°C
		—	1.5	—		V_{GS}=0V, I_S=8.5A, T_J=25°C
t_{rr}	Reverse recovery time	—	35	—	ns	I_S=18A, V_{DD}=400V, di/dt=1000A/ms, T_J=25°C
Q_{rr}	Reverse recovery charge	—	90	—	nC	

Notes:
a. Dynamic value
b. Equivalent capacitance to give same stored energy from 0V to 400V
c. Equivalent capacitance to give same charging time from 0V to 400V

Typical Characteristics (25 °C unless otherwise stated)

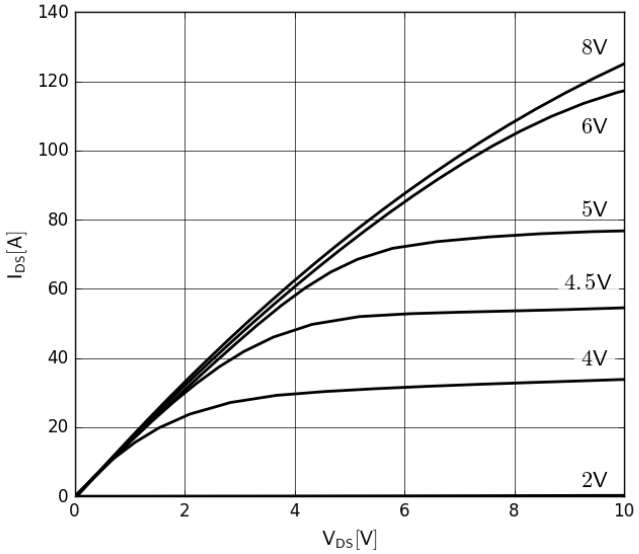


Figure 1. Typical Output Characteristics T_J=25 °C
Parameter: V_{GS}

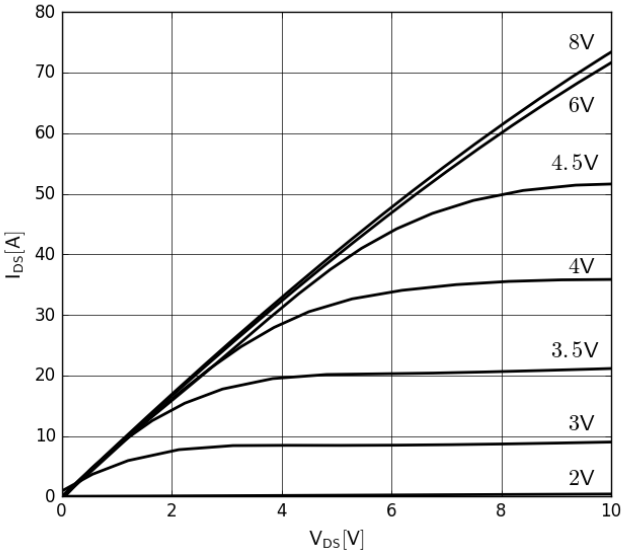


Figure 2. Typical Output Characteristics T_J=150 °C
Parameter: V_{GS}

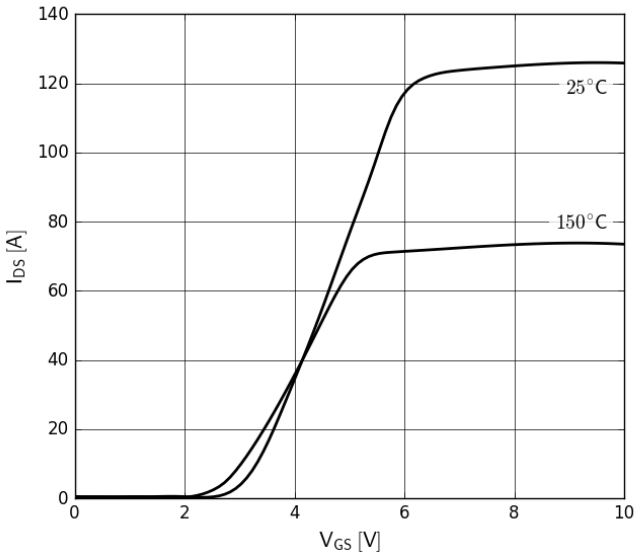


Figure 3. Typical Transfer Characteristics
V_{DS}=10V, Parameter: T_J

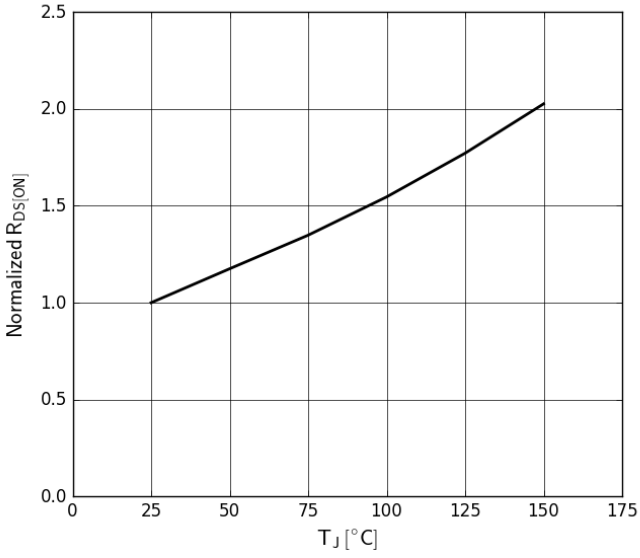


Figure 4. Normalized On-Resistance
I_D=17A, V_{GS}=8V

Typical Characteristics (25 °C unless otherwise stated)

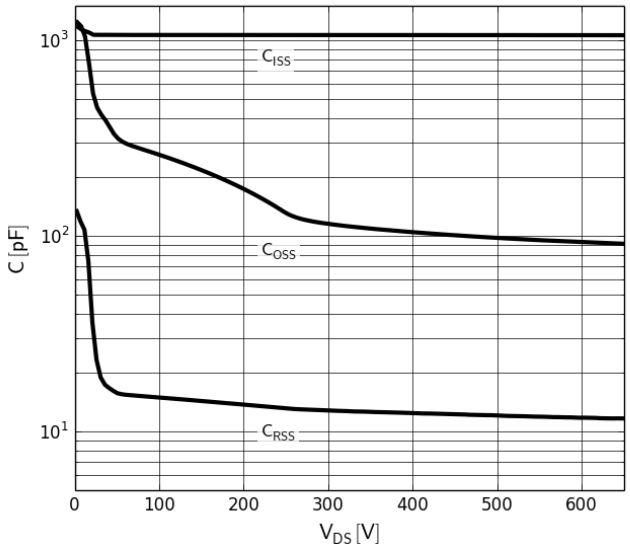


Figure 5. Typical Capacitance
V_{GS}=0V, f=1MHz

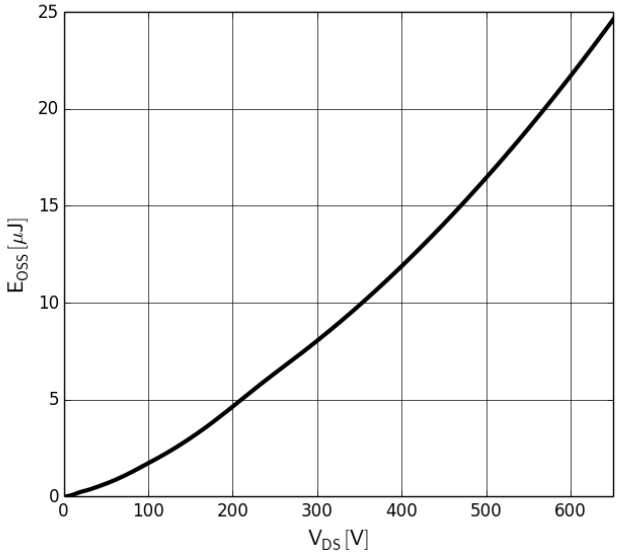


Figure 6. Typical C_{oss} Stored Energy

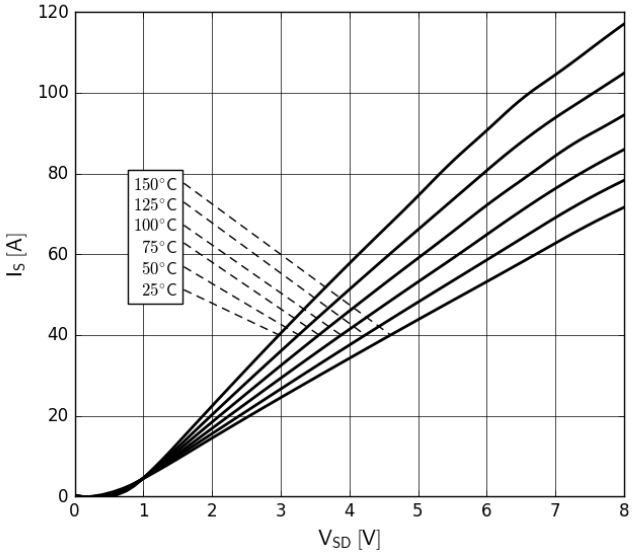


Figure 7. Forward Characteristics of Rev. Diode
I_S=f(V_{SD}), Parameter T_J

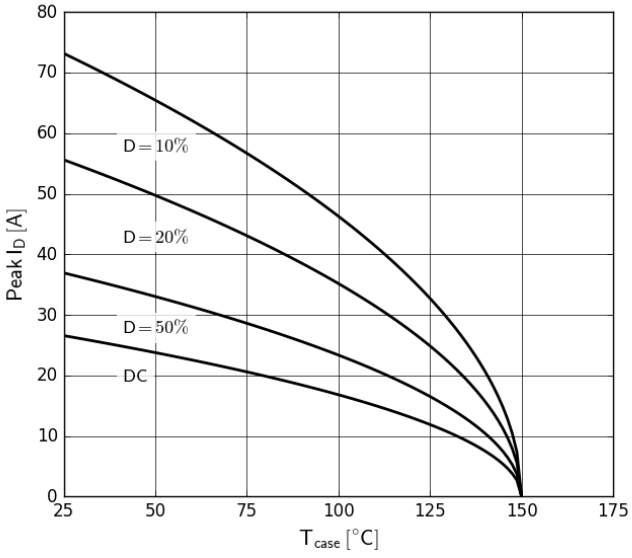


Figure 8. Current Derating
Pulse width ≤ 10µs

Typical Characteristics (25 °C unless otherwise stated)

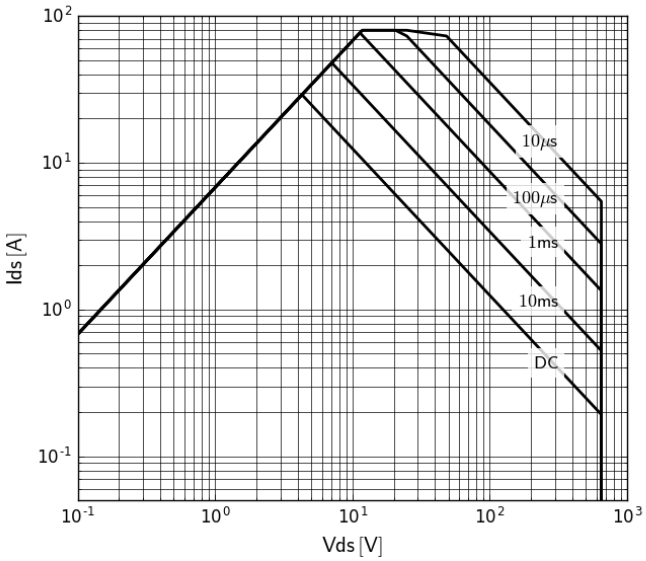


Figure 9. Safe Operating Area T_C=25 °C (calculated based based on thermal limit)

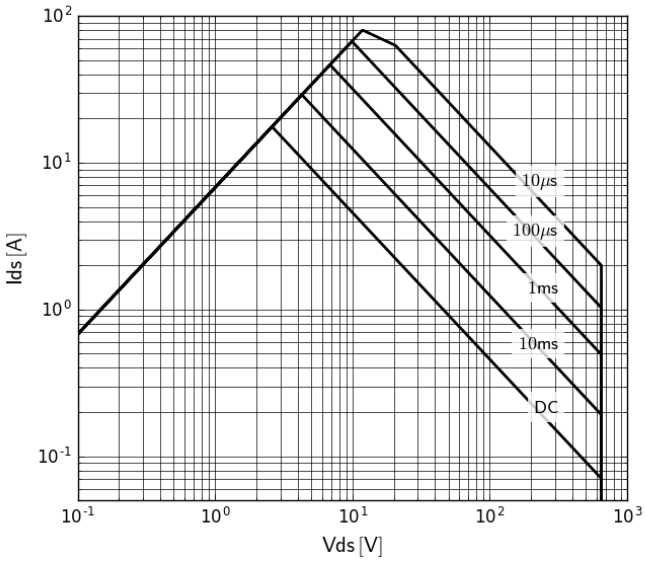


Figure 10. Safe Operating Area T_C=80 °C (calculated based on thermal limit)

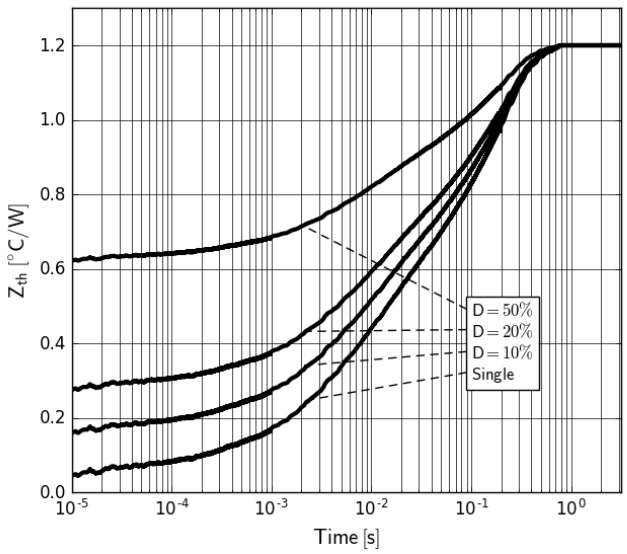


Figure 11. Transient Thermal Resistance

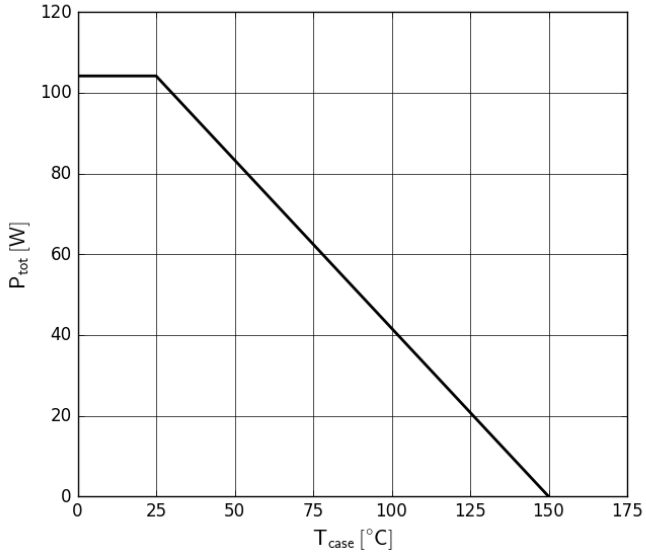


Figure 12. Power Dissipation

Test Circuits and Waveforms

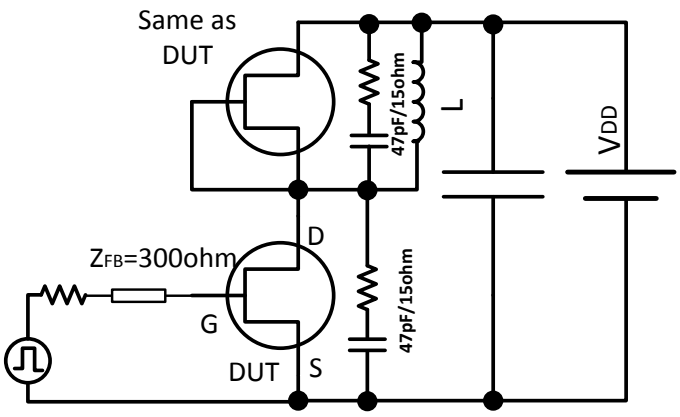


Figure 13. Switching Time Test Circuit
***See app note AN0009 for methods to ensure clean switching**

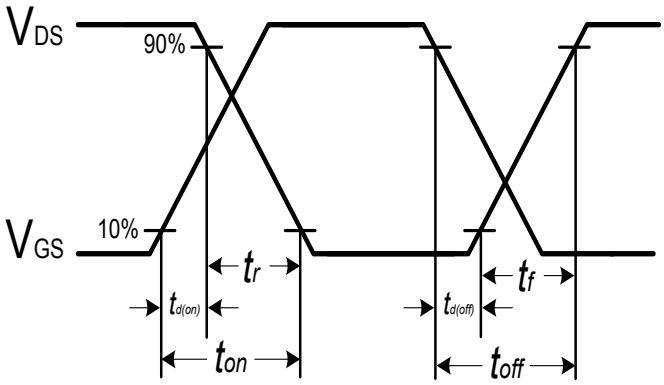


Figure 14. Switching Time Waveform

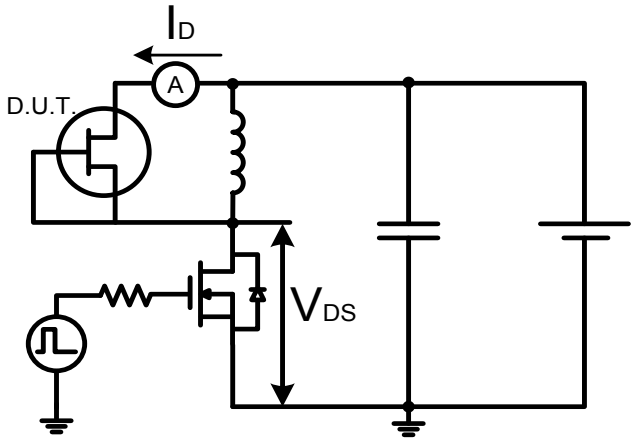


Figure 15. Test Circuit for Diode Characteristics

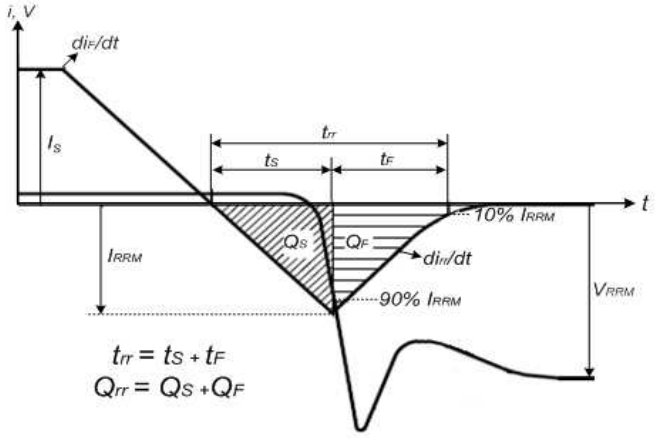


Figure 16. Diode Recovery Waveform

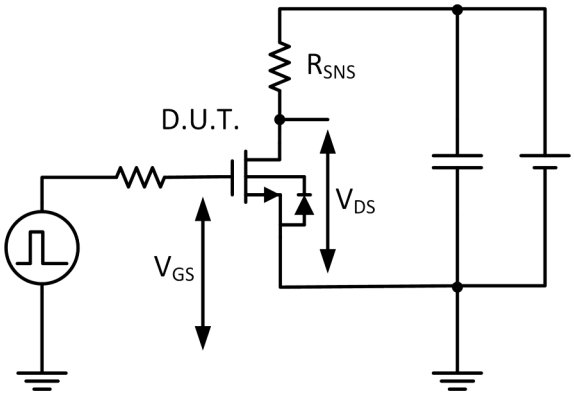


Figure 17. Test Circuit for Dynamic $R_{DS(on)}$

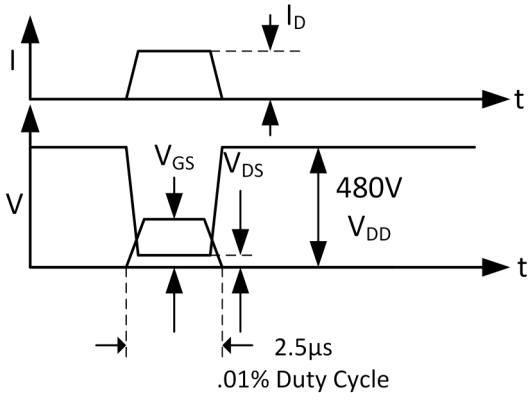
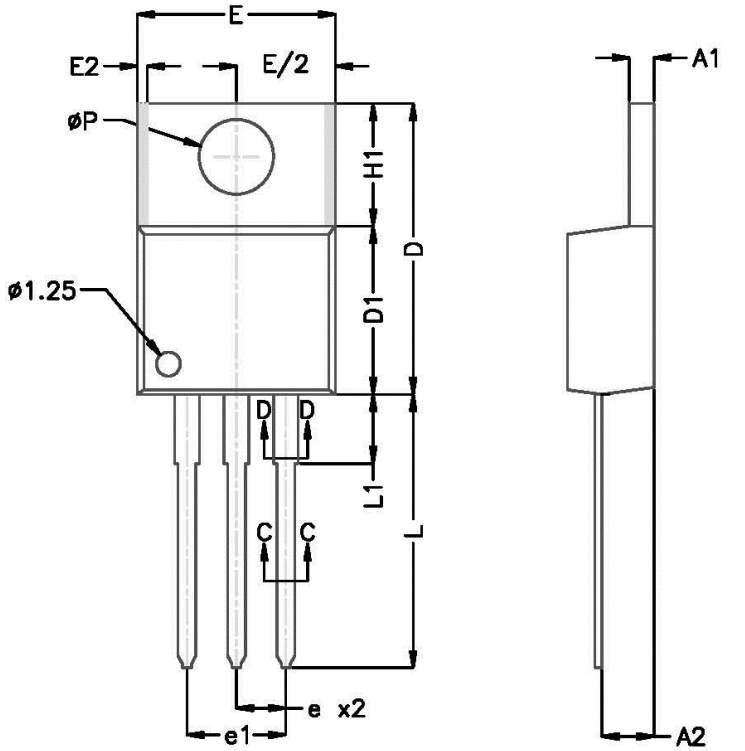


Figure 18. Dynamic $R_{DS(on)}$ Waveform

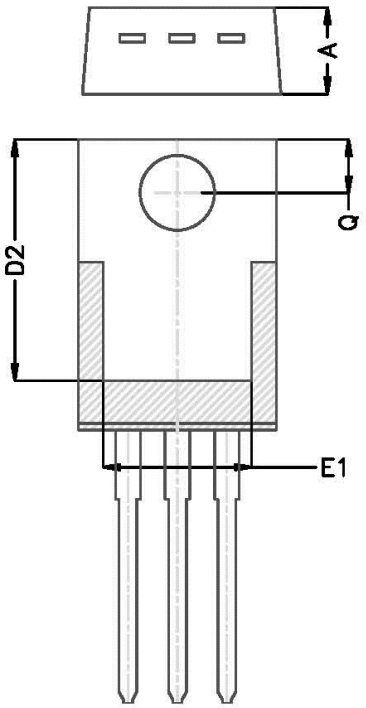
Mechanical

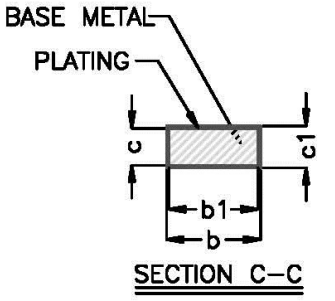
3 Lead TO-220 (PS) Package

Pin 1: Gate; Pin 2: Source; Pin 3: Drain, Tab: Source

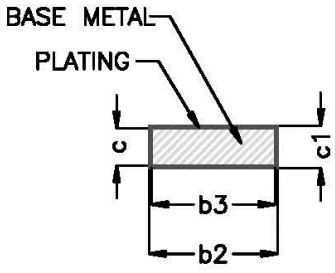


SYMBOL	MILLIMETERS			INCHES		
	MINIMUM	NOMINAL	MAXIMUM	MINIMUM	NOMINAL	MAXIMUM
A	3.56	4.45	4.83	0.140	0.175	0.190
A1	0.51	1.27	1.40	0.020	0.050	0.055
A2	2.03	–	2.92	0.080	–	0.115
b	0.38	–	1.01	0.015	–	0.040
b1	0.38	–	0.97	0.015	–	0.038
b2	1.14	–	1.78	0.045	–	0.070
b3	1.14	1.27	1.73	0.045	0.050	0.068
c	0.36	–	0.61	0.014	–	0.024
c1	0.36	0.38	0.56	0.014	0.015	0.022
D	14.22	–	16.51	0.560	–	0.650
D1	8.38	8.64	9.02	0.330	0.340	0.355
D2	11.68	–	12.88	0.460	–	0.507
E	9.65	10.19	10.67	0.380	0.401	0.420
E1	6.86	–	8.89	0.270	–	0.350
E2	–	–	0.76	–	–	0.030
e	2.54 BSC			0.100 BSC		
e1	5.08 BSC			0.200 BSC		
H1	5.84	6.30	6.86	0.230	0.248	0.270
L	12.70	14.05	14.73	0.500	0.553	0.580
L1	–	–	6.35	–	–	0.250
øP	3.54	3.84	4.08	0.139	0.151	0.161
Q	2.54	–	3.42	0.100	–	0.135





SECTION C–C



SECTION D–D

NOTES:

1. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 MM (0.005") PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
2. DIMENSIONS E2 & H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
3. OUTLINE CONFORMS TO JEDEC TO-220AB.

Design Considerations

The fast switching of GaN devices reduces current-voltage cross-over losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note Printed Circuit Board Layout and Probing for GaN Power Switches. The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Transphorm GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See AN0003: Printed Circuit Board Layout and Probing	

Application Notes

- AN0002: Characteristics of Transphorm GaN Power Switches
- AN0003: Printed Circuit Board Layout and Probing
- AN0004: Designing Hard-switched Bridges with GaN
- AN0008: Drain Voltage and Avalanche Ratings for GaN FETs
- AN0009: Recommended External Circuitry for GaN FETs

Evaluation Boards

- TDHBG2500P100-KIT: 2.5KW hard-switched half-bridge, buck or boost evaluation platform

Revision History

Version	Date	Change(s)
10	11/14/2016	Add application note AN0009
11	12/12/2016	Formatting Changes to p. 3, revision of dynamic measurement verbiage