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Tri-Rate Serial Digital Interface Physical Layer IP Core User's Guide

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Introduction

Serial Digital Interface (SDI) is the most popular raw video connectivity standard used in television broadcast studios and video production facilities. The availability of high-speed serial inputs/outputs and general purpose programmable logic makes FPGAs (field programmable gate arrays) ideal devices to be used for acquisition, mixing, storage, editing, processing and format conversion applications. Simpler applications use FPGAs to acquire SDI data from one or more SD (standard definition), HD (high definition) or 3G (3-Gigabit HD) sources, perform simple processing and re-transmit the video data in SDI format. Such applications require an SDI PHY (physical layer) interface and some basic processing blocks like a color space converter. In more complex applications, the acquired video is taken through multiple processing phases, like de-interlacing, video format conversion, filtering, scaling, graphics mixing and picture-in-picture display. FPGA devices can also be used as a bridge between SDI video sources and backplane protocols such as PCI Express or ethernet, with or without any additional video processing.

In an FPGA-based SDI solution, the physical interface portion is often the most challenging part of the solution. This is because the PHY layer includes several device-dependent components like the high-speed I/Os (inputs/outputs), serializer/de-serializer, clock/data recovery, word alignment and timing signal detection logic. Video processing, on the other hand, is algorithmic and is usually achieved using proprietary algorithms developed by the user's in-house design engineering teams.

The Lattice Tri-Rate SDI PHY intellectual property (IP) core is a complete SDI PHY interface that connects to the high-speed SDI serial data on one side (through LatticeECP3™ SERDES) and the formatted parallel video data on the other side. It enables faster development of applications for processing, storing, and bridging SDI video data. It is comprised of the following major functional blocks: SDI encoder/decoder, word alignment, CRC detection and checking, VPID (video payload identifier) insertion and extraction, and rate detection logic. The IP core supports the following interface standards and source formats for SDI as specified in standards published by the Society for Motion Picture and Television Engineers (SMPTE).

Interface:	SMPTE 259M-2006 [1] (SD), SMPTE 292M-1998 [2] (HD) and SMPTE 424 M [3] (3G)
SD source formats:	SMPTE 125M [4] and SMPTE 267M [5] (13.5 MHz only)
HD source formats:	SMPTE 260M [6], SMPTE 274M [7], SMPTE 295M [8] and SMPTE 296M [9]
3G source formats:	SMPTE 425M [10]

The Tri-Rate SDI PHY IP core, when connected with the LatticeECP3 SERDES, can transmit and/or receive any of the supported video standards and formats through a common physical serial interface. The Tri-Rate SDI PHY IP core can automatically scan and lock on to any of the supported video streams. Receiving multiple standards requires appropriate external clocks to be supplied by the application in response to commands from the Tri-Rate SDI PHY IP core.

Quick Facts

Table 1-1 gives quick facts about the Tri-Rate SDI PHY IP core for LatticeECP3 devices.

Table 1-1. Tri-Rate SDI PHY IP Core Quick Facts

		Tri-Rate SDI PHY IP Core		
		Tx Only	**Rx Only**	**Both Tx and Rx**
Core Requirements	FPGA Families Supported	LatticeECP3		
	Minimal Devices Needed	LFE3-17EA-6FTN256C		
Typical Resource Utilization	Targeted Device	LFE3-95EA-7FN1156C		
	Data Path Width	20		
	LUTs	850	1700	2500
	sysMEM EBRs	0		
	Registers	500	1300	1800
Design Tool Support[1]	Lattice Implementation	Lattice Diamond® 1.3 or ispLEVER® 8.1		
	Synthesis	Synopsys® Synplify™ Pro for Lattice E-2011.03L		
		Mentor Graphics® Precision™ RTL Synthesis 2010a_Update 2.254		
	Simulation	Aldec® Active-HDL™ 8.2 Lattice Edition		
		Mentor Graphics ModelSim™ SE 6.5		

1. Design tool support for IP core version 1.3.

Features

- Dynamic reception of multiple interface standards over the same physical cable: SD-SDI, HD-SDI and 3G-SDI interfaces
- Automatic Rx (receive) rate detection and dynamic Tx (transmit) rate selection
- Multiple SD source formats support: SMPTE 125M [4] and SMPTE 267M [5] (13.5 MHz only)
- Multiple HD source formats support: SMPTE 260M [6], SMPTE 274M [7], SMPTE 295M [8] and SMPTE 296M [9]
- Support for 3G source formats, including 3G Level-B format: SMPTE 425M [10]
- Word alignment and timing reference sequence (TRS) detection
- Field, vertical blanking (vblank) and horizontal blanking (hblank) timing signals generation
- CRC computation, error checking and insertion for HD/3G
- Line number (LN) decoding and encoding for HD/3G
- Custom source format support for HD/3G
- Video Payload Identifier (VPID) insertion and extraction for HD/3G
- 10-bit parallel input/output support for SD
- Soft-logic based low data-rate (LDR) serializer for SD transmission

Video Interface and Source Format Support

This Tri-Rate SDI PHY IP core supports SMPTE 259, SMPTE 292 and SMPTE 424 interface standards.

SMPTE 259 standard is applicable to 4:2:2 video streams defined by SMPTE 125M and SMPTE 267M. These source formats are briefly described below.

1. SMPTE 125M: System M – 525 lines and 60 fields based on ITU-R BT.601. The video is transmitted in the form of one luminance (Y) and two color-difference components (scaled versions of R-Y and B-Y). It follows a 4:2:2 family level of ITU-R BT.601 with a nominal luminance sampling at 13.5 MHz allowing for both 8-bit and 10-bit data types.

2. SMPTE 267M: System M – 525 lines and 59.94 fields, wide screen, 16x9 aspect ratio, based on ITU-R BT.601. The video is transmitted in the form of one luminance (Y) and two color-difference components (scaled versions of R-Y and B-Y). It follows a 4:2:2 family level of ITU-R BT.601 with a nominal luminance sampling at 13.5 MHz or 18 MHz, allowing for both 8-bit and 10-bit data types.

This IP core supports all of SMPTE 125M and only the 13.5 MHz version of SMPTE 267M.

SMPTE 292 defines a serial data rate of 1.485 Gbps and 1.485/M Gbps, where M = 1.001. This interface standard supports the source formats defined in the four SMPTE standards: SMPTE 260M, SMPTE 295M, SMPTE 274M and SMPTE 296M. The IP core can transmit, receive and identify all of these source formats. In addition to these formats, the IP core can be configured to receive any custom source format as long as the data conforms to the SMPTE 292M interface standard. This is achieved by allowing the user to define the source format in terms of the number of words between SAV (start of active video) and the next EAV (end of active video) and the number of words between EAV and the next SAV. It is also possible to have the IP receive multiple custom source formats by specifying a range for the above values.

The source format support for SMPTE 424M is specified by the SMPTE 425M specification [10]. SMPTE 425 defines four mapping structures that map the HD source formats to the 3G interface. The higher stream rate is used to accommodate 4:2:2 50p, 4:2:2 60p, 4:4:4, 4:4:4:4 and 12-bit formats. The Lattice Tri-Rate SDI PHY IP core detects the interface standard as 3G and the source format as one of many video and frame formats. The IP also supports the transmission and reception of 3G Level-B video formats. The following mapping nomenclature specified in SMPTE 425M are supported:

- SMPTE 372M dual link payloads on a 3 Gbps interface
- 2x720-line video payloads on a 3 Gbps interface
- 2x1080-line video payloads on a 3 Gbps interface

This chapter describes the functionality of the Tri-Rate SDI PHY IP core. The high-level functional diagram of the Tri-Rate SDI PHY IP core is shown in Figure 2-1.

Figure 2-1. Tri-Rate SDI PHY IP Core, High-Level Functional Diagram

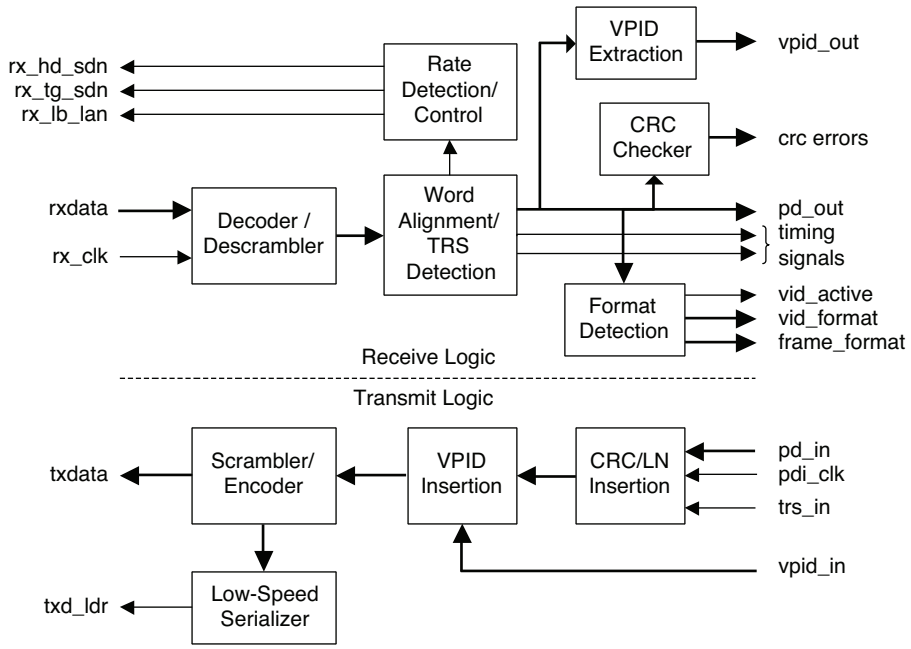


Figure 2-1 shows the top-level functional view of the IP core. As shown, the Tri-Rate SDI PHY IP core does not include the LatticeECP3 SERDES in it. The top portion of the diagram shows the receiver and the bottom portion the transmitter.

The Tri-Rate SDI PHY IP core is capable of receiving any of the video formats specified in the SMPTE 259M, SMPTE 292M and SMPTE 424M interface standards through the same physical input without the need for any manual intervention. The receiver can dynamically support the different video stream rates: SD video at 270 Mbps, HD integer frame rate video at 1.485 Gbps, HD fractional frame rate video at 1.4835 Gbps, 3G integer frame rate video at 2.97 Gbps and 3G fractional frame rate video at 2.967 Gbps. The multi-rate receiver cyclically scans for each of the video rates until it identifies and locks to the incoming video data. When scanning for a video rate, the IP core gives out the interface rate that it is trying to receive. The SERDES settings and reference clocks have to be changed to match this rate information. If there is a valid video corresponding to the scanned rate, the IP core locks to the video source and provides the parallel data and status outputs for that video. If no video is received or if there are multiple errors in the received data, the receiver goes on to scan the next rate. The scanning process continues until the receiver “locks” to the incoming video, that is, when the video data reception is valid and error-free for a few lines of video data.

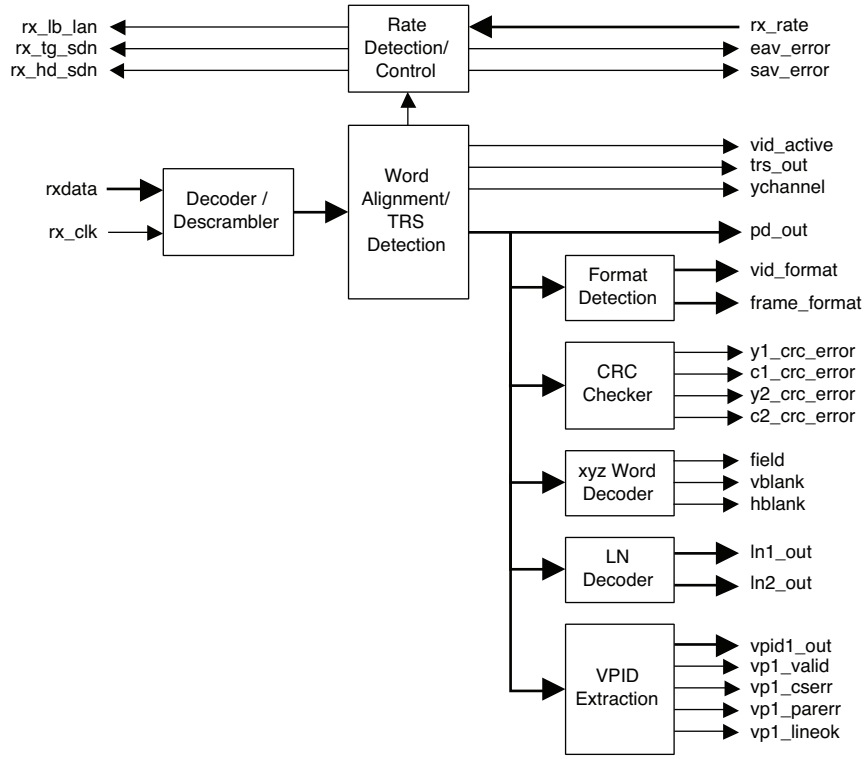
The Tri-Rate SDI PHY IP core is also capable of supporting dynamically varied transmit rates. The different video rates, viz., SD, HD and 3G are identified by the rate select input signals. The Tri-Rate SDI PHY IP core assumes that the clocks and the data applied at the inputs correspond to the rate select signals.

Receiver

A high-level block diagram of the tri-rate SDI receiver is shown in Figure 2-2. The receive side logic is comprised of the following logic blocks: decoder/descrambler, word alignment/TRS detection, rate detection and control, format

detection, CRC checker, XYZ word decoder, LN decoder and VPID extraction module. A description of each of these blocks is given below.

Figure 2-2. Tri-Rate SDI Receiver, High-Level Block Diagram



Decoder/Descrambler

All the interface standards supported by the Tri-Rate SDI PHY IP core specify the same scrambling and encoding methods. The polynomials used are given in the sub-section on the scrambler. The decoder/descrambler is implemented in the 20-bit parallel path. The input data is first decoded to NRZ and then descrambled following an essentially reverse process of the encoding and scrambling operations.

Word Alignment/TRS Detection

The receiver reads the raw, possibly misaligned parallel data from the SERDES. The word alignment block determines the degree of misalignment (offset) by looking for the special TRS sequences in the data. TRS is the unique sequence, 3FFh,000h,000h, in the video stream that marks either the end of active video (EAV) or the start of active video (SAV) time instants. In HD and 3G Level-A video streams, since two independent video streams are interleaved, the timing reference sequence to look for is $3FF_h$, $3FF_h$, 000_h, 000_h, 000_h, 000_h. The TRS for 3G Level-B video is $3FF_h$, $3FF_h$, $3FF_h$, $3FF_h$, 000_h, 000_h, 000_h, 000_h, 000_h, 000_h, 000_h, 000_h. Once the offset is determined, the words are re-aligned using the offset value.

Rate Detection and Control

This module is the heart of the multi-rate SDI receiver infrastructure. Rate detection is the process of determining the interface standard of the incoming video stream. Rate detection is performed by sequentially scanning the input for different interface standards. During each rate scan, the receiver identifies the rate that is being scanned through some output ports, to allow the external modules like the SERDES and clock generator, to be set to that rate. Once the clock generator and the SERDES are set to a data rate, the receiver tries to receive the signal for that rate. The receiver checks the TRS instances (number of active words and total words) to see if they are consistent with the source formats for the interface standard that is being received. If they match, the receiver locks to this

video stream and asserts the vid_active signal. On the other hand, if the TRS instances are not consistent with the source formats that are expected for the current scanned rate, the receiver advances to scan the next rate.

The rate detection state machine is set to scan for the HD rate first, followed by 3G and SD rates and then to go back to scan HD to start the sequence over. The state machine advances to scan the next rate only if that rate is enabled by the dynamic input signal rx_rate. For each scan rate, the state machine goes through three states- "Program", "Check" and "Lock". The state advances are based on the number of TRS matches, TRS mismatches and time-out errors. A time-out error occurs when a TRS is not received in a reasonably long duration of time. During the "Program" state, the external clock sources are set to provide the relevant clocks and/or the SERDES dividers are set to receive the relevant rate. If a TRS is received or if the number of time-out errors is more than the value set using "3G (HD/SD) Programming time" parameter, the state machine advances to the "Check" state. While in the "Check" state, if the number of TRS matches reaches the value set for "Lock match threshold" parameter, the state machine advances to "Lock" state. On the other hand, if the number of TRS mismatches and time-out errors exceeds the "Unlock error threshold" value, the state machine advances to the "Check" state for the next rate. While in the "Lock" state, the state machine continues to be in that state as long the number of time-out and TRS mismatch errors are within "Unlock error threshold" value. When the number of errors exceeds the threshold while in the "Lock" state, the state machine advances to the "Check" state for the next rate.

SMPTE 292M and SMPTE 424M also define a fractional frame rate video stream compliant with the North American standards. Thus SMPTE 292M includes a 1.4835 Gbps data rate in addition to the 1.485 Gbps rate and SMPTE 424M includes a 2.967 Gbps data rate in addition to the 2.97 Gbps rate. This IP core supports both the integer and fractional frame rates, as long as the data and clock inputs to the IP core are consistent with the corresponding rates. While the IP core can receive both integer and fractional frame rate standards, it will not be able to distinguish between the two. However, integer or fractional frame rate standards can be easily determined by constructing a small logic circuit outside the IP to compare the frequency of the receive recovered clock with that of another clock of known frequency (like the receive reference clock or the 100 MHz clock available on the LatticeECP3 Video Protocol Board).

Format Detection

This module determines the source format of the input video stream. The format is based on the number of active words, number of total words and whether the video is interlaced. The format is provided through the vid_format and frame_format output ports. For 3G Level-B video (3G-b), the stream 1 video data is used for format detection.

CRC Checker

The CRC checker computes the CRC values for each of the video streams and components and compares those with the CRC values available in CR0 and CR1 words of the received video. In HD and 3G Level-A video (3G-a) streams, there are two CRC words per line that contain the CRC value for the previous line. The CRC checker computes the CRC for each line, compares with the received CRC and flags an error if there is a mismatch. For 3G-b, there are four CRC words, one each for the Y and C components of each stream. Errors are flagged separately for each of the four CRC comparisons.

XYZ Word Decoder

This block decodes the "XYZ" word that follows the TRS in the video stream. By decoding the XYZ word, the video timing signals field, hblank (horizontal blanking) and vblank (vertical blanking) are determined. XYZ word is also used to determine whether the TRS corresponds to an EAV or a SAV instant.

LN Decoder

In HD and 3G video formats, the line number is encoded as a two-word sequence and inserted after the XYZ word of the EAV sequence. The LN decoder block decodes the line number from the LN double words and gives out the line number value on the ln1_out port. For 3G-b, the line numbers for stream 1 and stream 2 video are separately given out on ln1_out and ln2_out ports respectively.

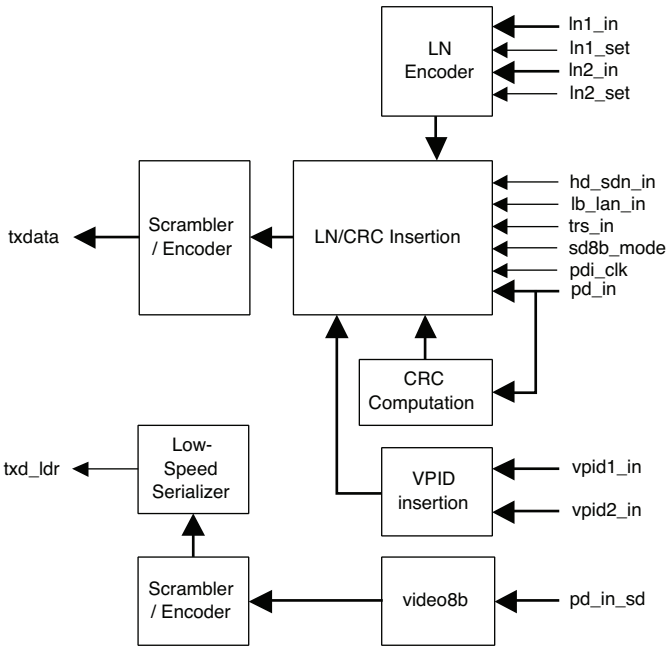
VPID Extraction

The VPID extraction module extracts the video payload information (SMPTE 352M [11]) embedded in the HANC part of the video stream. In addition to the VPID bytes, this module also provides some error and status signals. The status signal vp1_valid indicates whether the last received VPID information was valid and the signal vp1_lineok indicates if the VPID was available in the appropriate line numbers for the received format. The error signals vp1_cserr and vp1_parerr are used to denote the checksum error and parity error respectively.

Transmitter

The transmitter supports dynamic multi-rate operation catering to SD, HD and 3G standards. The transmit rate is set through the input ports, hd_sdn_in and lb_lan_in as well by the frequency of pdi_clk. The transmitter and receiver are independent of each other and each can be used to transport any rate or format. A high-level block diagram of the transmitter is shown in Figure 2-3.

Figure 2-3. Multi-Rate SDI Transmitter, High-Level Block Diagram



The input data to the transmitter is SMPTE-formatted parallel video data, which typically includes active video, blanking, ANC (Ancillary), and TRS words. If the CRC and line number (LN) words for HD/3G are available in the video stream, the IP core can pass them on. If the CRC and/or LN information is not available from the stream, the IP can fill them in and insert them in the stream at the right places. The transmitter is comprised of the following logical modules: LN encoder, CRC computation, VPID insertion, LN/CRC insertion, scrambler/encoder and low-speed serializer. A brief description of each of these modules is given below.

LN Encoder

The LN encoder converts the raw line number value read from the input port to two LN words for insertion in the video stream. This module is used only for HD/3G inputs. This module is optional and used only when the LN words are not already available in the video data stream. For 3G-b video, there are two line number input ports, ln1_in and ln2_in, one for each of the two 3G-b video streams.

CRC Computation

The CRC computation module is optionally added if the CRC insertion option is enabled through the IP GUI. The CRC is computed separately for each Y and C component of the entire active line, encoded to two CRC words per component and embedded at the appropriate places in the next line. For 3G-b streams, there are four separate

CRC computations, one for each component and each stream. Line-based CRC is supported only for HD/3G standards, i.e., when the input hd_sdn_in is high. The CRC is computed using the following polynomial equation:

$$CRC\ (X) = X^{18} + X^5 + X^4 + 1$$

VPID Insertion

This module prepares the VPID words and determines the checksum from the raw VPID value(s) read from vpid1_in (and vpid2_in) port for insertion into the video stream. This module also determines the line number of the current video line and the appropriate line number when the VPID must be inserted for the current standard.

LN/CRC Insertion

This module inserts the computed CRC and LN words at appropriate places in the data stream before the data is sent to the Scrambler/Encoder module.

Scrambler/ Encoder

This module performs scrambling and NRZI (Non-Return to Zero-Inverted) encoding per the requirements set forth in SMPTE 259M, SMPTE 292M and SMPTE 424M standards. The scrambler implements the following equation:

$$G_1(x) = x^9 + x^4 + 1$$

The NRZI encoder is defined by the following equation:

$$G_2(x) = x + 1$$

Low-Speed Serializer

This block is the FPGA fabric-based serializer used for SD video transmission. This is required when fractional frame rate HD/3G and SD streams are to be transmitted from different channels of the same SERDES quad. In this scenario, the low-speed serializer replaces the SERDES serializer for SD transmission.

Signal Descriptions

The top-level interface for the Tri-Rate SDI PHY IP core is shown in Figure 2-4. A brief description of the signals is given in Table 2-1. While the figure and table show the exhaustive port list for the IP core, some ports may not be available for a selected configuration.

Figure 2-4. Tri-Rate SDI PHY IP Core, Top-Level Interface

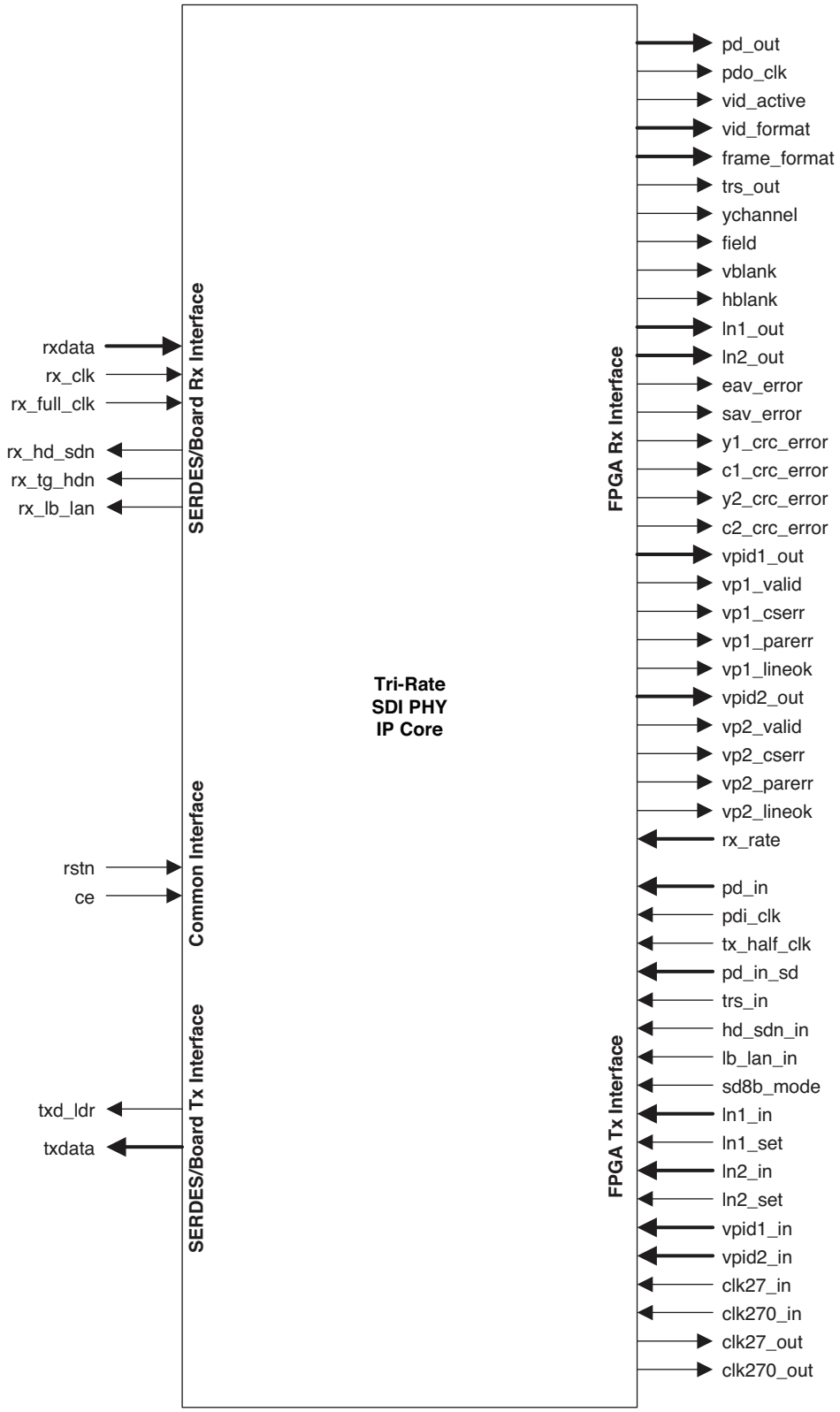


Table 2-1. Top-Level I/O Interface

Port	Bits	I/O	Description
SERDES/Board Rx Interface			
rxdata	20	I	Received data (parallel) from the SERDES. This input is read in using rx_clk.
rx_clk	1	I	This clock is synchronous with rxdata. The frequency of this clock is 148.5 MHz or 148.35 MHz for 3G, 74.25 MHz or 74.175 MHz for HD and 13.5 MHz for SD. This usually comes from the Rx recovered clock (rx_half_clk_chx) from the SERDES CDR.
rx_full_clk	1	I	This clock is required if 10-bit/27 MHz SD output is enabled (i.e. when the 10-bit mode for SD Rx option is selected). This clock must be frequency-synchronous with rx_clk and should be exactly double the frequency of rx_clk while receiving SD video. The Rx recovered clock from the SERDES (rx_full_clk_chx) can be directly used for this clock.
rx_hd_sdn	1	O	HD or SD status output. This signal indicates the rate that is being received by the IP (a zero value for SD and a one value for HD or 3G). This signal can be used to set the SERDES to receive the right rate and/or command the clock generator to output the appropriate clock.
rx_tg_hdn	1	O	3G or HD status output. This signal indicates the rate that is being received by the IP (a zero value if SD or HD and a one value if 3G). This signal can be used to set the SERDES to receive the right rate and/or command the clock generator to output the appropriate clock.
rx_lb_lan	1	O	3G Level-B or not status output. This signal indicates whether the received video is a 3G Level-B stream or not. This output is one if the received video is 3G Level-B and zero otherwise.
SERDES/Board Tx Interface			
txdata	20	O	Transmit data (parallel) to the SERDES. This data is synchronous with the tx_half_clk or pdi_clk, depending on whether 10-bit mode for SD Tx is enabled or not.
txd_ldr	1	O	Low data rate transmit data. This is the transmit data for the SD rate, serialized in the IP to be connected to the out-of-band transmit path of the SERDES channel. This output is typically connected to txd_ldr_chx of the SERDES.
Common Interface			
rstn	1	I	System-wide asynchronous active-low reset signal. This signal resets all the registers in the IP.
ce	1	I	Optional clock enable signal. A zero input at ce freezes all the switching operations in the IP. It is useful for putting the IP in a power save mode.
FPGA Rx Interface			
pd_out	20	O	Parallel data output. This is the parallel video data output from the receiver. This data is synchronous with the receiver clock rx_clk, if 10-bit mode for SD Rx is disabled. It is synchronous with the pdo_clk if 10 bits mode for SD Rx is enabled.
pdo_clk	1	O	Parallel data output clock. This clock port is available when the 10-bit mode for SD Rx option is selected. This clock is a multiplexed version of rx_clk and rx_full_clk. If this clock is available, the output data as well as output status and control signals are synchronous with this clock.
vid_active	1	O	Video active signal. This output signal is high if the receiver is locked to a valid video stream at the receiver input.
vid_format	2	O	Video format output. The format is identified as follows: 00 – 1440 x 486/576 01 – 1280 x 720 10 – 1920 x 1035 11 – 1920 x 1080 For 3G-b outputs, the video format corresponds to stream 1 video.

Table 2-1. Top-Level I/O Interface (Continued)

Port	Bits	I/O	Description
frame_format	3	O	Frame format output. This output identifies the number of fields and whether the video is interlaced or progressive as follows: 000 – Unknown or custom 001 – 24p or 23.98p or 23.98psF 010 – 25p, 25psF 011 – 30p or 29.97p or 29.97psF 100 – 50i 101 – 60i or 59.94i 110 – 50p 111 – 60p or 59.94p For 3G-b outputs, the frame format corresponds to stream 1 video.
trs_out	1	O	Timing reference sequence output. This output is high during the start of the TRS sequence, i.e., during the time when $3FF_h$ or $FFFFF_h$ is available on pd_out. For 3G-b video, this output is high during the Y-channel $FFFFF_h$ word.
ychannel	1	O	Y-channel indicator. This output is meaningful only when 3G-b video is received. This output is one when Y-channel data is given out at pd_out and zero when C-channel data is given out.
field	1	O	Field number. This is the field number information available in the XYZ word. The field value at this output changes state when the XYZ word appears at the output. For 3G-b video, the field output corresponds to stream 1 video and it changes state when the y-channel XYZ word appears at the output.
vblank	1	O	Vertical blanking signal. The value at this output changes state when the XYZ word appears at the output. For 3G-b video, the vblank output corresponds to stream 1 video and it changes state when the y-channel XYZ word appears at the output.
hblank	1	O	Horizontal blanking signal. The value at this output changes state when the XYZ word appears at the output. For 3G-b video, the hblank output corresponds to stream 1 video and it changes state when the y-channel XYZ word appears at the output.
ln1_out	11	O	Line number output. This provides the line number corresponding to the current parallel data output. This output is not valid for SD video rates. The value at this output changes when LN1 word is given out at pd_out port. When 3G-b video is being received, this output corresponds to stream 1 video and changes state when y-channel LN1 word is given out at pd_out port.
ln2_out	11	O	Line number output for stream 2 video. This output is valid only when 3G-b video is being received. The output changes state when y-channel LN1 word is given out at pd_out port.
eav_error	1	O	EAV error output. This one-cycle pulse indicates that an EAV has been received at an incorrect time instant or that the EAV has not been received when it should have been received.
sav_error	1	O	SAV error output. This one-cycle pulse indicates that a SAV has been received at an incorrect time instant or that the SAV has not been received when it should have been received.
y1_crc_error	1	O	This signal indicates that a CRC error has been detected for the y-channel of the current line. This output is not valid for SD video rates. The CRC error output goes high during the clock cycle when the CRC comparison is made. When 3G-b video is being received, this output denotes the CRC error for the y-channel of stream 1 video.
c1_crc_error	1	O	This signal indicates that a CRC error has been detected for the c-channel of the current line. This output is not valid for SD video rates. The CRC error output goes high during the clock cycle when the CRC comparison is made. When 3G-b video is being received, this output denotes CRC error for the c-channel of stream 1 video.
y2_crc_error	1	O	This signal is valid only when receiving 3G-b video. This output indicates that a CRC error has been detected for the y-channel of the current line of stream 2 video.
c2_crc_error	1	O	This signal is valid only when receiving 3G-b video. This output indicates that a CRC error has been detected for the c-channel of the current line of stream 2 video.
vpid1_out (vpid2_out)	32	O	Video payload identifier output. This output is not valid when receiving SD video. The VPID bytes are organized as follows: {byte4, byte3, byte2, byte1}. When receiving 3G-b video, this output corresponds to the VPID for stream 1. The stream 2 VPID in that case is available at vpid2_out port.

Table 2-1. Top-Level I/O Interface (Continued)

Port	Bits	I/O	Description
vp1_valid (vp2_valid)	1	O	VPID valid output. This output indicates that the VPID received is valid as determined by the ADF, DID and SDID words. When receiving 3G-b video, this output corresponds to stream 1. The stream 2 VPID valid in that case is available at vp2_valid port.
vp1_cserr (vp2_cserr)	1	O	VPID checksum error output. This output denotes a checksum error for the received VPID. When receiving 3G-b video, this output corresponds to stream 1 video. The stream 2 VPID checksum error in that case is available at vp2_cserr port.
vp1_parerr (vp2_parerr)	1	O	VPID parity error output. This output denotes a parity error for the received VPID. When receiving 3G-b video, this output corresponds to stream 1. The stream 2 VPID parity error in that case is available at vp2_parerr port.
vp1_lineok (vp2_lineok)	1	O	VPID line okay output. This output indicates that the VPID was embedded in the correct line number of the received video. VPID needs to be embedded at line 10 for progressive transports and lines 10 and 572 for interlaced transports. When receiving 3G-b video, this output corresponds to stream 1 video. The stream 2 VPID line okay indication in that case is available at vp2_lineok port.
rx_rate	3	I	This input command controls the rates scanned by the receiver. Each bit enables the scanning of one of the rates, as shown below: rx_rate [2]: 0 - disable 3G scan, 1 - enable 3G scan rx_rate [1]: 0 - disable HD scan, 1 - enable HD scan rx_rate [0]: 0 - disable SD scan, 1 - enable SD scan This is an asynchronous control input. The receiver scans only for the rates that are enabled. However, if the scan for one of the rates is disabled when that rate is being received, the reception is not affected.
FPGA Tx Interface			
pd_in	20	I	Parallel data input. This is the parallel video data for transmission. The data is read with pdi_clk. If the 10-bit mode for SD Tx is enabled, only the lower 10 bits of the data are read in when reading SD data.
pdi_clk	1	I	Clock input for the parallel input data. The data at pd_in is read using this clock. This clock should have the same frequency as the transmit reference clock to the SERDES (divided appropriately by 1, 2 and 11 for 3G, HD and SD respectively). In a typical usage, this clock is the same as Tx half clock from the SERDES if 10-bit mode for SD Tx is disabled and a multiplexed version of Tx half clock and Tx full clock if 10-bit mode for SD Tx is enabled.
tx_half_clk	1	I	This additional clock input is required, if the 10-bit mode for SD Tx option is selected. This clock must be frequency-synchronous with pdi_clk and must correspond to the 20-bit data width. The frequency of this clock is 148.5 MHz or 148.35 MHz for 3G, 74.25 MHz or 74.175 MHz for HD and 13.5 for SD. The SERDES tx_half_clk output can be connected to this input, as long as pdi_clk is derived from the same SERDES output clock.
pd_in_sd	10	I	Optional parallel data input for SD. If available, the data on this port is read in with clk27_in.
trs_in	1	I	Timing Reference Sequence identifier for the input video stream. This is a one-clock cycle wide pulse that identifies the TRS instance in the parallel input data. This input is high during the start of the TRS sequence for HD and 3G-a inputs, i.e., during the time when $FFFFF_h$ is presented on pd_in. For 3G-b video, this input is high during the Y-channel $FFFFF_h$ word. The trs_in signal is used for the computation of CRC as well as to determine CRC, LN and VPID insertion instants. This signal is not used for SD or if CRC, LN and VPID insertions are all disabled for HD/3G.
hd_sdn_in	1	I	HD/SD input. This input must be zero to transmit SD video and one for 3G or HD video.
lb_lan_in	1	I	3G Level-B indicator input. This input must be one if the input is a 3G-b video and zero otherwise.
sd8b_mode	1	I	SD 8-bit mode. If this input is high, the incoming data is considered to be 8 bits wide. Only the most significant 8 bits (bits [9:2]) are read from the port. The least significant 2 bits are set to zero for all data except the leading TRS sequence (or ANC identifier). When the most significant 8 bits are 1's, then the least significant 2 bits are made equal to '11'.

Table 2-1. Top-Level I/O Interface (Continued)

Port	Bits	I/O	Description
ln1_in (ln2_in)	11	I	Line number input. This input is read in HD/3G modes only. The line number is read in when ln1_set is high. When transmitting 3G-b video, this input provides the line number for stream 1 video. In that case, ln2_in is used to read the line number for the stream 2 video and ln2_set is used as strobe.
ln1_set (ln2_set)	1	I	Line number set signal. This signal is used as a strobe to read the value at the ln1_in port. The line number must be set during or before LN0 word is applied at the pd_in input. When transmitting 3G-b video, this input serves as a strobe for the line number for stream 1 video. In that case, ln2_set is used to strobe the line number for the stream 2 video.
vpid1_in (vpid2_in)	32	I	Video payload identifier input. This input is not used when transmitting SD video. The VPID bytes are organized in the following order: {byte4, byte3, byte2, byte1}. When transmitting 3G-b video, this input corresponds to the VPID for stream 1. The stream 2 VPID in that case is read from the vpid2_in input port.
clk27_in	1	I	This is the 27 MHz input clock for the optional 10-bit/27 MHz SD Tx interface. This clock must be frequency-synchronous with pdi_clk (exactly double that of pdi_clk) during SD operation, if the parameter LDR path for SD is not selected.
clk270_in	1	I	This is the 270 MHz serial clock used for SD serialization in soft logic. This port is available if the LDR path for SD option is selected and the Include PLL for LDR option is not selected. This clock frequency must be exactly 10 times that of clk27_in.
clk27_out	1	O	SD LDR clock output. This 27 MHz clock is synchronous with clk270_out and is available if Include PLL for LDR is selected. This clock, along with clk270_out is useful for feeding another IP instance.
clk270_out	1	O	High-speed SD LDR clock output. This 270 MHz clock is synchronous with clk27_out and is available if Include PLL for LDR is selected. This clock, along with clk27_out is useful for feeding another IP instance.

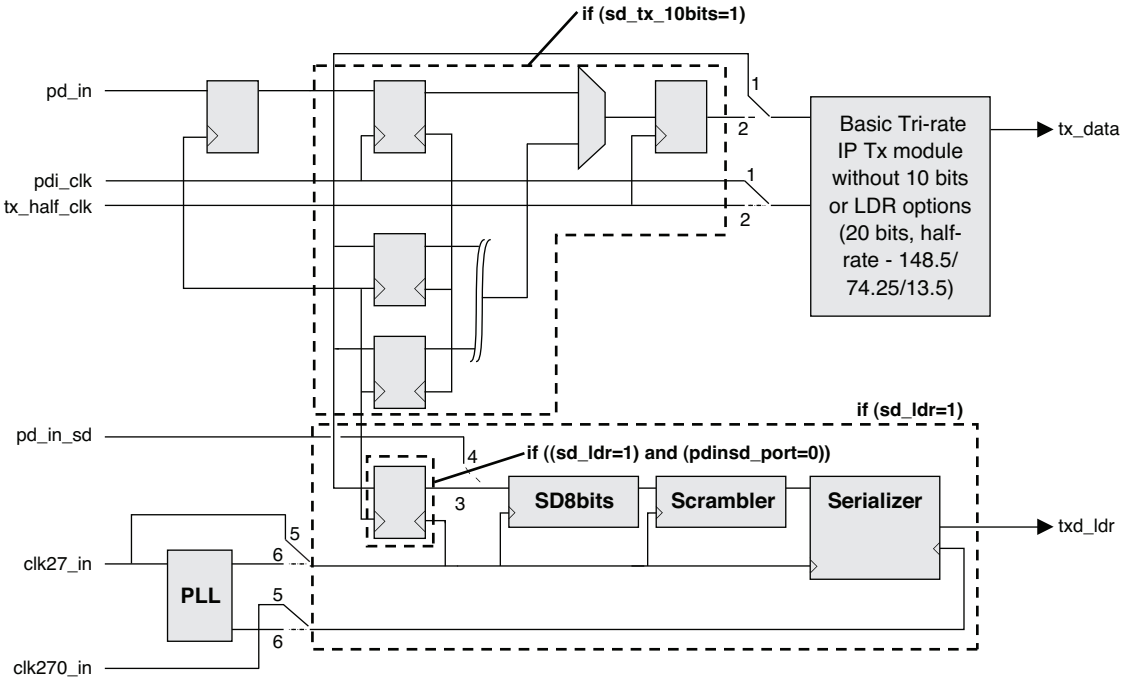
Interfacing with Tri-Rate SDI PHY IP Core

The Tri-Rate SDI PHY IP core is a single-channel transmit/receive PHY and it does not include the SERDES. This section provides some detail on interfacing with the IP, including connecting the IP with the LatticeECP3 SERDES.

SERDES/Board Tx Interface

The encoded and formatted parallel data from the IP core is given out of the 20-bit txdata output port. This directly connects to the SERDES parallel input for serialization. The output from the IP is synchronous with tx_half_clk or pdi_clk, depending on whether 10-bit mode for SD Tx is enabled or not. By deriving the pdi_clk from SERDES' Tx half clock and Tx full clock, the data can be made synchronous with the SERDES Tx PLL clock. The Tx half clock from the SERDES can then be used to drive data into SERDES Tx (for SERDES' txi_clk). Refer to Figure 2-5 for an illustration of how the clocks and data are synchronized for the Tx path.

Figure 2-5. LDR and 10-Bit Data Path for Tx



Notes on switch positions:
If (sd_tx_10bits=1) connection 1 is active, else connection 2 is active.
If (pdinsd_port=0) connection 3 is active, else connection 4 is active.
If (sdpll_exclude=1) connection 5 is active, else connection 6 is active.

SD 10-bit Mode for Tx

The Tri-Rate SDI PHY IP is designed to directly interface with the LatticeECP3 SERDES. Since the width of the SERDES data interface has to be fixed at 20 bits for multi-rate operation, the data transfer frequency is fixed at 13.5 MHz for SD rate. In the simplest configuration, the IP takes in 20 bits of SD data at 13.5 MHz to be consistent with the SERDES interface. However, since most SD video is typically available as 10-bit, 27 MHz data, the IP offers the 10-bit option for the SD interface. The 10-bit SD options are provided separately for Tx and Rx paths. With the 10-bit mode for SD Tx option, SD data is applied at the lower 10 bits of pd_in and the corresponding 27 MHz clock is applied at the pdi_clk input. The clock synchronization used in the IP core for the SD 10 bits and SD LDR options are shown in Figure 2-5.

SD LDR Mode

This is the SD low data rate transmit mode. This mode is used if it is necessary to transmit fractional frame rate HD or 3G video and SD video in different channels of the same SERDES quad. LatticeECP3 SERDES has only one transmit PLL for each quad. This means that the transmit frequencies of different channels in the quad must either be same or one of the permissible divided frequencies. If the SERDES PLL is tuned for 2.97 GHz, the channels can transmit 2.97 Gbps, 1.485 Gbps and 270 Mbps. However, if the PLL is tuned for 2.967 GHz, the channels can only transmit 2.967 Gbps and 1.4835 Gbps. They cannot be used to transmit 270 Mbps. In this scenario, the LDR path is employed for transmitting the SD video. In the LDR scheme, a serializer is built in the soft logic and its output is multiplexed with the SERDES serial output at the driver end of the SERDES. The multiplexer at the output of the SERDES is dynamically controlled by the SERDES input control signals txd_ldr_en_chx.

As shown in Figure 2-5, the parallel data for the LDR serializer can come from either the main input data bus, pd_in or the dedicated 10-bit SD input bus pd_in_sd. If the data is read from the common input bus, the input clock pdi_clk and the LDR clock, clk27_in must be frequency-synchronized during the time SD is transmitted. The 270 MHz bit-rate clock for LDR, clk270_in must be exactly 10 times the frequency of clk27_in.

VPID Extraction

The VPID extraction option enables the extraction of VPID bytes embedded in the horizontal ancillary (HANC) data area of specific lines in the video stream. In addition to the VPID bytes, a few other signals are brought out to indicate a valid VPID, the appropriate lines carrying VPID information, checksum error and parity error.

FPGA Tx Interface

The FPGA side transmit interface consists of the parallel video data to be transmitted, LN/ VPID input data, clocks and rate identification inputs. If SD transmission is not used or if the SD parallel data is available as 20-bit/13.5 MHz data, only one clock (pdi_clk) is required for the entire transmit logic. In that case, the pdi_clk as well as the txi_clk can both be connected to the Tx half clock from the SERDES.

However, if the SD data is available as a 10-bit/27 MHz data stream, the 10-bit mode for SD Tx option needs to be enabled. In this case, the additional tx_full_clk input can be connected to the Tx full clock from the SERDES. The pdi_clk can be a multiplexed version of Tx full clock and Tx half clock from the SERDES. Most of the transmit logic and the data output to SERDES Tx uses tx_half_clk as shown in Figure 2-5.

When the 10-bit mode for SD Tx option is enabled, the 10-bit parallel input for SD video is applied at pd_in_sd. In this case, the SD transmit path is independent and asynchronous with the HD/3G transmit path. The SD data is applied with respect to the clk27_in clock and the entire SD transmit logic operates with this clock. In addition to the 27 MHz clock, another bit-rate clock at 270 MHz (having exactly 10 times the frequency of the 27 MHz clock), is also required for the LDR transmission. If the Include PLL for LDR option is selected, the 270 MHz clock is internally generated within the IP. In this case, both the 27 MHz and the 270 MHz clocks are given out through clk27_out and clk270_out ports.

Custom Format

Valid HD and 3G rates are identified by matching the relative time instants of EAV and SAV timing signals to the possible source format standards in that rate. The IP supports receiving non-standard formats, by accepting custom formats for 3G and HD rates. The custom formats are specified by the time from EAV to SAV and from SAV to EAV. The time can be specified as a fixed value or a range defined by a minimum and a maximum. The custom format for 3G-b is set based on the format of the stream 1HD component that is part of the 3G video.

Advanced Settings

The Advanced Settings tab allows the user to specify the programming time and threshold values. The programming time is specified by a number proportional to the time from which the receiver waits from switching to a new rate and before looking for TRS matches for that rate. Lock match threshold is the number of TRS matches to wait, before locking to a video rate. Unlock error threshold is the number of TRS or timeout errors after which the receiver unlocks to scan for the next rate.

SERDES/Board Rx Interface

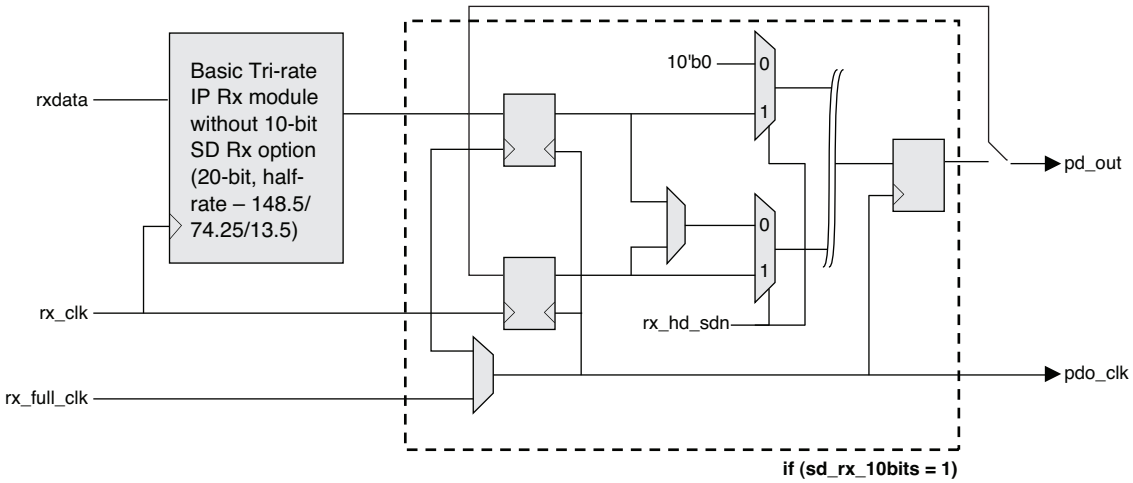
The deserialized parallel output from the SERDES can be directly connected to the rxdata port. The parallel data connection to and from the SERDES is always 20 bits wide irrespective of any SD 10-bit mode set in the IP. The parallel data is read in using rx_clk. If the data comes directly out of the SERDES Rx, then the Rx recovered clock from the SERDES must be connected to the rx_clk input. If the 10-bit mode for SD Rx option is enabled, the IP core needs the 27 MHz recovered clock for the SD data to be applied at the rx_full_clk port.

The output signals, rx_hd_sdn, rx_tg_hdn and rx_lb_lan indicate the rate that the receiver is trying to receive or lock on to. It is important for that these signals be used to promptly change the SERDES divider settings or the frequency of the clock generator that supplies the input clock ports. The outputs rx_hd_sdn and rx_tg_hdn can be used to drive the clock divider controls of the LatticeECP3 SERDES to select one of the three rates (3G, HD and SD) to receive.

FPGA Rx Interface

The FPGA Rx interface includes the parallel output data, output clock, video status/format outputs, video timing signals, LN output, CRC and EAV/SAV error outputs, VPID bytes and VPID status/error outputs. The parallel data output is synchronous with the pdo_clk if 10 bits mode for SD option is enabled and with the rx_clk otherwise. The pdo_clk is derived by multiplexing rx_clk and rx_full_clk using FPGA logic as shown in Figure 2-6.

Figure 2-6. SD 10-Bit Data Path for Rx



The vid_format and frame_format values are determined from the relative EAV/SAV positions in the received data and whether the field value is toggling or not. The y-channel data is always used for format determination. For 3G-b video, the format determination is based on the y-channel data of stream 1 video. The line number output, ln1_out (and ln2_out, if receiving 3G-b video) is the line number contained in the LN0 and LN1 words of the received y-channel data.

If it is not necessary to scan for all the three rates, it is possible to disable the scanning of a particular rate or rates. The 3-bit rx_rate input can be used to independently disable the scanning of a rate or a combination of rates. The scan enable inputs can be dynamically changed. Rate scan disable applies only when the receiver goes on to scan a rate. Therefore, disabling a rate that is being currently received or locked on to will not affect the reception of that rate.

SD 10-Bit Mode for Rx

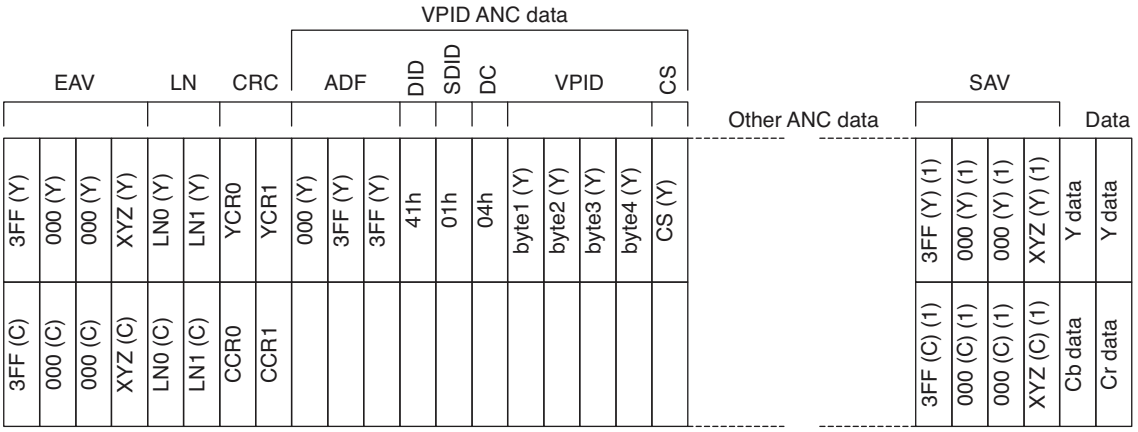
Similar to the 10-bit option for SD Tx, the 10-bit option for SD Rx provides SD data output at 27 MHz and 10 bits. A block diagram of the 10-bit mode is shown in Figure 2-6. The SD output is available at the lower 10 bits of the common pd_out port. If this option is selected, the IP provides an output clock, pdo_clk that is synchronous with the output data. The output clock pdo_clk is the multiplexed version of rx_half_clk and rx_full_clk, the recovered clocks from the SERDES.

Video Payload Identification and Extraction

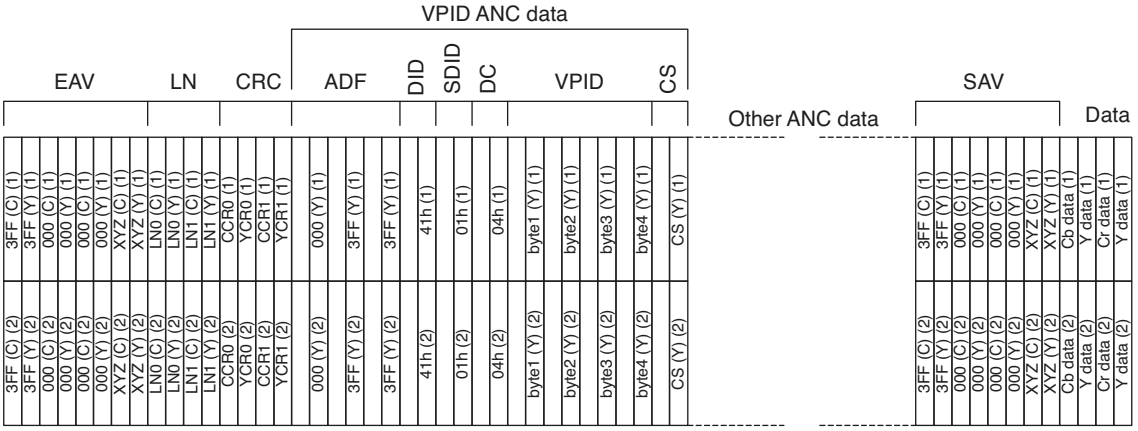
The 4-byte video payload identifier (VPID) added to the ancillary data space of SDI interfaces is defined in the SMPTE 352M standard. The VPID bytes are added as ancillary data and follow the general format of ANC data defined by the SMPTE 291M [12] standard. The VPID is inserted in the y-channel (for 3G-b, in the y-channel of both stream 1 and stream 2 videos) on particular video lines depending on the video format. Figure 2-7 shows the organization of VPID bytes in the SDI formatted data.

Figure 2-7. Format and Structure of Video Payload Identifier

HD stream, 20 bits at 74.25 MHz or 3G Level-A stream, 20 bits at 148.5 MHz



3G Level-B stream, 20 bits at 148.5 MHz



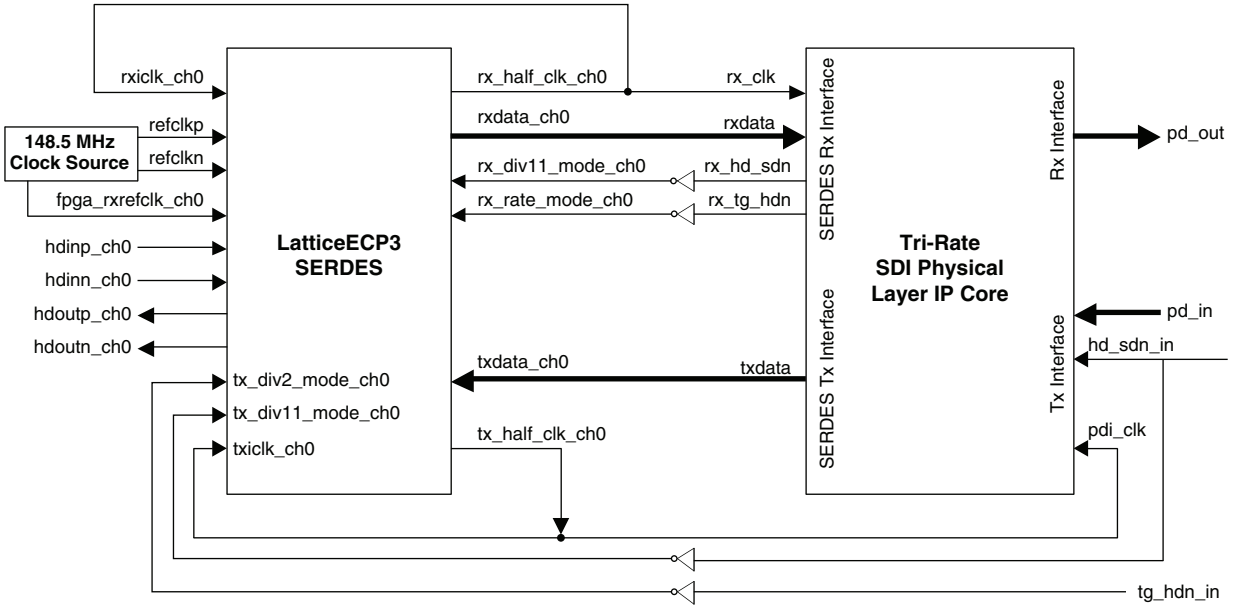
The VPID bytes, byte1, byte2, byte3 and byte4 are combined into one 32-bit word as {byte4, byte3, byte2, byte1} for input/output purposes. Thus vpid1_in, vpid2_in, vpid1_out and vpid2_out follow the same byte organization format given above. The line number for VPID insertion is determined by counting the line numbers from field transitions and using the video format from the input VPID bytes.

On the receive side, the VPID bytes are extracted, if present, and given out through vpid1_out port (and vpid2_out port, if 3G-b video is received). If the ANC data packet is recognized as a VPID ANC packet based on DID and SDID matches, then vp1_valid is asserted high. If a valid VPID is available at the expected line numbers, vp1_lineok is asserted. If VPID is valid, then vp1_cserr and vp1_parerr indicate the occurrence of checksum and parity errors respectively. When receiving 3G-b video, the status and error signals for stream 2 video are given out through vp2_valid, vp2_lineok, vp2_cserr and vp2_parerr ports.

Integer Frame-Rate Applications

Figure 2-8 shows a typical IP configuration and its connection with the SERDES for integer frame rate transmission applications. The figure does not list all the signals and connections, only the essential ones. In this configuration, the SERDES is configured to use REFCLK for transmit reference clock and FPGA fabric clock for the receive reference clock. Only one clock source, 148.5 MHz, is required for the transmission and reception of all the three SDI rates. Multi-rate compatibility is achieved using the built-in clock dividers and multiplexers in the SERDES.

Figure 2-8. Tri-Rate IP Usage for Integer Frame Rate Applications

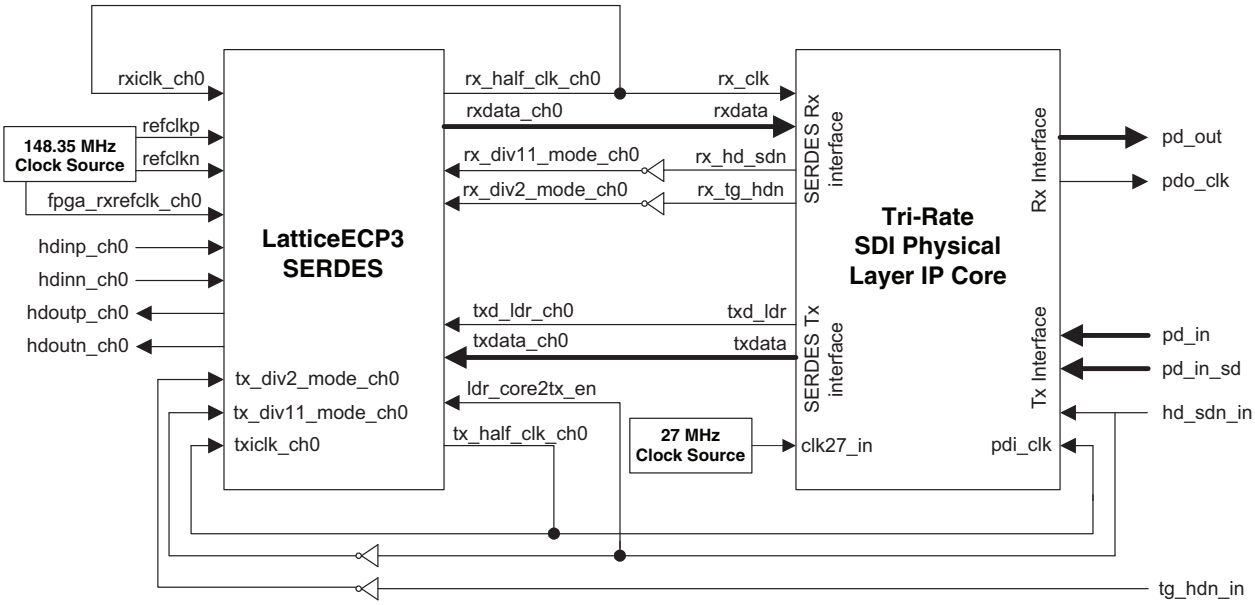


As shown above, one 148.5 MHz clock source is sufficient for multi-rate transmission/reception as long as fractional frame rate HD/3G transmission is not required.

Fractional Frame-Rate Applications

In order to transmit fractional frame-rate HD or 3G simultaneously with SD transmission in the same SERDES quad, the low data rate (LDR) transmit path in the SERDES needs to be employed for SD transmission. Figure 2-9 shows this application scenario. As shown in the figure, a 27 MHz clock is required for this configuration in addition to the 148.35 MHz fractional frame rate reference clock. The control ldr_core2tx_en is driven by hd_sdn_in to switch the SERDES output between the SERDES serializer and the LDR data from the IP core.

Figure 2-9. Tri-Rate IP Usage for Fractional Frame Rate Applications



Two sample designs provided with the IP core can be used to implement a complete SDI transmit/receive system on the LatticeECP3 Video Protocol Board. The designs are available in the user's IP project directory after the Tri-Rate SDI PHY IP is generated. A detailed explanation of the sample designs and their usage is provided in the Tri-Rate SDI PHY IP Loopback and Passthrough Sample Designs User's Guide available in the IP project directory.

Timing Specifications

The timing for the Tx data and controls for HD/3G-a is given in Figure 2-10. The Tx timing for 3G-b is shown in Figure 2-11.

Figure 2-10. Tx Data and Controls for HD/3G-a

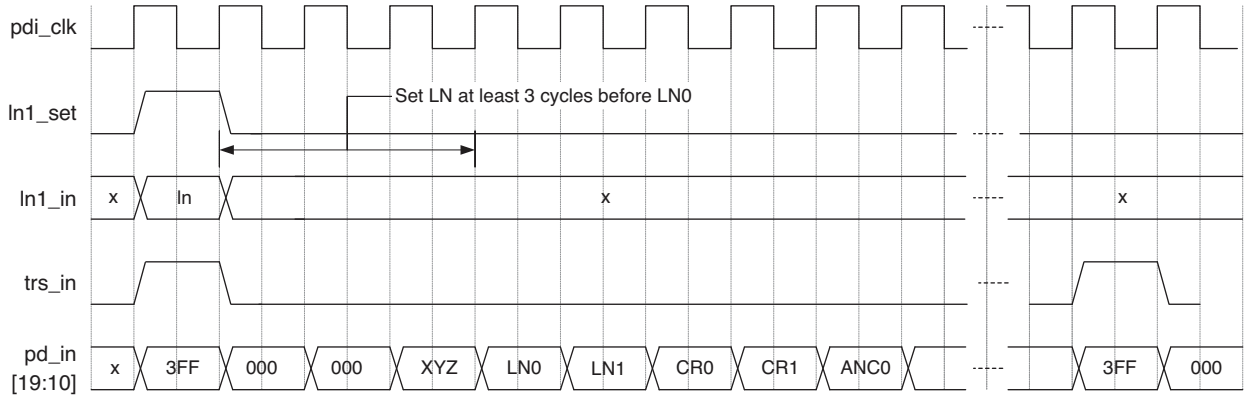
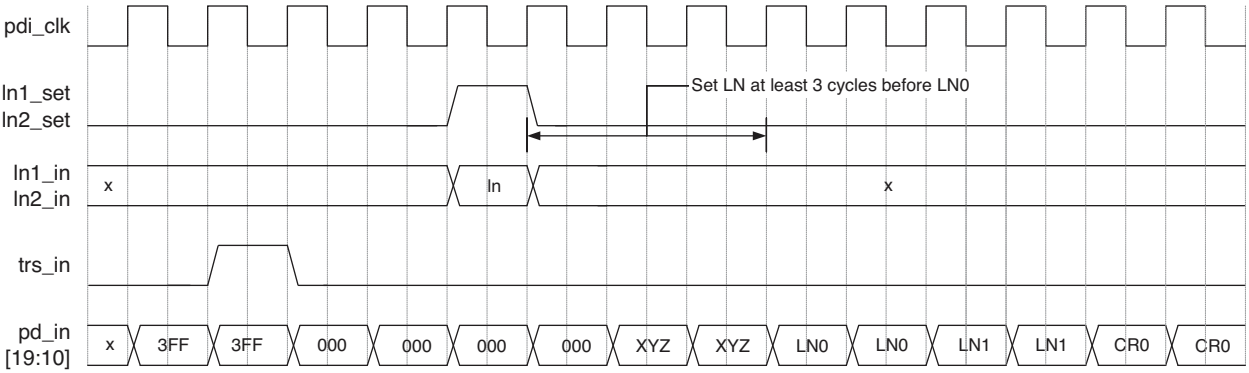


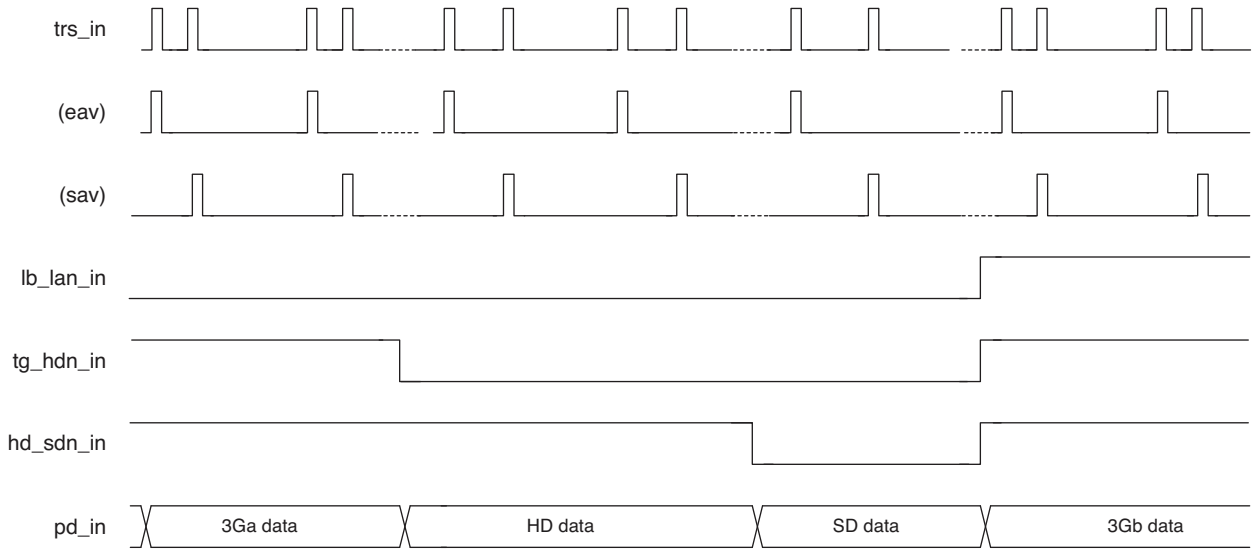
Figure 2-11. Tx Data and Controls for 3G-b



For SD transmission, the trs_in signal is not used. For HD and 3G-a inputs, trs_in must coincide with the "3FF" data as shown in Figure 2-10. However, for 3G-b inputs, the trs_in should go high when the y-channel "3FF" (or the second "3FF") occurs in the stream as shown in Figure 2-11. The line number for both cases must be set at least three cycles before the LN0 word is given at pd_in.

Figure 2-12 shows the timing for the rate-select control signals for different transmit rates.

Figure 2-12. Rate-select Control Signals for Different Transmit Rates



The timing diagram for the Rx side data and status signals for HD/3G-a is shown in Figure 2-13 and that for 3G-b is shown in Figure 2-14. The timing for the multi-rate receive operation is shown in Figure 2-15.

Figure 2-13. Rx Data and Status Signals for HD/3G-a

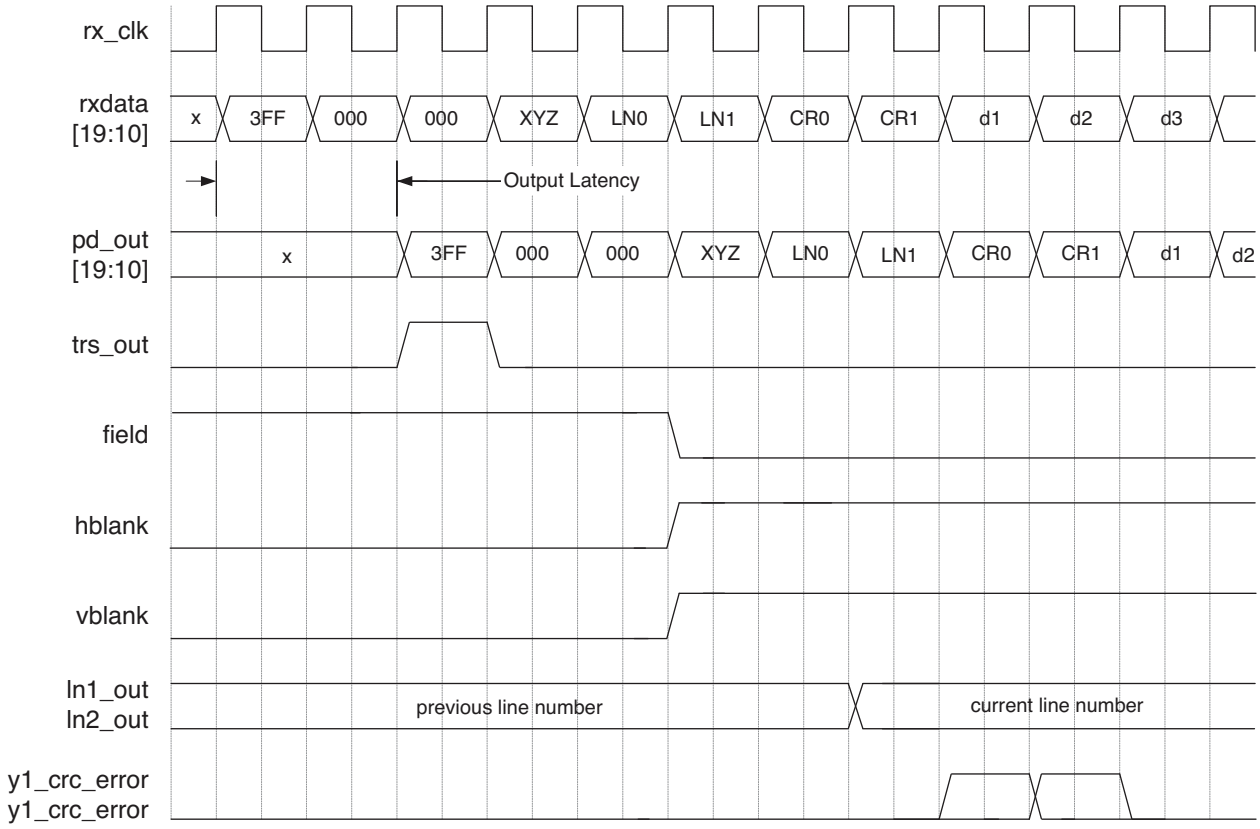


Figure 2-14. Rx Data and Status Signals for 3G-b

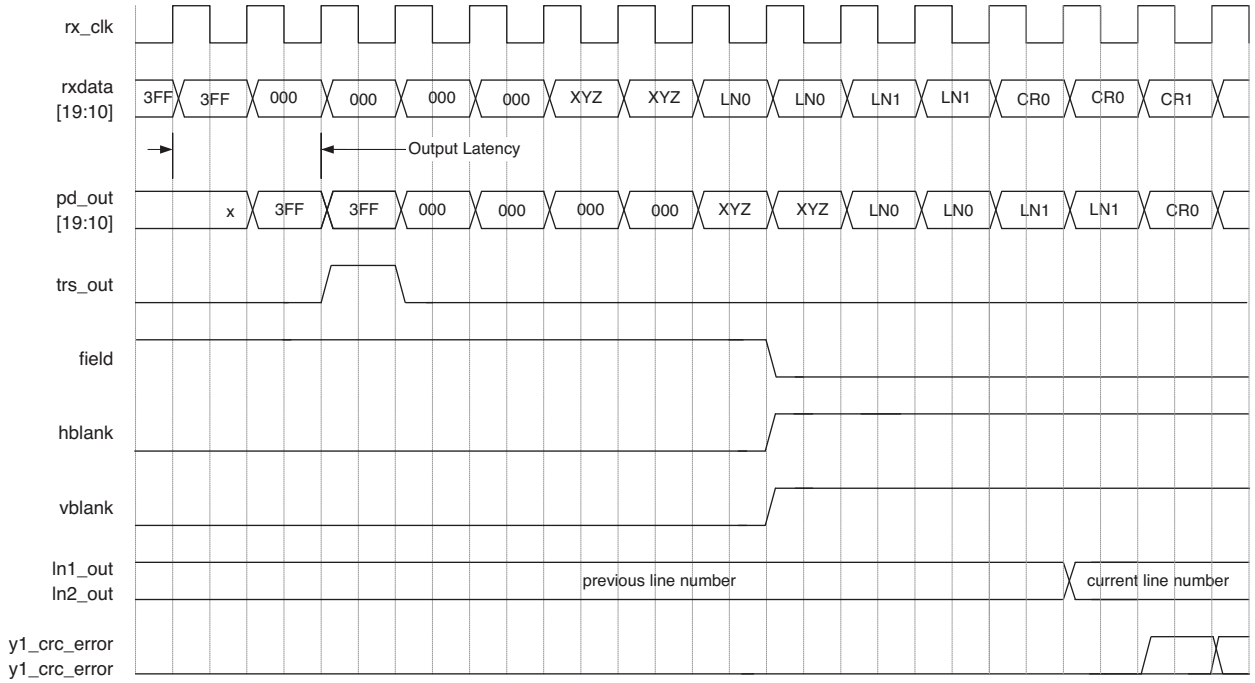


Figure 2-15. Control Signals for Rx-Side Rate Variations