Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

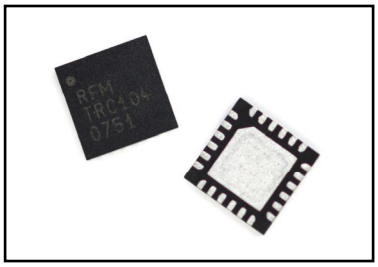
Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

RFM products are now Murata products.

TRC104

2.4 GHz RF Transceiver



Product Overview

TRC104 is a single chip, multi-channel, low power RF transceiver. It is an ideal fit for low cost, high volume, two-way short range wireless applications operating in the worldwide unlicensed 2.4 GHz ISM band. The TRC104 is FCC & ETSI certifiable. All critical RF and base-band functions are integrated in the TRC104, minimizing external component count and simplifying design-in. Only a microcontroller, crystal and several passive components are needed to create a complete, robust radio function. The TRC104 includes a set of low-power states to reduce overall current consumption and extend battery life. The small size and low power requirements of the TRC104 make it ideal for a wide variety of short range radio applications. The TRC104 complies with Directive 2002/95/EC (RoHS).

Key Features

- Modulation: GFSK with frequency hopping spread spectrum capability
- Frequency range: 2401-2527 MHz
- 127 Channels
- High sensitivity: -95 dBm @ 250 kb/s
- High data rate: Up to 1 Mb/s
- Low current consumption -
  - Receive current: 18 mA
  - Transmit current: 13 mA @ 0 dBm
- Up to 1 mW transmit power
- Wide operating supply voltage: 1.9 to 3.6 V
- Low sleep current: 0.4 µA
- Integrated PLL, IF and base-band circuitry
- Integrated data & clock recovery
- Programmable RF output power
- 32-byte Transmit/receive FIFO
- Programmable TX/RX FIFO depth
- Continuous & protocol modes
- Packet destination and sender addressing
- Packet handling features -
  - Packet address filtering
  - Error detection
- SPI configuration & data interface
- TTL/CMOS compatible I/O pins
- Low-cost crystal reference
- Integrated RSSI
- Integrated crystal oscillator
- Host microcontroller interrupt outputs
- Programmable data rate
- Integrated 16-bit packet CRC
- Integrated DC-balanced data scrambling
- Integrated voltage regulators
- Four power-saving operating states
- Very low external component count
- Small plastic package: 24-pin QFN
- Standard 13 inch reel, 3K pieces

Applications

- Wireless keyboards
- Wireless mice
- Wireless game controllers
- Wireless headsets
- Wireless Toys
- Active RFID tags
- Security systems
- Two-way remote keyless entry
- Automobile immobilizers
- Sports and performance monitoring
- Low power two-way telemetry systems
- Wireless modules

Table of Contents

1 Pin Configuration

TRC104 Pin Out - View Through Top

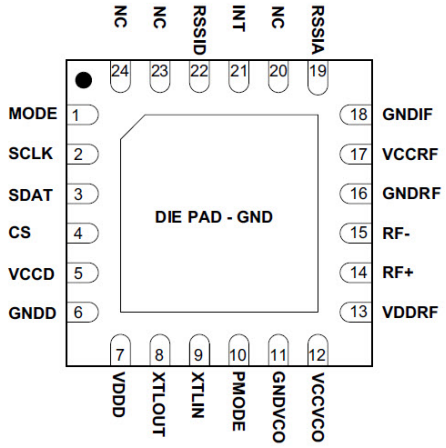


Figure 1

1.1 Pin Description

PIN	TYPE	NAME	DESCRIPTION
1	I	MODE	Operating mode select input - used with PMODE and CS
2	I/O	SCLK	Serial clock input for burst mode, serial data output for continuous mode, and SPI/FIFO clock signal
3	I/O	SDAT	Serial data input/output for SPI mode and TX/RX active mode
4	I	CS	SPI serial interface select, active high
5		VCCD	External digital power input, 3.0 V typical
6		GNDD	Digital ground
7		VDDD	Regulated digital output voltage
8	O	XTLOUT	Crystal oscillator output
9	I	XTLIN	Crystal oscillator input
10	I	PMODE	Power mode select input - used with MODE to select standby or sleep mode
11		GNDVCO	VCO ground pin
12		VCCVCO	External VCO power input , 3.0 V typical
13		VDDRF	Regulated supply output for RF power amplifier
14	RFIO	RF+	Differential RF I/O pin
15	RFIO	RF-	Differential RF I/O pin
16		GNDRF	RF ground
17		VCCRF	External RF power input, 3.0 V typical
18		GNDIF	IF ground
19	O	RSSIA	Analog RSSI output - continuous mode only
20		NC	No connection - not used
21	O	INT	Transmit or receive complete interrupt output
22	O	RSSID	RSSI threshold interrupt output
23		NC	No connection - not used
24		NC	No connection - not used
P	-	DIE PAD	IC die pad on bottom of package - ground

Table 1

2 Electrical Characteristics

Absolute Maximum Ratings

SYMBOL	PARAMETER	NOTES	MIN	MAX	UNITS
Vcc	Supply Voltage		-0.4	+3.6	V
T_{STG}	Storage Temperature		-55	+125	°C
RF_{IN}	RF Input Level			0	dBm

Table 2

Recommended Operating Range

SYMBOL	PARAMETER	NOTES	MIN	MAX	UNITS
Vcc	Supply Voltage		+1.9	+3.6	V
T_{OP}	Operating Temperature		-40	+85	°C

Table 3

2.1 DC Electrical Characteristics

Minimum/maximum values are valid over the recommended operating range Vcc = 1.9-3.6 V. Typical conditions: T_O = 25°C; V_{CC} = 3.3 V. The electrical specifications given below are valid when using a Murata XTL1021 or equivalent crystal.

PARAMETER	SYM	NOTES	MIN	TYP	MAX	UNITS	Test Conditions
Sleep Mode Current	I_{SL}			0.4		µA	
Stop Mode Current	I_{ST}			1.4		µA	
Standby Mode Current	I_{SB}	crystal oscillator running		22		µA	16 MHz crystal
Configuration Mode Current	I_{CM}	crystal oscillator running		15		mA	
Receiver Mode Current	I_{RX}	250 kb/s		18		mA	
		1 Mb/s		19			
Transmitter Mode Current	I_{TX}	Pout = 0 dBm		13		mA	
		Pout = -10 dBm		9			
RSSI Analog Output Level			500		1500	mV	
Digital Input Low Level	V_{IL}		-0.4		0.8	V	
Digital Input High Level	V_{IH}		0.7*Vcc		Vcc+0.4	V	
Digital Input Current Low	I_{IL}			1		µA	V_{IL} = 0 V
Digital Input Current High	I_{IH}			1		µA	V_{IH} = Vcc
Digital Output Low Level	V_{OL}		-		0.4	V	I_{OL} = -1 mA
Digital Output High Level	V_{OH}		Vcc-0.4		-	V	I_{OH} = +1 mA

Table 4

2.2 AC Electrical Characteristics

Minimum/maximum values are valid over the recommended operating range Vcc = 1.9-3.6 V. Typical conditions: T_O = 25°C; V_{CC} = 3.3 V. The electrical specifications given below are valid when using a Murata XTL1021 or equivalent crystal.

RECEIVER							
PARAMETER	**SYM**	**NOTES**	**MIN**	**TYP**	**MAX**	**UNITS**	**Test Conditions**
RF Input Impedance				200		ohms	differential
RF Input Power					0	dBm	
Receiver Bandwidth				1.5		MHz	
Receiver Sensitivity		250 kb/s		-95		dBm	10^{-3} BER
		1 Mb/s		-90			10^{-3} BER
Blocking Immunity		250 kb/s		9		dB	1 MHz offset, unmodulated
		1 Mb/s		5			
Co-channel Rejection		250 kb/s		-20		dB	
		1 Mb/s		1			
Image Rejection		250 kb/s		-26		dB	
		1 Mb/s		-26			
FSK Bit Rate			250		1000	kb/s	NRZ
RSSI Accuracy		4-bit value		±3		dB	
RSSI Dynamic Range				40		dB	

Table 5

TRANSMITTER							
PARAMETER	**SYM**	**NOTES**	**MIN**	**TYP**	**MAX**	**UNITS**	**Test Condition**
RF Output Impedance				200		ohms	differential
RF Output Power				0		dBm	
RF Output Power Range			-20		0	dBm	programmable
2nd Adjacent Channel Power		2 MHz channel offset		-20		dBm	1 Mb/s data rate, 0 dBm TX power
3rd Adjacent Channel Power		3 MHz channel offset		-40		dBm	1 Mb/s data rate, 0 dBm TX power
2nd Harmonic				-54		dBm	0 dBm TX power
3rd Harmonic				-46		dBm	0 dBm TX power
FSK Deviation				±160		kHz	fixed for both data rates
20 dB Modulation BW				1		MHz	

Table 6

TIMING							
PARAMETER	**SYM**	**NOTES**	**MIN**	**TYP**	**MAX**	**UNITS**	**Test Condition**
TX to RX Switch Time		oscillator & PLL running		200		µs	
RX to TX Switch Time		oscillator & PLL running		200		µs	
Sleep to Receive		serial command to RX bit			120	ms	
Sleep to Transmit		serial command to TX bit			120	ms	
Sleep to Stop Mode					120	ms	
Stop to Standby Mode					1.5	ms	
Standby to Receive		oscillator running		200		µs	
Standby to Transmit		oscillator running		200		µs	
Frequency Hop Time		channel switching time		200		µs	
Transmit Rise/Fall Time				10/5		µs/step	programmable
RSSI Rise Time				10		mV/µs	no external filter capacitor

Table 7

PLL CHARACTERISTICS							
PARAMETER	**SYM**	**NOTES**	**MIN**	**TYP**	**MAX**	**UNITS**	**Test Condition**
Crystal Oscillator Frequency			4	16	20	MHz	
PLL Lock Time		settling to less than 10 kHz		170		µs	
PLL Step Resolution				1		MHz	
Crystal Load Capacitance				12		pF	
Crystal Oscillator Start time				1.5		ms	from sleep mode
Frequency Range			2401		2527	MHz	

Table 8

3 Architecture

The TRC104 is a single-chip FSK transceiver that operates in the worldwide 2.4 GHz ISM band. The TRC104's highly integrated architecture requires a minimum of external components. Advanced features including the TX/RX FIFO and the burst packet data mode significantly reduce the TRC104's load on the host microcontroller. As shown in Figure 2, the TRC104 utilizes a dual-conversion superheterodyne receiver architecture with an image-reject second mixer. The VCO operates directly at the output frequency when transmitting, and is modulated by a Gaussian-filtered bit stream.

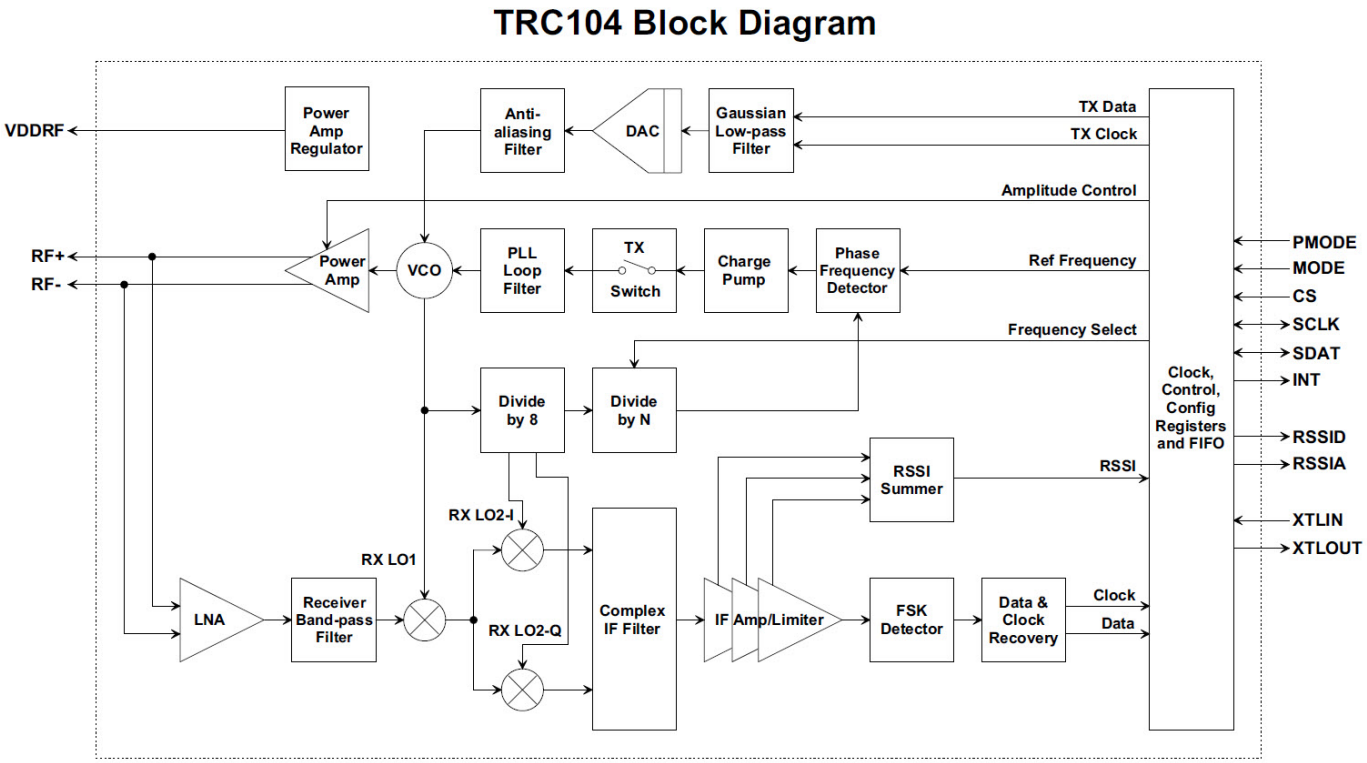


Figure 2

3.1 RF Port

The TRC104 has a differential RF port that is capable of delivering the required transmitter output power at low supply voltages. The differential RF port also provides common mode signal rejection to enhance receiver interference immunity. A simple L-C balun can be used to convert the differential port to a single-ended output to drive an unbalanced antenna, as shown in Figure 3.

3.2 Transmitter Power Amplifier

The power amplifier controls the output power level of the transmitter. The power amplifier has four programmable power levels. The power level is set by the **PWR** bits in configuration register 0x01.

TRC104 Application Circuit

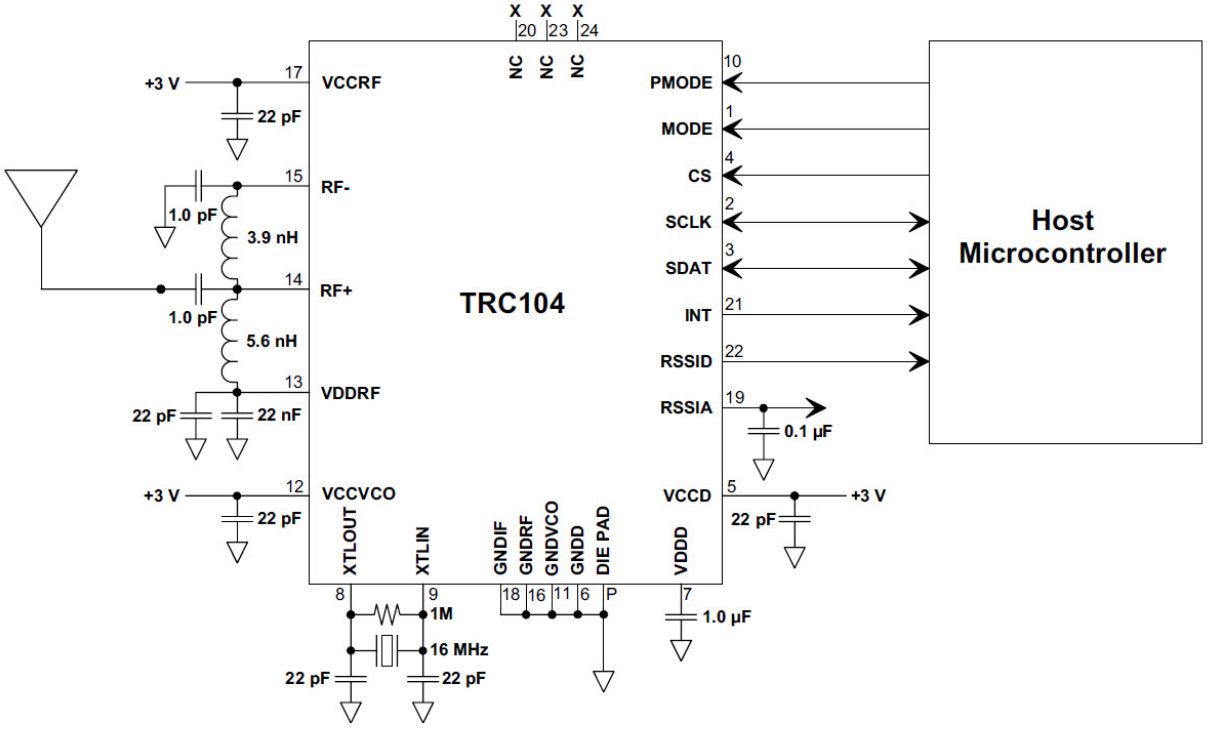


Figure 3

For Burst Transmit Mode, the TRC104 RF output ramp-up and ramp-down times are configurable, controlling excessive transmitter bandwidth due to fast rise and fall times of the transmitter RF envelope. After the PLL is locked for transmission, the power amplifier is ramped up stage by stage beginning with the lowest power level until the power level that is specified by the **PWR** bits in register 0x01 is reached. Once the transmission is complete, the power amplifier is ramped down stage-by-stage until it is completely disabled.

The ramp-up/ramp-down function increases or decreases the output power stage-by-stage as specified by the **PA_RU** and **PA_RD** bits of register 0x07, respectively. Figure 4 shows the timing for the ramp-up/ramp-down.

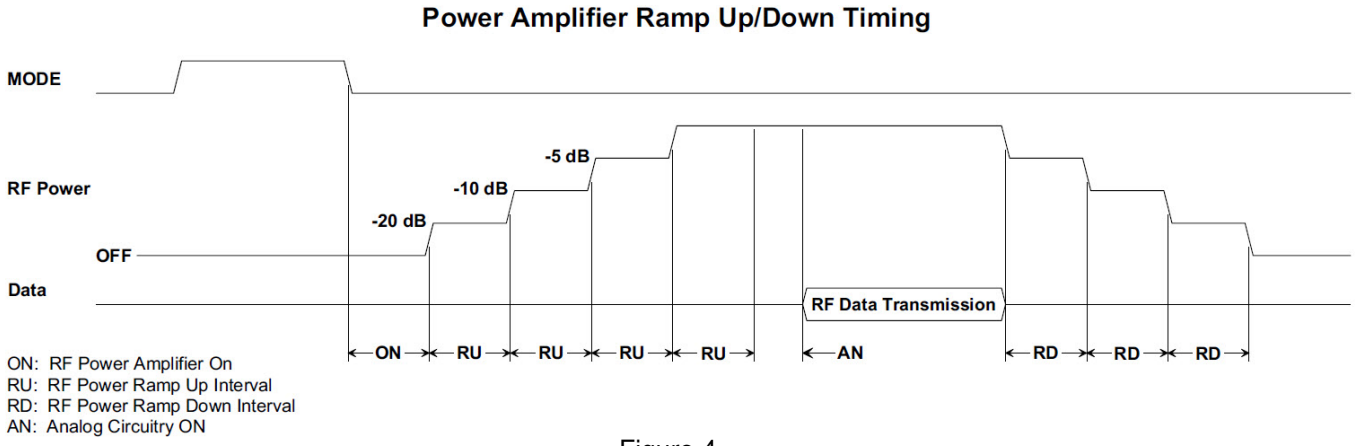


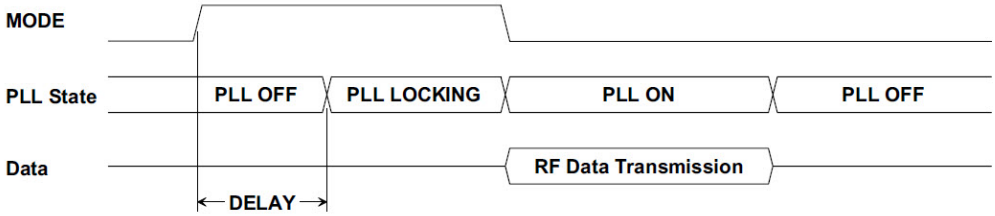
Figure 4

3.3 PLL

The PLL channel is set with the **Ch_Num** bits in configuration register 0x00. In transmit mode, the PLL is normally turned on with the falling edge of the MODE input. The TRC104 transmits the data after the PLL locks and the power amplifier has ramped up to its programmed level. PLL lock time is typically 170 µs. It is possible to enable and lock the PLL before the falling edge of MODE input. This can provides a shorter transition time to transmit.

The PLL pre-start delay time is adjustable from 20 µs up to 5 ms. The value of **PLL_ON** in register 0x14 sets this time. The pre-start delay timer is triggered on the rising edge of MODE as shown in Figure 5. The value of **PLL_ON** determines the delay time from the rising edge of MODE before the PLL is enabled. Care must be taken to carefully calculate the write time of the data packet into the transmit FIFO so that the TRC104 does not enable the transmitter and begin sending data before the data packet is fully written to the FIFO, in which case the TRC104 will discard the current packet.

PLL Pre-start Timing



DELAY: Pre-start delay interval

Figure 5

3.4 Crystal Oscillator

At the 1 Mb/s RF data rate, the TRC104 uses a 16 MHz crystal. At the 250 kb/s RF data rate, the TRC104 can use any one of five standard crystal frequencies: 4, 8, 12, 16, or 20 MHz. The crystal frequency is configured by setting the **FXTAL** bits in register 0x01. At the 250 kb/s data rate, the TRC104's power consumption is reduced by using one of the lower crystal frequencies. The total load capacitance C_L seen between the XTLIN and XTLOUT terminals is composed primarily of C_{IN} and C_{OUT} in series, as shown if Figure 6:

$C_L = 1/((1/C_{IN}) + (1/C_{OUT})) + C_{STRAY}$, where C_{STRAY} is the capacitance associated with the PCB layout

TRC104 Crystal Oscillator Implementation

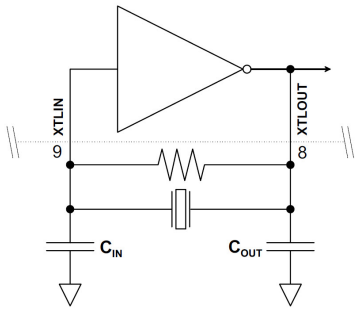


Figure 6

A typical value for C_{STRAY} is 1 pF. The values of C_{IN} and C_{OUT} should be approximately equal and chosen so that C_L matches the load capacitance specified for the crystal. A typical C_L value for a 16 MHz crystal is 12 pF. The

maximum recommended value for C_L is 20 pF. The required crystal frequency tolerance for the TRC104 is ±30 ppm maximum including temperature and aging drift. A typical ESR for the crystal is 35 ohms, and the maximum static capacitance is 7 pF. Murata recommends the 16 MHz XTL1021 for use with the TRC104.

3.5 On-chip Regulators

The TRC104 has on-chip regulators used to power the VCO, the digital circuitry, and for biasing of the RF port. Power pins with a VCC designation are external power inputs to the on-chip regulators. Power pins with a VDD designation are regulated power outputs that are filtered by external capacitors or are used to power external TRC104 functions.

3.6 Receiver

As shown in Figure 2, the TRC104 receiver chain starts with a 2.4 GHz differential input LNA, followed by an on-chip 2.4 GHz band-pass filter. The output of the band-pass filter drives the first mixer, which converts the RF input to the first IF frequency. The output of the first mixer is applied to the second-conversion I and Q mixers, which are driven by I and Q LO signals 1/8 the frequency of the first LO. The outputs of the I and Q mixers are processed by a 5 MHz complex IF filter, which provides both band-pass filtering and Hilbert transform phasing between the I and Q channels. The phased I and Q channels are summed, nulling the unwanted image response.

The output from the complex IF filter is applied to a limiting IF amplifier, which also generates inter-stage outputs that drive the RSSI signal summer. The limited output from the IF amplifier drives an FSK detector. The FSK detector output is applied to a data slicer and then a data and clock recovery circuit. The recovered data and clock signals are processed by the TRC104 control logic according to the receiver mode of operation.

3.7 RSSI

The RSSI signal is an indication of received signal strength. A diagram of the RSSI implementation is shown in Figure 7. Once the RSSI signal is enabled by setting the **RSSIA_rfsh** bit of register 0x03 to 1, the TRC104 will begin to detect the strength of incoming signals. The RSSIA pin outputs an analog voltage corresponding to the strength of the received signal. Once the RSSI sample is complete, the **RSSIA_rfsh** bit resets to 0. Any reading of the RSSIA pin or RSSID pin should be taken after the **RSSIA_rfsh** bit resets to 0.

TRC104 RSSI Implementation

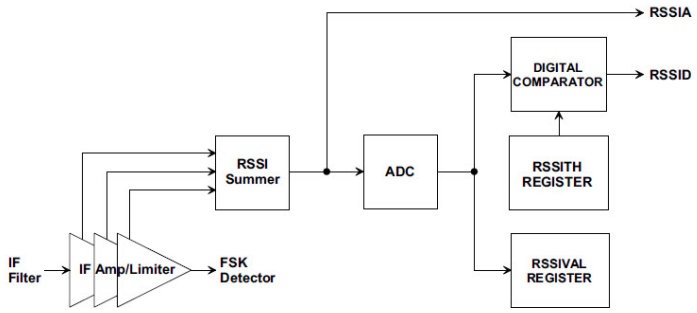


Figure 7

The analog RSSI signal is applied to an ADC to obtain a digital RSSI value, RSSID. The digital value is stored in the **RSSI_val** of register 0x04. The RSSI covers two ranges of signal strength, based on the state of the **RSSI_G** bit in configuration register 0x04. If **RSS_G** is 0, the RSSI covers the received signal strength range of -95 to

-42 dBm. If **RSS_G** is 1, the RSSI covers the received signal strength range of -55 to -2 dBm. The RSSID value is also compared to the **RSSI_thr** threshold value of register 0x03.

If the digital value is greater than the threshold value, the RSSID pin is asserted according to the configuration of the **LVLDRSSI** bit of register 0x17. If the **LVLDRSSI** bit is set to 1, the RSSID pin is asserted high, otherwise the pin is asserted low. The output state of the RSSID pin is disabled while MODE is asserted. The RSSI function is only available in continuous mode, as discussed below.

4 Operating Modes

The TRC104 can operate in one of five modes: Sleep, Stop, Stand-by, Configuration or Active TX/RX. Figure 8 details the state transitions between the operating modes.

TRC104 Operating Mode State Diagram

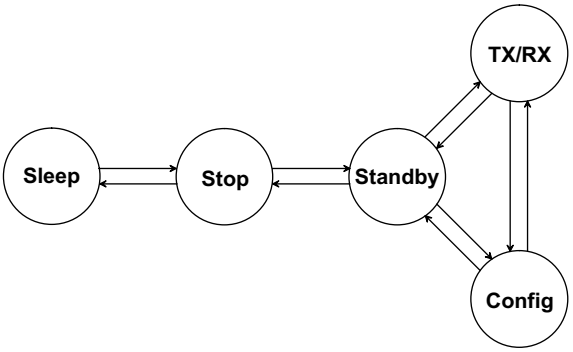


Figure 8

There are three input pins that determine the operating mode for the TRC104. The states of these pins are shown in Table 9 and associated timing diagrams are provided in the Sections below where needed.

Operating Mode	Pin State		
	PMODE	CS	MODE
Sleep Mode	0	**X**	1
Stop Mode	0	0	0
Standby Mode	1	0	0
Configuration Mode	1	1	0
Transmit Load/Receive Mode	1	0	1
Burst Transmit	1	0	1 → 0

X – Don't Care

Table 9

4.1 Sleep Mode

Sleep Mode provides the lowest TRC104 current consumption, typically less than 0.4 µA. No serial transactions can occur while in Sleep Mode. The contents of the FIFO and the internal configuration registers are not maintained in Sleep Mode. When waking from Sleep Mode the TRC104 executes a power-up reset, which takes 120 ms. Any operation to the TRC104 must wait until the reset period is complete. Following a sleep cycle, configuration registers must be rewritten to utilize operating parameters other than the power on default settings. Figure 9 demonstrates the states of the mode control pins and the timing related to Sleep Mode. For minimum current consumption, hold the SDAT, SCLK, INT and RSSID pins low in this mode. 100K pull-down resistors can be used for this purpose.

Sleep Mode Configuraton Timing

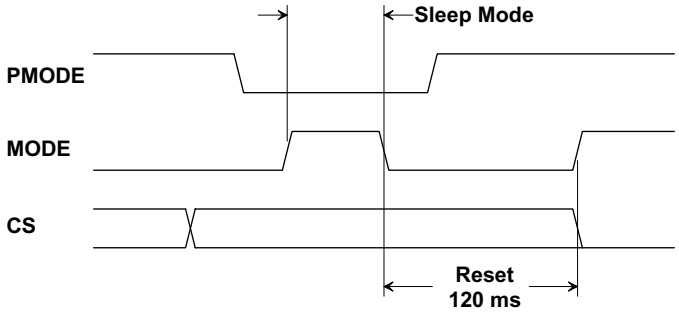


Figure 9

4.2 Stop Mode

In Stop Mode the contents of the TRC104 configuration registers are maintained, and the digital voltage regulator and parts of the digital circuitry are enabled. The remaining digital and analog circuitry is disabled to minimize current consumption, which is typically 1.4 µA. No serial transaction can occur in Stop Mode. The typical turn-on time from Stop Mode is 1.5 ms. Any operation to the TRC104 must wait until the turn on period is complete. Figure 10 demonstrates the states of the mode control pins and the timing related to Stop Mode.

Stop Mode Configuraton Timing

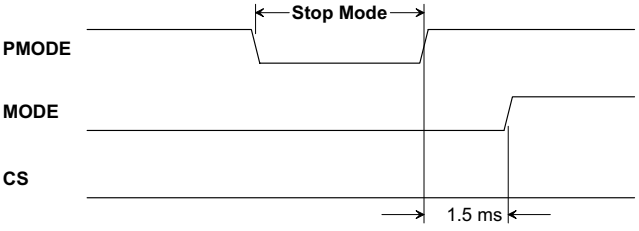


Figure 10

4.3 Standby Mode

Stand-by Mode is a low current mode that provides a very low transition time to configuration, transmit or receive modes. In Standby Mode circuit blocks that are not being utilized are shutdown to minimize current usage. When the TRC104 is set to Transmit, Receive or Configuration Mode, there is no start-up delay and the next action may occur immediately. The power consumption of Standby Mode is dictated mainly by the crystal frequency used.

4.4 Configuration Mode

Configuration Mode allows access to the TRC104's configuration registers. Serial data is applied to the SDAT pin and serial clock is applied to the SCLK pin. See Section 5 for additional details.

4.5 Transmit/Receive Mode

This mode is enabled to load the transmit FIFO or receive data. The mode function, transmit or receive, is set before enabling this mode. The mode function is selected by the **C_Mode** bit in configuration register 0x00. See Section 5 for descriptions and timing of the various data transfer modes.

5 Data Transfer Modes

The TRC104 supports two data transfer modes - Continuous Data Mode and Burst Data Mode. The data transfer mode is selected by the **D_Mode** bit in configuration register 0x02.

5.1 Continuous Data Mode

Continuous Data Mode is selected when the **D_Mode** bit of register 0x02 is set to 0. Continuous Receive Mode routes demodulated data directly to the SDAT pin and the associated clock to the SCLK pin. In Continuous transmit mode the data bit stream is applied directly to the SDAT pin. The internal FIFOs and the automatic packet features are disabled in Continuous Data Mode. It is the responsibility of the TRC104 host microcontroller to handle these functions.

5.1.1 Continuous Transmit Mode

Continuous Transmit Mode is enabled when the **C_Mode** bit of register 0x00 is set to 1 and the **D_Mode** bit of register 0x02 is set to 0. In Continuous Transmit Mode, the transmit FIFO and all automatic packet features including preamble generation, addressing, DC-balanced data scrambling and CRC generation are disabled. The TRC104 host microcontroller must handle these functions for Continuous Transmit Mode. Specifically, the host microcontroller *must* generate a 1-0-1-0 … preamble sequence of at least 16 bits followed immediately by the destination address for the transmission (called the sender or local device address at the destination node).

Also for this mode, it is the responsibility of the host microcontroller to maintain correct bit timing to an accuracy of 1% as there is no bit clock output for transmit timing. The host microcontroller must be powerful enough to accurately support the selected serial data rate (250 kb/s or 1 Mb/s) in addition to other functions required for the end application. Figure 11and Table 10 show the timing for transmitting data on SDAT. Note that three 1 dummy bits must be sent prior to sending the preamble and the rest of the packet.

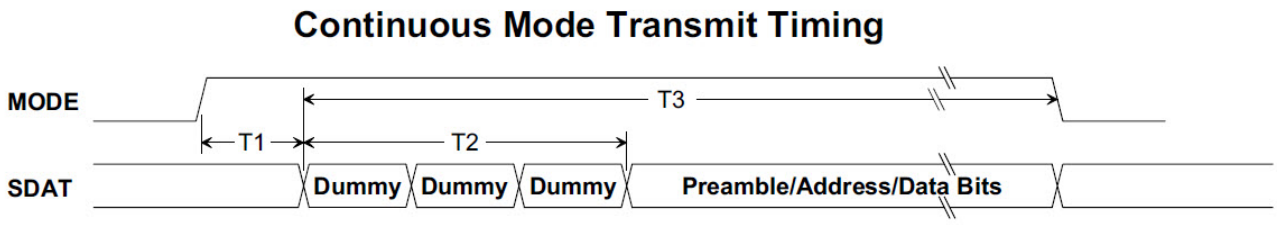


Figure 11

Item	Description	Min	Typ	Max	Unit
T1	MODE to 1st Bit Time		250		µs
T2	Dummy Bits		3		bit
T3	RF Transmission Time			4	ms

Table 10

The TRC104 should not be active for more than 4 ms at a time to allow for internal auto-calibration. Typical calibration time is 200 µs.

5.1.2 Continuous Receive Mode

Continuous Receive Mode is enabled when the **C_Mode** bit of register 0x00 is set to 0 and the **D_Mode** bit of register 0x02 is set to 0. In Continuous Receive Mode, the receive FIFO and automatic packet features *except*

address detection are disabled. The TRC104 host microcontroller must handle functions such as DC-balanced data scrambling and CRC generation for Continuous Receive Mode. Note that a valid sender (local device) address is required for address detection and proper Continuous Receive Mode operation. This address is configured by writing the address byte(s) into configuration registers 0x0E - 0x12, according to the address length specified by the **ADDR_len** bits in configuration register 0x08. The sender address is written least significant byte first, starting in register 0x0E.

The host microcontroller must be powerful enough to handle the chosen serial data rate (250 kb/s or 1 Mb/s) in addition to the other functions required for the end application. Data is read from the SDAT pin. To assist in data recovery, a bit clock is available on the SCLK pin. The state of the SDAT pin is read on the rising edge of SCLK to recover the demodulated data. Figure 12 and Table 11 show the timing for reading data from SDAT.

Continuous Mode Receive Timing

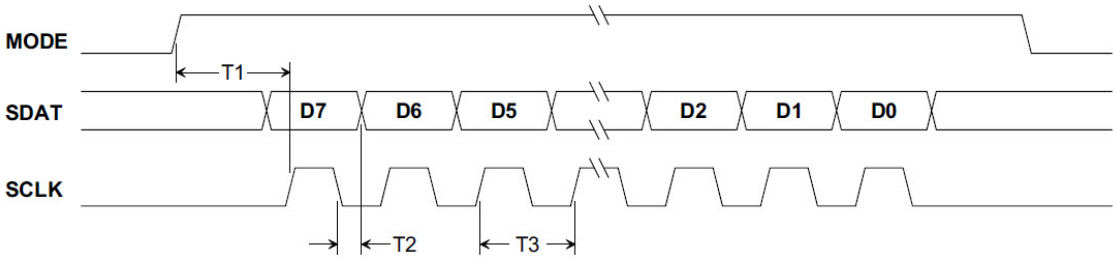


Figure 12

Item	Description	Min	Typ	Max	Unit
T1	MODE to SCLK Time		250		µs
T2	Bit Delay Time		15		ns
T3	SCLK Cycle Time for 1 Mb/s		1		µs
	SCLK Cycle Time for 250 kb/s		4		

Table 11

5.2 Burst Packet Modes

Burst Packet Mode is enabled when the **D_Mode** bit of register 0x02 is set to 1. Burst Packet Mode handles automatic packet features such as preamble generation, address insertion and filtering, DC-balanced data scrambling/descrambling, and CRC generation and error detection. In Burst Packet Mode the FIFO is enabled and used for transmitting or receiving packets. In Burst Packet Mode, the host microcontroller does not have the heavy overhead of bit, byte and packet processing as is the case with the Continuous Mode.

5.2.1 Burst Transmit Mode

Burst Transmit Mode is enabled when the **C_Mode** bit of configuration register 0x00 is set to 1 and the **D_Mode** bit of register 0x02 is set to 1. In Burst Transmit Mode, data is written to the TRC104 before being transmitted, most significant bit or each byte first. The automatic packet features listed in Section 5.2 are available in Burst Mode. Once the FIFO is loaded, three additional dummy bits (any value) are clocked in. The MODE pin is then de-asserted (low) and the packet transmission starts. At the end of the transmission the INT flag is asserted. The INT flag resets when the TRC104 is placed in another mode. Figure 13 and Table 12 show the serial port timing parameters for Burst Transmit Mode.

In Burst Mode, the FIFO length is set to match the number of payload data bytes. When transmitting a packet , the destination address may obtained from one of two sources, either automatically from configuration registers

0x09 - 0x0D, or by writing it directly before the payload data bytes. The source for the destination address is chosen by the **DesADD_ref** bit in configuration register 0x05. When writing the destination address directly, the most significant address byte is written first. Sender (local device) addressing is optional. If used, the sender address is automatically loaded from configuration registers 0x0E - 0x12. The destination address can be from one to five bytes in length. If used, the sender address must be the same length as the destination address.

Serial Port Burst Transmit Mode Timing

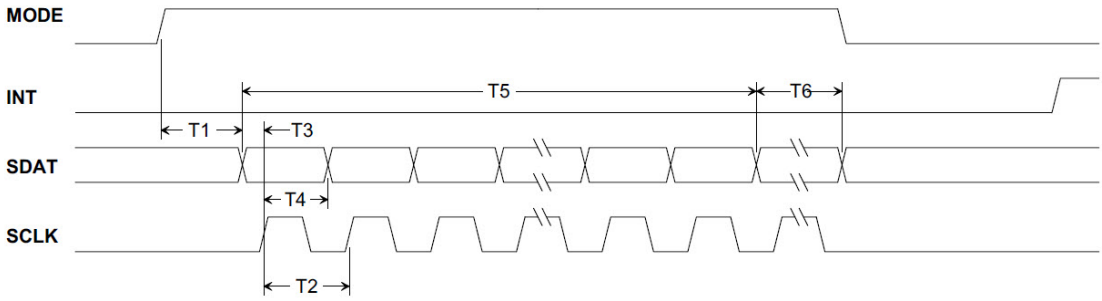


Figure 13

Item	Description	Min	Typ	Max	Unit
T1	MODE to 1st Bit Time	20			µs
T2	SCLK Cycle Time	500			ns
T3	Setup Time		15		ns
T4	Hold Time		15		ns
T5	Address & Payload Data	8		296	bits
T6	Dummy Bit Writes			3	bits

Table 12

5.2.2 Burst Receive Mode

Burst Receive Mode is enabled when the **C_Mode** bit of register 0x00 is set to 0 and the **D_Mode** bit of register 0x02 is set to 1. In Burst Receive Mode, the FIFO is loaded with the payload data part of a received packet. The automatic packet features listed in Section 5.2 are available for use in Burst Receive Mode. Using these features frees up the host microcontroller to perform other tasks.

As a packet is received, the TRC104 uses the preamble to lock to the incoming data rate and then determines if the packet is for it by testing the address following the preamble for a match to its own device address. If the addresses match, the TRC104 receives the remainder of the packet, including the sender address if present, the payload data and CRC. The TRC104 then performs a CRC calculation and compares the result with the received CRC value. If the CRC's match, the INT flag is asserted according to the interrupt polarity as configured by the **LVLINT** bit of configuration register 0x17. Otherwise, the packet is discarded unless this default is overridden.

Upon assertion of the INT flag, the host microcontroller clocks out and discards two dummy bits, and then clocks out received bits, checking the INT flag after each group of 8 bits. The INT flag will de-assert when the next-to-last payload data byte in the FIFO is read. The host microcontroller then completes the read transaction by clocking out the last FIFO byte followed by clocking out and discarding three more dummy bits. When the INT flag is asserted the host microcontroller should read the data quickly so as not to delay listening for the next packet. If the data has not been completely read when the next packet is transmitted, reception will not occur and the transmitted data will be missed. Figure 14 and Table 13 show the serial port timing parameters for Burst Receive Mode.

Serial Port Burst Receive Mode Timing

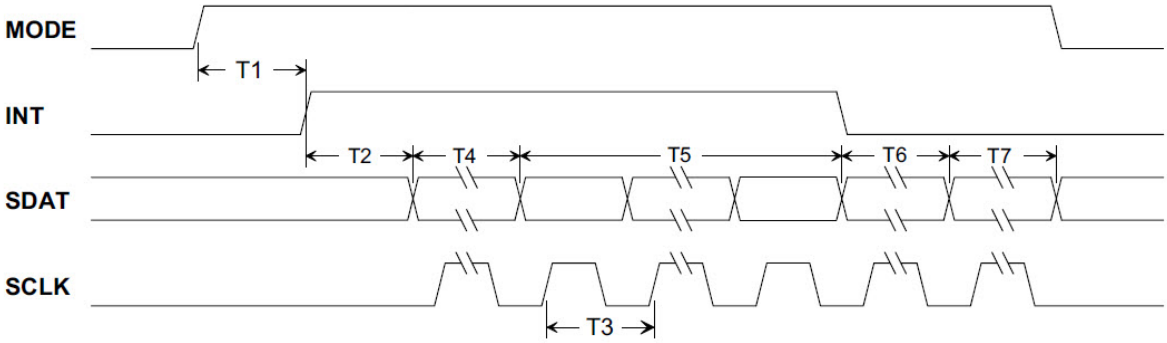


Figure 14

Item	Description	Min	Typ	Max	Unit
T1	MODE to INT Time	0			ns
T2	INT to 1st Bit	0			ns
T3	SCLK Cycle Time	500			ns
T4	Dummy Bit Reads			2	bits
T5	Address & Payload Data Except Last Byte	0		288	bits
T6	Last Payload Data Byte	8			bits
T7	Dummy Bit Reads			3	bits

Table 13

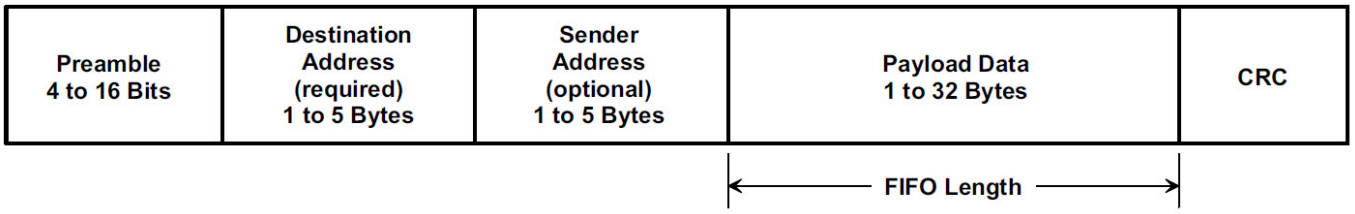
6 Burst Packet Mode Configuration

In Burst Packet Mode, the following packet features are available :

- Configurable FIFO length up to 32 bytes
- Configurable preamble length up to 16 bits
- Configurable address filtering
- Configurable sender/destination address length up to 5 bytes
- Configurable sender (local device) address
- Configurable destination address
- Configurable DC-balanced data scrambling/descrambling
- Configurable CRC generation and error detection

The configuration details of these features are covered below in Sections 6.1 through 6.4. Figure 15 shows the general format of a TRC104 packet.

TRC104 Fixed Length Packet Format



When used, the sender address must be the same length as the destination address. The FIFO must be completely filled with payload data bytes.

Figure 15

6.1 FIFO Configuration

The transmit/receive FIFO length is set with the **FIFO_len** bits in configuration register 0X05. The length can be set from one to 32 bytes. The FIFO must be long enough to hold all payload data bytes. All TRC104 radios in a network *must use the same FIFO length*. The FIFO must be completely filled on every transmission. Padding bytes (user selected value) are used to fill up the transmit FIFO when payload data bytes do not completely fill it.

6.2 Preamble Configuration

The preamble is a 1-0-1-0… sequence of bits sent at the beginning of a packet to allow the receiver data and clock recovery function to lock to the packet bit stream. The preamble is discarded by the receiver. The preamble length is programmable up to 16 bits. The length is configurable in 4-bit segments by setting the **Pream_len** bits in configuration register 0x06. A 16-bit preamble is recommended for most applications.

6.3 Addressing

In Burst Packet mode, the destination address allows a TRC104 to determine if a packet is for it. The sender address can be optionally added to a packet, and is especially useful in networks consisting of more than two radios. The length of the destination addresses is configurable from 1 to 5 bytes. The sender address length is automatically set to the same length. All TRC104 radios in a network *must use the same address length*. The destination address is stripped off by the receiver and is not included in the read out from the FIFO. The sender address may be output before the payload data in a received packet. This feature is enabled through configuration register 0x05, bits 7..6. To avoid random noise causing frequent false detections of a destination address, an address length of at least two bytes is recommended, and three to five bytes is preferred.

6.3.1 Sender (Local Device) Address

The sender (local device) address is configured by writing the address byte(s) into configuration registers 0x0E - 0x12, according to the address length specified by the **ADDR_len** bits in configuration register 0x08. The sender address is written least significant byte first, starting in register 0x0E. The sender address is automatically added to a transmit packet by setting the **DevADD_En** bit to 0 in configuration register 0x05. The sender address may be optionally read out before the payload data in a received packet. This is useful when receiving messages from multiple sources. This option is enabled by setting the **SADDR_pos** bit to 0 in configuration register 0x05.

6.3.2 Destination Address

The destination address is the first field sent after the preamble. If the destination address in a received packet does not match the address stored in the sender (local device) address configuration registers, the packet is discarded and the host microcontroller does not receive an INT flag. The destination address is configured by writing the address byte(s) into configuration registers 0x09 - 0x0D, according to the address length specified by the **ADDR_len** bits in configuration register 0x08. The destination address is written least significant byte first, starting in register 0x09. When transmitting a packet, the destination address may obtained from one of two sources, either automatically from configuration registers 0x09 - 0x0D, or by writing it directly in the packet destination address field. The source for the destination address is chosen by the **DesADD_ref** bit in configuration register 0x05.

6.4 DC-Balanced Scrambling

The TRC104 is equipped with a scrambling/descrambling function to improve the DC-balance of a transmitted bit stream. The implementation is show in Figure 16. This function is enabled by setting the SCR_En bit in configuration register 0x02 to 1. The scrambling/descramble function is only available in Burst Packet Mode.

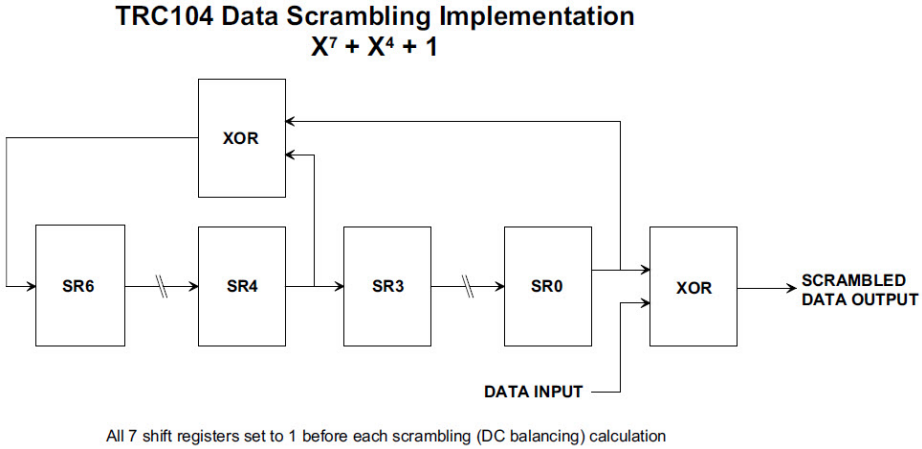


Figure 16

6.4 CRC Error Detection

The CRC error detection option is enabled by setting the **CRC_En** bit in configuration register 0x02 to 1. A two-byte CRC is automatically calculated on the payload field and appended to the end of the transmitted packet. On the receive side, the CRC is recalculated on the payload field and compared to the received CRC. If the CRC match fails, the received packet is handled according to the setting of the **CRC_ERR** bit in configuration register 0x02. Otherwise, a good CRC match generates a flag on the INT pin, and the received CRC is discarded. The polarity of the INT flag is configured by the **LVLINT** bit in configuration register 0x17. There is no interrupt generation for a failed packet. The CRC calculation is based on the CCITT polynomial as shown in Figure 17.

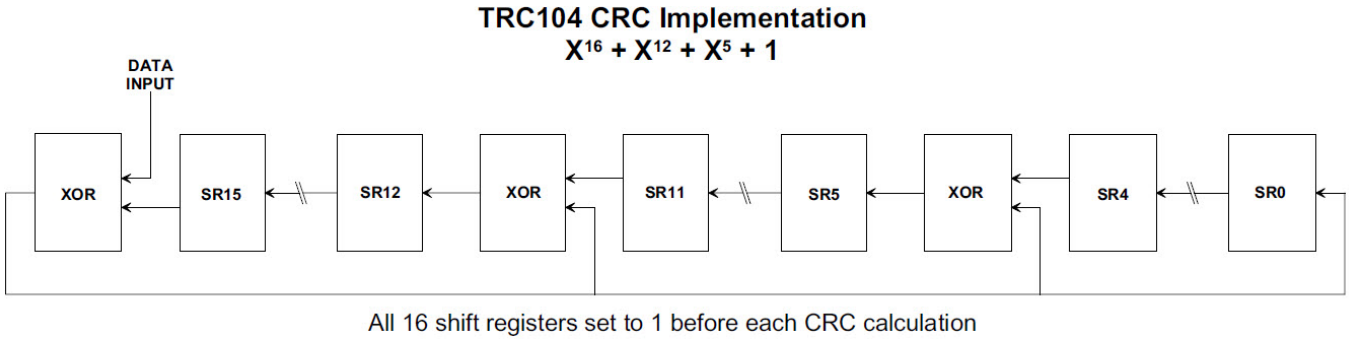


Figure 17

7 Serial Interface

The serial interface provides two-wire serial communication between the TRC104 and its host microcontroller, as shown in Figure 18. All FIFO and configuration parameters are accessible through the serial interface. The FIFO and configuration data pass through the bidirectional SDAT pin with host microcontroller clocking on the SCLK pin. The CS pin state selects whether the FIFO (Burst Packet Mode only) or the internal configuration registers are accessed.

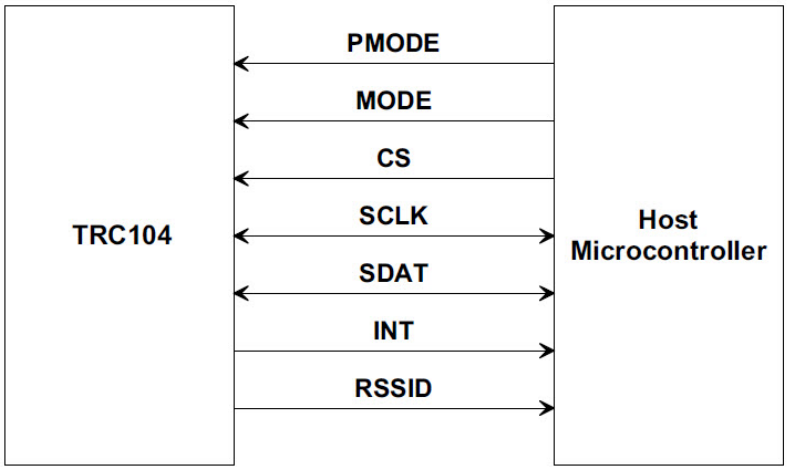


Figure 18

The serial interface is enabled for read/write transactions with the configuration registers by holding the CS pin high. The CS pin must remain high during the transmission of both the address and data bytes or the data will be corrupted. Between each configuration register read/write transaction the serial interface *must be reset by pulling the CS pin low*. Pulling CS high again re-enables the serial interface for a new configuration register read/write transaction. Back-to-back configuration register read/writes are not possible as the configuration register address is not automatically incremented. Refer to Sections 7.1 for additional configuration register access details.

The serial interface is enabled for read/write transactions with the FIFO by holding the CS pin low. Data and clocking are handled through the SDAT and SCLK pins, respectively.

7.1 Configuration Registers Access

The most significant bit of each byte is sent first. The rising SCLK edge is used to sample the received bit, and the falling SCLK edge shifts the data inside the shift register. The most significant bit of the first byte specifies a read or write command followed by seven address bits. The following byte contains the read/write data.

Two bytes are required for each configuration register transaction. The first byte contains the R/W bit (0 = read, 1 = write) and the 7-bit configuration register address. The second byte contains the configuration value to be written or read from the address specified in the first byte. Figure 19 and Table 14 show the timing for a configuration read sequence from the TRC104.

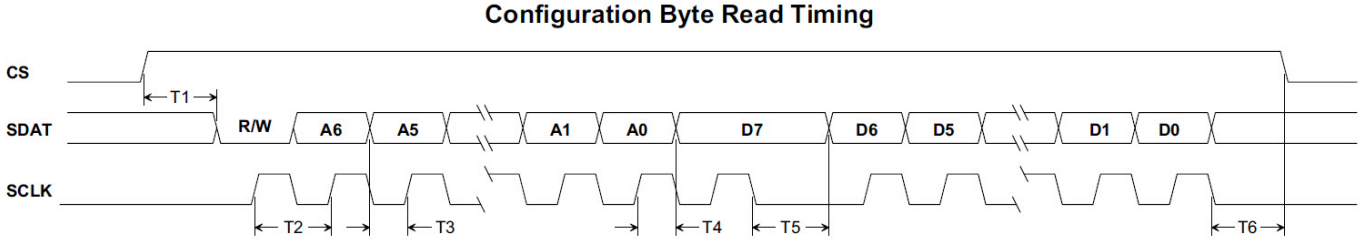


Figure 19

Item	Description	Min	Typ	Max	Unit
T1	CS to 1st Bit Time	20			µs
T2	SCLK Cycle Time	200			ns
T3	Setup Time	10			ns
T4	Hold Time	10			ns
T5	Data Bit Hold Time			20	ns
T6	Last Bit to CS Time	50			ns

Table 14

Figure 20 and Table 5 show the timing for a configuration write sequence to the TRC104.

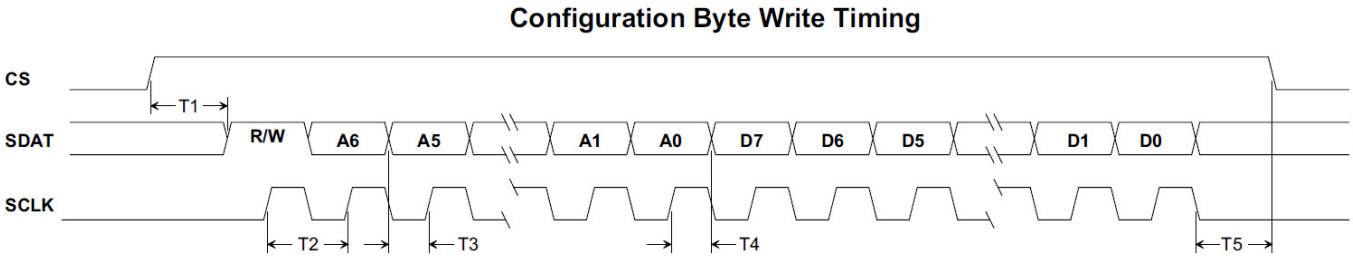


Figure 20

Item	Description	Min	Typ	Max	Unit
T1	CS to 1st bit time	20			µs
T2	SCLK cycle time	200			ns
T3	Setup time	10			ns
T4	Hold time	10			ns
T5	Last bit to CS time	50			ns

Table 15

7.2 Transmit/Receive FIFO Access

Serial data is sent or received through the FIFO according to the TRC104 mode of operation. If the TRC104 is configured for Burst Receive Mode, a FIFO read transaction is implemented on the serial interface. If the TRC104 is configured for Burst Transmit Mode, a FIFO write transaction is implemented on the serial interface. The CS pin must be held low during FIFO transactions. If the CS is allowed to go high, the TRC104 will interpret the data as a register configuration transaction and possibly corrupt the device configuration. See Sections 5.2.1 and 5.2.2 for details on Burst Transmit Mode and Burst Receive Mode using the FIFO.

8 Configuration Registers

The TRC104's user configuration registers are mapped in the address range of 0x00 through 0x18. Sections 8.1 through 8.17 below provide the details for each configuration register. Power-up default settings for the configuration register bit and byte patterns are shown in **bold.**

8.1 T/R Mode and Channel Frequency Control

0x00 [default 0x28]

Address	Name	Bits	R/W	Description
0X00	C_Mode	7	r/w	Chip Mode: **0 → Receive Mode** 1 → Transmit Mode
	Ch_Num	6..0	r/w	Channel Frequency: F_{RF} = 2400 + (Ch_Num) in MHz, 1 ≤ Ch_Num ≤ 127 **[default is 00101000b]**

Table 16

8.2 Transmitter Power and Crystal Frequency Control

0x01 [default 0x03]

Address	Name	Bits	R/W	Description
0X01	-	7..5	r/w	Reserved, always set to 000b
	PWR	4..3	r/w	Transmitter Output Power: **00 → -20 dBm** 01 → -10 dBm 10 → -5 dBm 11 → 0 dBm
	FXTAL	2..0	r/w	Crystal Frequency Selection: 000 → 4 MHz 001 → 8 MHz 010 → 12 MHz **011 → 16 MHz** 100 → 20 MHz

Table 17

8.3 Data Function Control

0x02 [default 0x78]

Address	Name	Bits	R/W	Description
0X02	-	7	r/w	Reserved, always set to 0b
	D_Mode	6	r/w	Data Mode Select: 0 → Continuous Mode **1 → Burst Mode**
	DR	5	r/w	Data Rate Select: 0 → 250 kb/s **1 →1 Mb/s**
	Ciph_En	4	r/w	DC-balanced Data Scrambling Enable bit (Burst Mode only): 0 → Disable Data Scrambling **1 → Enable Data Scrambling** Scramble Polynomial = $X^7 + X^4 + 1$
	CRC_En	3	r/w	CRC-16 Enable bit (Burst Mode only): 0 → Disable CRC **1 → Enable CRC** CRC Polynomial = $X^{16} + X^{12} + X^5 + 1$
		2..1	r/w	Reserved, always set to 0b
	CRC_ERR	0	r/w	Controls clearing the FIFO in Burst Receive Mode if the CRC fails for the current packet **0 → Discard on CRC error** 1 → Do not discard on CRC error

Table 18

8.4 RSSI Function Control

0x03 [default 0x87]

Address	Name	Bits	R/W	Description
0X03	-	7..5	r/w	Reserved, always set to 000b
	RSSIA_Rfsh	4	r/w	Analog RSSI refresh control bit (Continuous Mode only): **0 → Do not refresh RSSI value** 1 → Refresh RSSI value See Section 3.7 for details of RSSI operation
	RSSIA_thr	3..0	r/w	DRSSI threshold: when the RSSIA level exceeds RSSIA_thr, the RSSID pin is set high **default is 0111b**

Table 19

8.5 RSSI Value

0x04 [default 0x20]

Address	Name	Bits	R/W	Description
0X04	-	7..6	r/w	Reserved, always set to 00b
	AGC_En	5	r/w	Automatic Gain Control Enable (Continuous Mode only): 0 → Disable AGC **1 → Enable AGC** AGC should be left enabled for most applications
	RSSI_G	4	r/w	RSSI Gain Mode Selection (Continuous Mode only): **0 → High gain mode** 1 → Low gain mode
	RSSI_val	3..0	r/w	4-bit digital value of RSSI level after A/D conversion.

Table 20

8.6 Data Format Control

0x05 [default 0x0F]

Address	Name	Bits	R/W	Description
0X05	DevAdd_En	7	r/w	Insert sender (local device) address in transmit packet (Burst Mode only): **0 → Insert sender address** 1 → Do not insert sender address
	DevAdd_pos	6	r/w	Output received sender address before payload data on receive (Burst Mode only): **0 → Output sender address** 1 → Do not output sender address
	DesAdd_ref	5	r/w	Destination address reference (Burst Mode only): **0 → Registers 0x09 - 0x0D** 1 → Provided by the host microcontroller before data is written to FIFO
	FIFO_len	4..0	r/w	FIFO length (number of payload data bytes, Burst Mode only): 00000 → 1 byte 00001 → 2 bytes … 11111 → 32 bytes Payload data bytes = FIFO_len + 1 where 0 ≤ FIFO_len ≤ 31 **default is 01111b**

Table 21

8.7 Preamble Control

0x06 [default 0x30, override to 0xB0]

Address	Name	Bits	R/W	Description
0X06	-	7..6	r/w	Reserved, always set to **10b**
	Pream_len	5..4	r/w	Preamble length (Burst Mode only): 00 → 4 bits 01 → 8 bits 10 → 12 bits **11 → 16 bits**
	-	3..0	r/w	Reserved, always set to **0000b**

Table 22

8.8 Transmitter Rise/Fall Time Control

0x07 [default 0x21]

Address	Name	Bits	R/W	Description
0X07	-	7..6	r/w	Reserved, always set to 00b
	PA_RU	5..4	r/w	Power amplifier ramp-up time (Burst Mode only), reduces transmit bandwidth 00 → 0 µs **01 → 10 µs** 10 → 20 µs 11 → 30 µs
	PA_RD	3..2	r/w	Power amplifier ramp-down time (Burst Mode only), reduces transmit bandwidth **00 → 5 µs** 01 → 10 µs 10 → 20 µs 11 → 30 µs
	PA_ON	1..0	r/w	Power amplifier turn-on delay time (Burst Mode only) 00 → 0 µs **01 → 50 µs** 10 → 100 µs 11 → 150 µs

Table 23