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High Efficiency 1A/2A/3A Current-Mode Synchronous Buck DC/DC Converter, 1MHz

TRIUNE PRODUCTS

Features

- Fixed output voltage choices: 1.5V, 1.8V, 2.5V, 3.3V, and 5V with +/- 2% output tolerance
- Adjustable version output voltage range: 0.9V to (VCC – 1V) with +/-1.5% reference.
- Wide input voltage range
  - TS30011/12: 4.5V to 24V (26.4V Abs Max
  - TS30013: 4.5V to 18V (20V Abs Max)
- 1MHz +/- 10% fixed switching frequency
- Continuous output current: 1A (TS30011), 2A (TS30012) and 3A (TS30013)
- High efficiency – up to 95%
- Current mode PWM control with PFM mode for improved light load efficiency
- Voltage supervisor for VOUT reported at the PG pin
- Input supply under voltage lockout
- Soft start for controlled startup with no overshoot
- Cycle-by-cycle currrent limit with frequency foldback
- Full protection for over-temperature and VOUT over-voltage
- Less than 10uA in standby mode
- Low external component count

Applications

- On-card switching regulators
- Set-top box, DVD, LCD, LED supply
- Industrial power supplies

Description

The TS30011 (1A), TS30012 (2A) and TS30013 (3A) are DC/DC synchronous switching regulator with fully integrated power switches, internal compensation, and full fault protection. The switching frequency of 1MHz enables the use of small filter components resulting in minimal board space and reduced BOM costs.

The TS30011/12/13 utilizes current mode feedback in normal regulation PWM mode. When the regulator is placed in standby (EN is low), the device draws less than 10uA quiescent current.

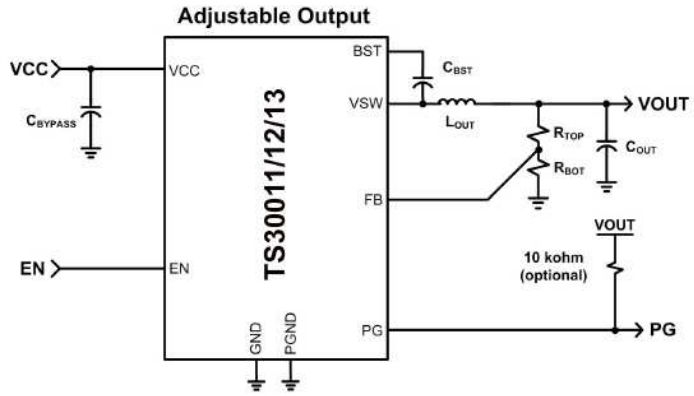
The TS30011/12/13 integrates a wide range of protection circuitry including input supply under-voltage lockout, output voltage soft start, current limit, and thermal shutdown.

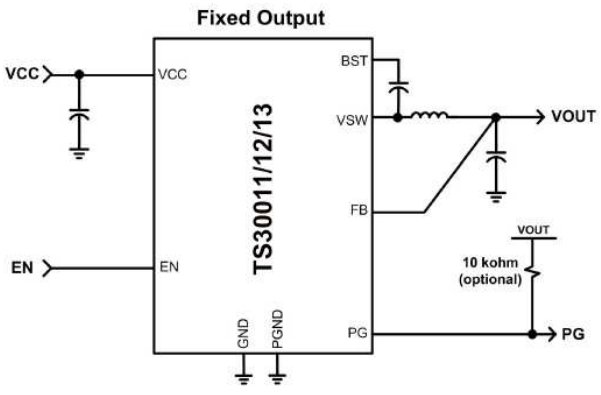
The TS30011/12/13 includes supervisory reporting through the PG (Power Good) open drain output to interface other components in the system.

Summary Specification

- Junction operating temperature -40 °C to 125 °C
- Packaged in a 16pin QFN (3x3)

Typical Application Circuit





Pin Configuration

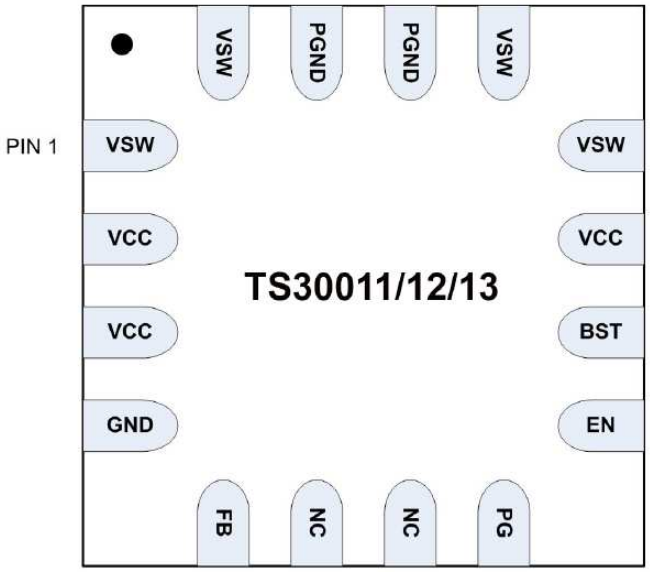


Figure 1: 16 Lead 3x3 QFN, Top View

Pin Description

Pin #	Pin Symbol	Function	Description
1	VSW	Switching Voltage Node	Connected to 4.7uH (typical) inductor
2	VCC	Input Voltage	Input voltage
3	VCC	Input Voltage	Input voltage
4	GND	GND	Primary ground for the majority of the device except the low-side power FET
5	FB	Feedback Input	Regulator FB Input. Connects to VOUT for fixed mode and the output resistor divider for adjustable mode
6	NC	No Connect	Not Connected
7	NC	No Connect	Not Connected
8	PG	Power Good Output	Open-drain output
9	EN	Enable Input	Above 2.2V the device is enabled. GND the EN pin to put device in standby mode. Includes internal pull-up resistor.
10	BST	Bootstrap Capacitor	Bootstrap capacitor for the high-side FET gate driver. Connect a ceramic capacitor in the range 15 nF - 200 nF from BST pin to VSW pin
11	VCC	Input Voltage	Input Voltage
12	VSW	Switching Voltage Node	Connected to 4.7uH (typical) inductor
13	VSW	Switching Voltage Node	Connected to 4.7uH (typical) inductor
14	PGND	Power GND	GND supply for internal low-side FET/integrated diode
15	PGND	Power GND	GND supply for internal low-side FET/integrated diode
16	VSW	Switching Voltage Node	Connected to 4.7uH (typical) inductor
17	PAD	Thermal PAD	Connected internally to GND

Functional Block Diagrams

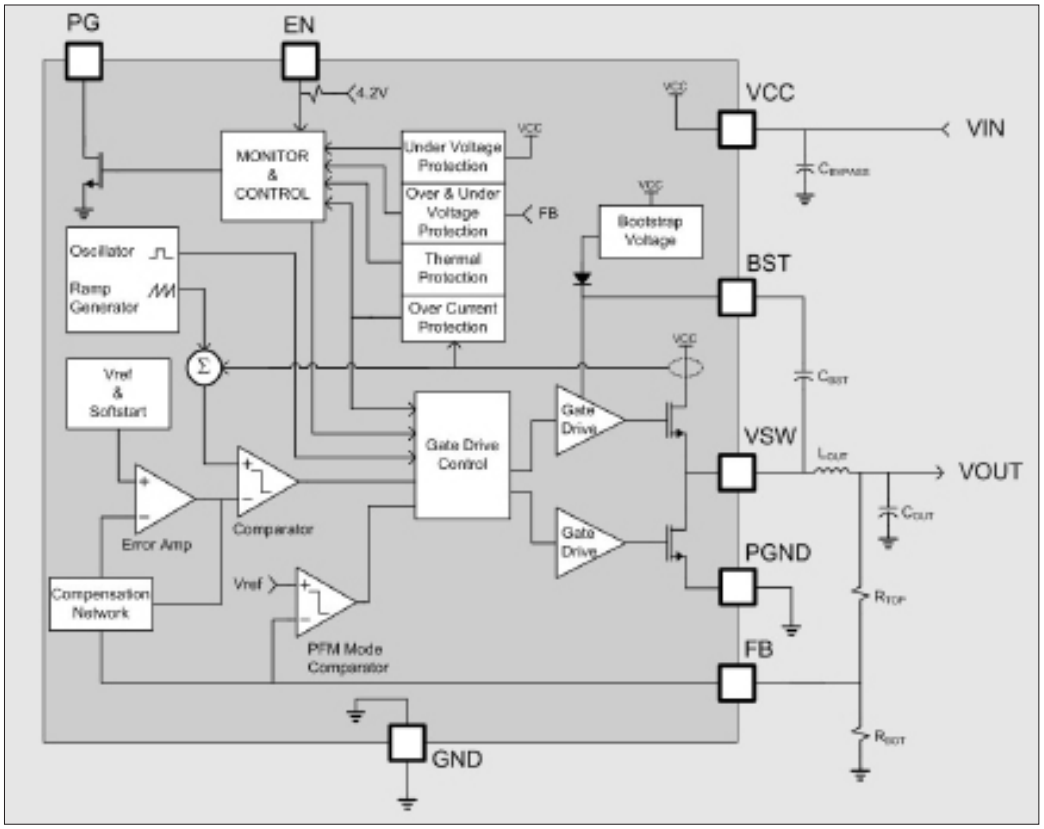


Figure 2: TS30011/12/13 Block Diagram

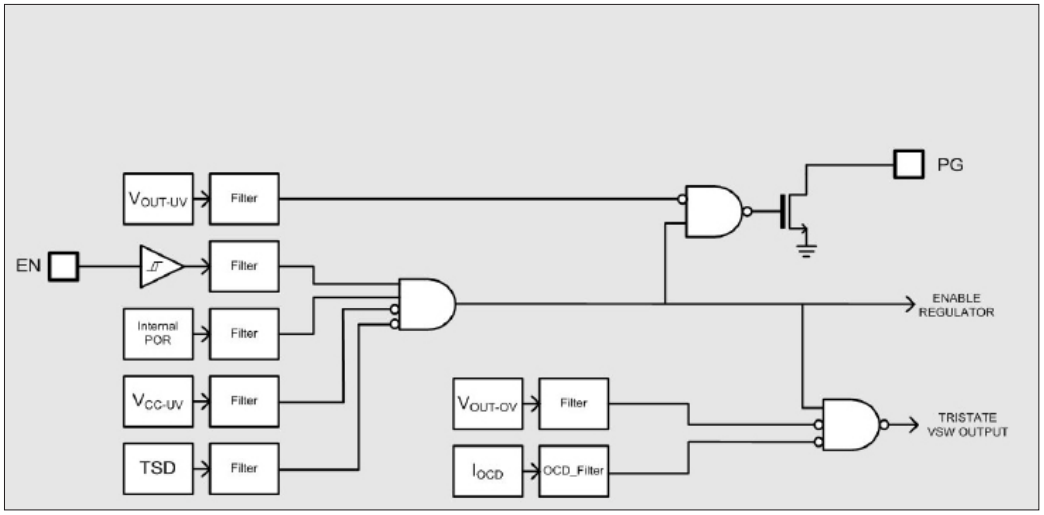


Figure 3: Monitor & Control Logic Functionality

Absolute Maximum Ratings

Over operating free–air temperature range unless otherwise noted(1, 2).

Parameter	Value	Units
VCC to PGND	-0.3 to 26.4 (-0.3 to 20 for TS30013)	V
BST to PGND	-0.3 to (VCC+6)	V
BST to VSW	-0.3 to 6	V
VSW to PGND	-1 to 26.4 (-1 to 20 for TS30013)	V
EN, PG, FB to GND	-0.3 to 6	V
PGND to GND	-0.3 to 0.3	V
Electrostatic Discharge – Human Body Model	+/-2k	V
Electrostatic Discharge – Charge Device Model	+/-500	V
Lead Temperature (soldering, 10 seconds)	260	^{O}C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

Thermal Characteristics

Parameter	Symbol	Value	Units
Thermal Resistance Junction to Air (Note 1)	θ_{JA}	34.5	^{O}C/W
Thermal Resistance Junction to Case (Note 1)	θ_{JC}	2.5	^{O}C/W
Storage Temperature Range	T_{STG}	-65 to 150	^{O}C
Maximum Junction Temperature	$T_{J\,MAX}$	150	^{O}C
Operating junction Temperature Range	T_{J}	-40 to 125	^{O}C

Note 1: Assumes 16LD 3x3 QFN with hi-K JEDEC board and 13.5 inch^2 of 1 oz Cu and 4 thermal vias connected to PAD

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Input Operating Voltage	VCC	4.5	12	24 (18 for TS30013)	V
Bootstrap Capacitor	C_{BST}	15	22	200	nF
Output Filter Inductor Typical Value (Note 1)	L_{OUT}	3.3	4.7	5.64	uH
Output Filter Capacitor Typical Value (Note 2)	C_{OUT}	33	44 (2 x 22)		uF
Output Filter Capacitor ESR	$C_{OUT-ESR}$	2		100	mΩ
Input Supply Bypass Capacitor Typical Value (Note 3)	C_{BYPASS}	8	10		uF

Note 1: For best performance, use an inductor with saturation current rating exceeding the maximum expected load plus 50% of the inductor current ripple.

Note 2: For best performance, a low ESR ceramic capacitor should be used.

Note 3: For best performance, a low ESR ceramic capacitor should be used. If C_{BYPASS} is not a low ESR ceramic capacitor, a 0.1uF ceramic capacitor should be added in parallel to CBYPASS

Electrical Characteristics

Electrical Characteristics, T_J = -40C to 125C, V_{CC} = 12V (unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
VCC Supply Voltage						
Input Supply Voltage	V_{CC}		4.5		24 (18 for TS30013)	V
Quiescent current Normal Mode	$I_{CC-NORM}$	V_{CC} = 12V, V_{OUT}=1.8V, I_{LOAD} = 0A		3.3		mA
Quiescent current Normal Mode – Non-switching	$I_{CC-NOSWITCH}$	V_{CC}=12V, I_{LOAD}=0A, Non-switching		2.3		mA
Quiescent current Standby Mode	$I_{CC-STBY}$	V_{CC} = 12V, EN = 0V		5	10	µA
VCC Under Voltage Lockout						
Input Supply Under Voltage Threshold	V_{CC-UV}	V_{CC} Increasing		4.3	4.5	V
Input Supply Under Voltage Threshold Hysteresis	V_{CC-UV_HYST}	V_{CC} Decreasing		350		mV
OSC						
Oscillator Frequency	f_{OSC}		0.9	1	1.1	MHz
Foldback Switching Frequency	f_{fb}	V_{FB}<60% x 0.9V (For TS30013)		250		KHz
PG Open Drain Output						
PG Threshold Voltage	V_{OUT_UV}	Sweep V_{FB} from Low-to-High	91	93	95	$\%V_{OUT}$
PG Hysteresis	$V_{OUT\_UV\_HYST}$	Sweep V_{FB} from High-to-Low		1.5		$\%V_{OUT}$
PG Recovery Hold Time	t_{PG}	PG recovery after power restoration		11		ms
High-Level Output Leakage	I_{OH-PG}	V_{PG} = 5V		0.5		µA
Low-Level Output Voltage	V_{OL-PG}	V_{FB} < 90% x V_{NOM}, I_{PG} = -0.3mA			0.01	V
EN Input Voltage Thresholds						
High Level Input Voltage	V_{IH-EN}		2.2			V
Low Level Input Voltage	V_{IL-EN}				0.8	V
Input Hysteresis	$V_{HYST-EN}$			480		mV
Input Leakage	I_{IN-EN}	V_{EN} = 5V		3.5		µA
		V_{EN} = 0V		-1.5		µA
Thermal Shutdown						
Thermal Shutdown Junction Temperature	TSD	Note: not tested in production	150	170		°C
TSD Hysteresis	TSD_{HYST}	Note: not tested in production		10		°C

Regulator Characteristics

Electrical Characteristics, T_J = -40C to 125C, V_{CC} = 12V (unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Switch Mode Regulator: L=4.7uH and C=2 x 22uF						
Output Voltage Tolerance in PWM Mode	$V_{OUT-PWM}$	I_{LOAD} =1A	V_{OUT} – 2%	V_{OUT}	V_{OUT} + 2%	V
Output Voltage Tolerance in PFM Mode	$V_{OUT-PFM}$	I_{LOAD} = 0A	V_{OUT} – 1%	V_{OUT} + 1%	V_{OUT} + 3%	V
Line Regulation		V_{cc} = 4.5V to 24V (to 18V for TS30013)		0.5		%
Load Regulation		I_{OUT} = 100mA to 3A (For TS30013)		0.5		%
High Side Switch On Resistance	R_{DSON}	I_{VSW} = -1A (Note 1)		180		mΩ
Low Side Switch On Resistance		I_{VSW} = 1A (Note 1)		120		mΩ
Output Current	I_{OUT}	TS30013 (Note 4)			3	A
		TS30012 (Note 4)			2	A
		TS30011			1	A
Over Current Detect (High Side Switch Current)	I_{OCD}	TS30013	3.4	3.8	4.4	A
		TS30012	2.4	2.8	3.4	A
		TS30011	1.4	1.8	2.4	A
Feedback Reference (Adjustable Mode)	FB_{TH}	(Note 3)	0.886	0.9	0.914	V
Feedback Reference Tolerance	FB_{TH-TOL}	(Note 3)	-1.5		1.5	%
Feedback Bias Current	I_{FB}	V_{FB}=0.6V		50	500	nA
Soft start Ramp Time	t_{SS}			4		ms
PFM Mode FB Comparator Threshold	FB_{TH-PFM}			V_{OUT} + 1%		V
V_{OUT} Over Voltage Threshold	V_{OUT-OV}			103% V_{OUT}		
V_{OUT} Over Voltage Hysteresis	V_{OUT-OV_HYST}			1% V_{OUT}		
Max Duty Cycle	$DUTY_{MAX}$	(Note 2)	95%	97%	99%	

Note 1: R_{DSON} is characterized at 1A and tested at lower current in production.
Note 2: Regulator VSW pin is forced off for 240ns every 8 cycles to ensure the BST cap is replenished.
Note 3: For the adjustable version, the ratio of VCC/Vout cannot exceed 16.
Note 4: Based on Over Current Detect testing

Typical Performance Characteristics

T_J = -40C to 125C, VCC = 12V (unless otherwise noted)

Figure 4. Startup Response

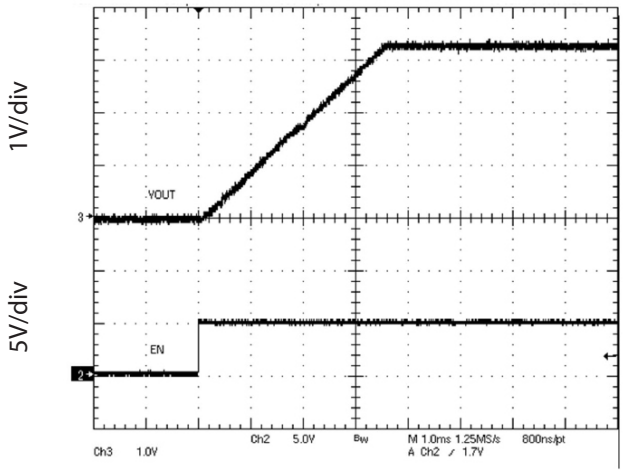


Figure 5. 100mA to 1A Load Step (V_{CC}=12V, V_{OUT}=1.8V)

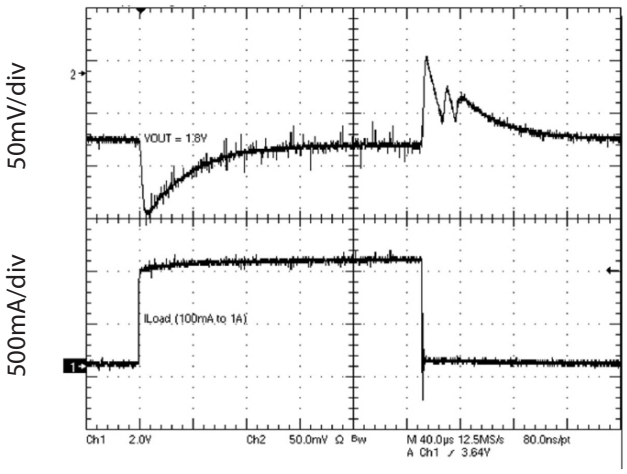


Figure 6. 100mA to 2A Load (V_{CC}=12V, V_{OUT}=1.8V)

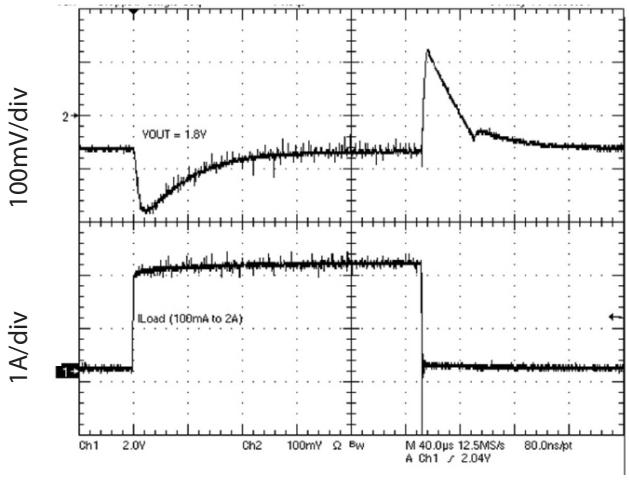


Figure 7. 100mA to 1A Load Step (V_{CC}=12V, V_{OUT}=3.3V)

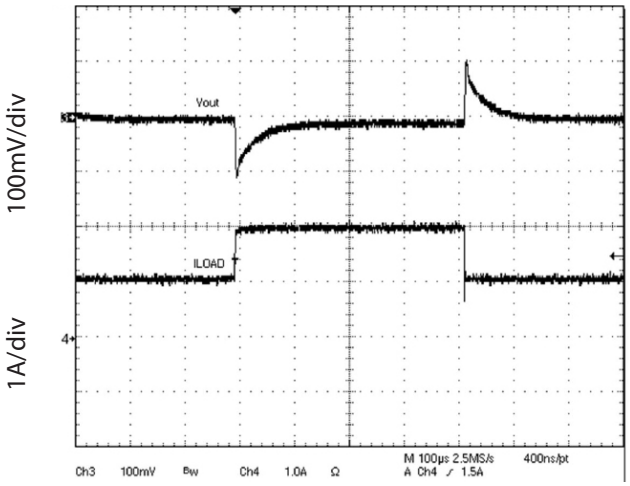


Figure 8. 100mA to 2A Load Step (V_{CC}=12V, V_{OUT}=3.3V)

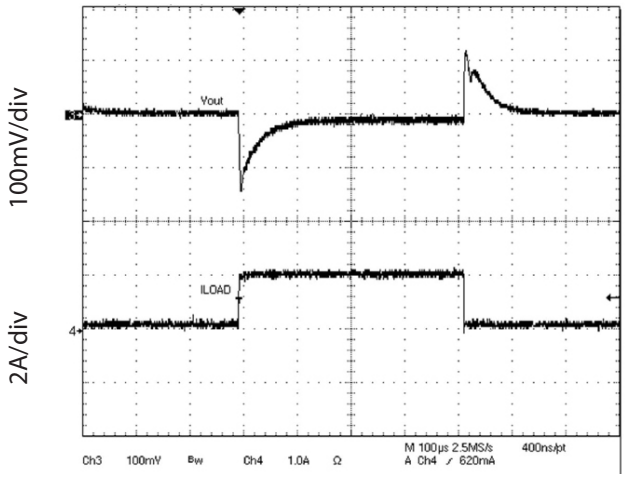
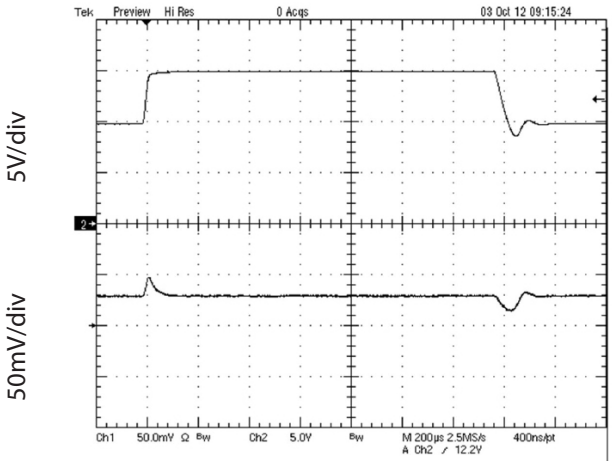


Figure 9. Line Transient Response (V_{CC}=12V, V_{OUT}=3.3V)



Typical Performance Characteristics continued

T_J = -40C to 125C, VCC = 12V (unless otherwise noted)

Figure 10. Load Regulation (V_{OUT} = 3.3V)

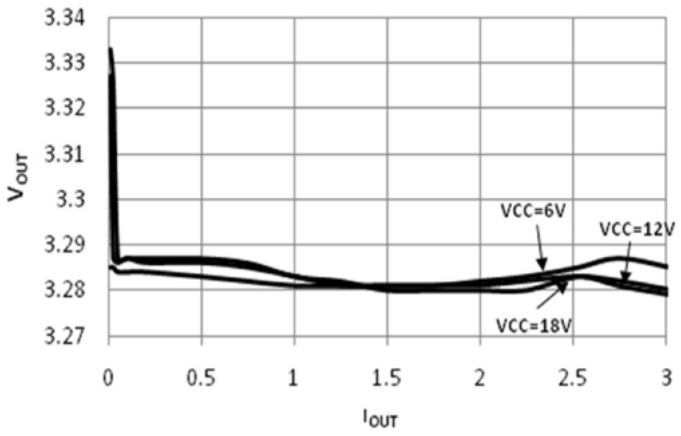


Figure 11. Line Regulation (I_{OUT}=1A)

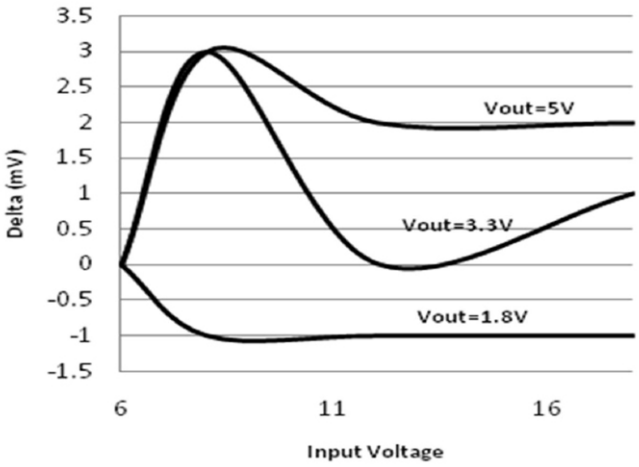


Figure 12. Efficiency vs. Output Current (V_{OUT} = 1.8V)

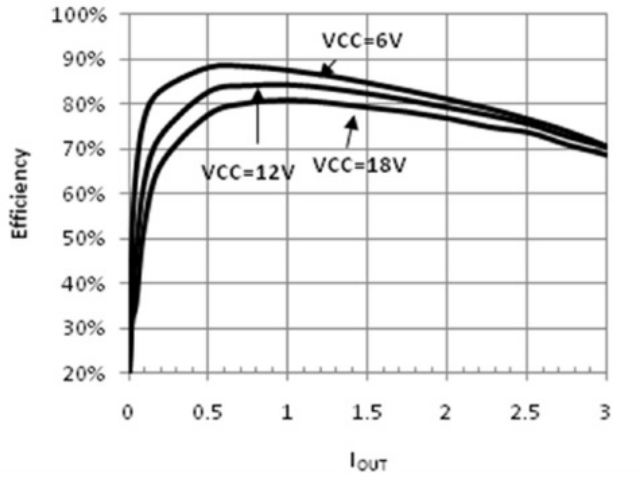


Figure 13. Efficiency vs. Output Current (V_{OUT} = 3.3V)

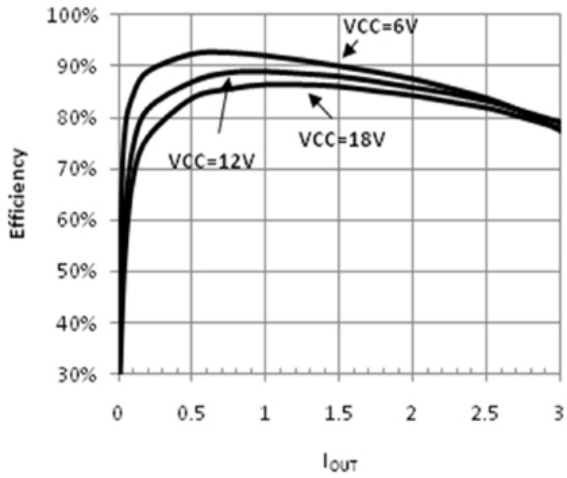


Figure 14. Efficiency vs. Output Current (V_{OUT} = 5V)

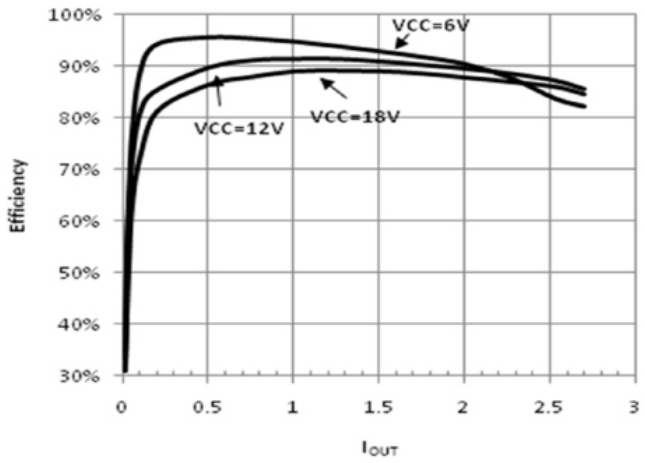
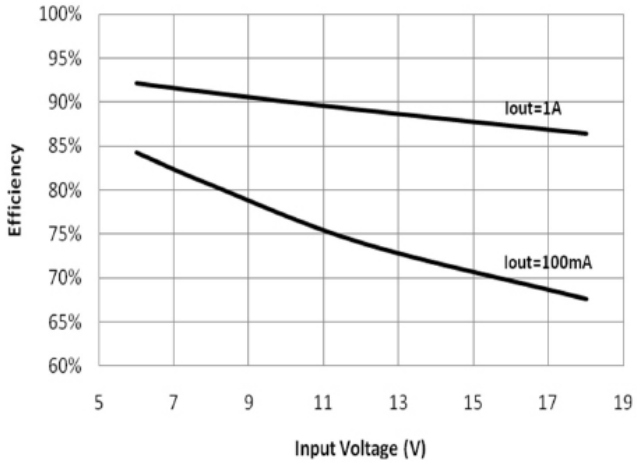


Figure 15. Efficiency vs. Input Voltage (V_{OUT} = 3.3V)



Typical Performance Characteristics continued

T_J = -40C to 125C, VCC = 12V (unless otherwise noted)

Figure 16. Standby Current vs. Input Voltage

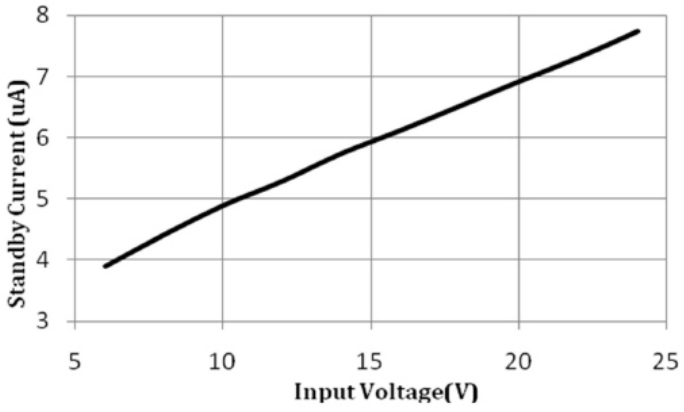


Figure 17. Standby Current vs. Temperature

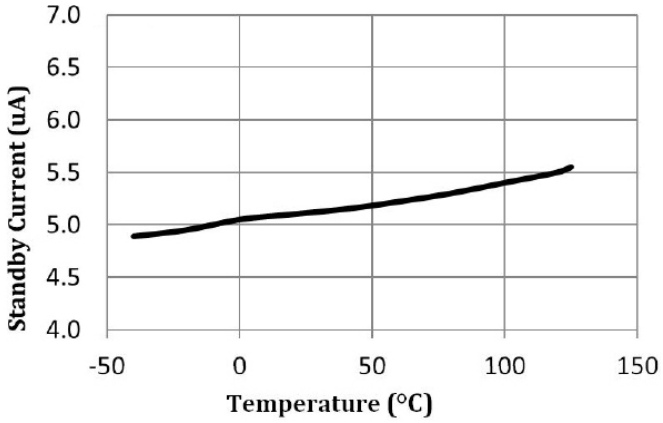


Figure 18. Output Voltage vs. Temperature (V_{OUT} = 3.3V)

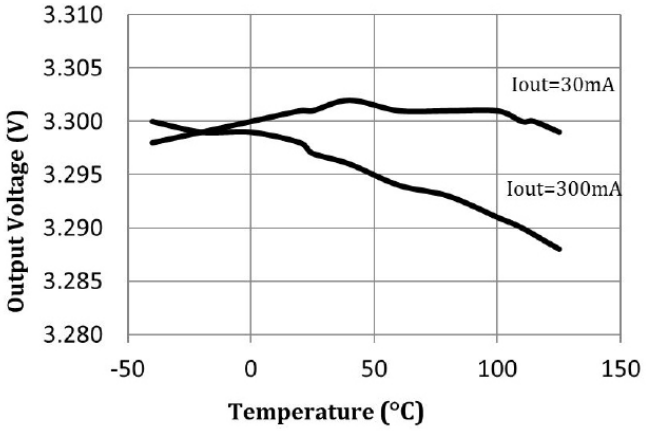


Figure 19. Oscillator Frequency vs. Temperature (I_{OUT}=300mA)

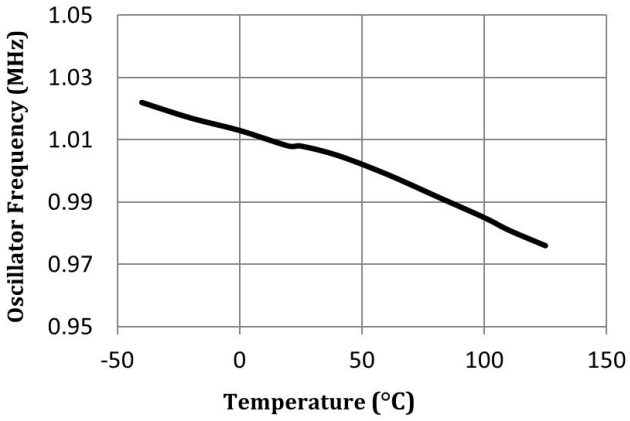


Figure 20. Quiescent Current vs. Temperature (No load)

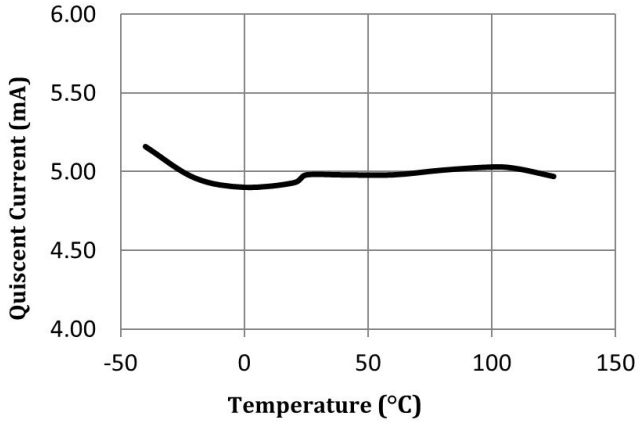
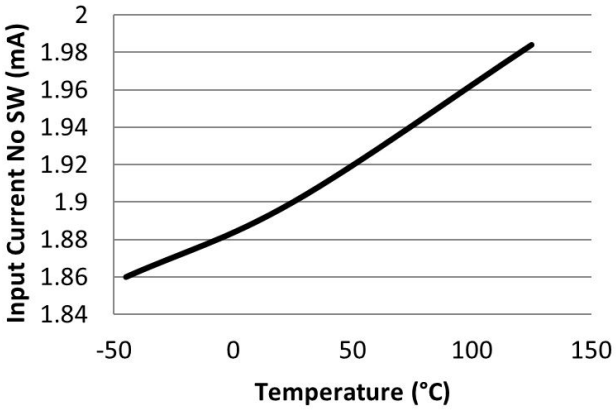


Figure 21. Input Current vs. Temperature (No load, No switching)



Functional Description

The TS30011/12/13 current-mode synchronous step-down regulator is ideal for use in the commercial, industrial, and automotive market segments. It includes flexibility to be used for a wide range of output voltages and is optimized for high efficiency power conversion with low RDSON integrated synchronous switches. A 1MHz internal switching frequency facilitates low cost LC filter combinations. Additionally, the fixed output versions enable reduce the external component count and provide a complete regulation solution with only 4 external components: an input bypass capacitor, an inductor, an output capacitor, and the bootstrap capacitor. The regulator automatically transitions between PFM and PWM mode to maximize efficiency for the load demand.

The TS30011/12/13 provides these system benefits:

- Reduced board real estate
- Lower system cost
  - Lower cost inductor
  - Low external parts count
- Ease of design
  - Bill of Materials and suggested board layout provided
  - Power Good output
  - Integrated compensation network
  - Wide input voltage range
- Robust solution
  - Over current, over voltage and over temperature protection

Detailed Pin Description

Unregulated input, VCC

This terminal is the unregulated input voltage source for the IC. It is recommended that a 10uF bypass capacitor be placed close to the device for best performance. Since this is the main supply for the IC, good layout practices need to be followed for this connection.

Bootstrap control, BST

This terminal provides the bootstrap voltage required for the upper internal NMOS switch of the buck regulator. An external ceramic capacitor placed between the BST input terminal and the VSW pin provides the necessary voltage for the upper switch. In normal operation the capacitor is recharged on every switching cycle when the low-side NMOS is on.

In the case of where the switch mode approaches 100% duty cycle for the high side FET, the device automatically reduces the duty cycle switch to a minimum off time on every 8th cycle to allow this capacitor to re-charge

Sense feedback, FB

This is the input terminal for the output voltage feedback.

For the fixed output versions, this should be hooked directly to $V_{OUT.}$ The PCB connection should be kept as short as possible, and should be made as close as possible to the output capacitor. The trace should not be shared with any other connection. (Figure 24)

For adjustable output versions, the FB input should be connected to the external resistor divider. To choose the resistors, use the following equation:

$$V_{OUT} = 0.9\ (1 + R_{TOP}/R_{BOT})$$

The FB input is high impedance and input current should be less than 100nA. As a result, good layout practices are required for the feedback resistors and feedback traces. When using the adjustable version, the feedback trace should be kept as short as possible with minimum width to reduce stray capacitance and to reduce the injection of noise.

For adjustable output versions, the ratio of VCC/V_{OUT} cannot exceed 16.

Switching output, VSW

This is the switching node of the regulator. It should be connected directly to the 4.7uH inductor with a wide, short trace and also to one end of the Bootstrap capacitor. This node switches between VCC and PGND at the switching frequency.

Ground, GND

This ground is used for the majority of the device including the analog reference, control loop, and other circuits.

Power Ground, PGND

This is a separate power ground connection used for the low-side synchronous switch, to isolate switching noise from the rest of the device. (Figure 24)

Enable, EN

This is the input terminal to activate the regulator. The input threshold is TTL/CMOS compatible. It also has an internal pull-up to ensure a stable state if the pin is disconnected.

Power Good Output, PG

This is an open drain output. During start-up the FB input is monitored and the PG line remains low, until the FB voltage reaches the V_{OUT_UV} threshold. A 10KΩ resistor to VOUT is required for pull-up. Once the internal comparator detects that the FB voltage is above the desired threshold, an internal delay timer is activated and the PG line is de-asserted to high once this delay timer expires. In the event of a fault, when the FB voltage decreases below $V_{OUT\_UV,}$ the PG line asserts low and remains low until the FB input exceeds V_{OUT_UV} and the delay timer times out. See Figure 3 for the control of the PG signal.

Internal Protection Details

Internal Current Limit

The high-side NMOS current is sensed on a cycle by cycle basis and if current limit is reached, the IC truncates the high-side on-time. The device also senses the FB pin to identify hard output shorts or extended over-current conditions. It then directs the VSW output to skip 4 cycles and frequency will foldback to 250KHz, if current limit occurs when FB is low. This allows current built up in the inductor during the minimum on time to decay sufficiently. Current limit is always active when the regulator is enabled. Soft start ensures current limit does not prevent regulator startup.

Once the over current condition is removed, the device returns to normal operation automatically. (Alternately the factory can configure the device to shutdown the regulator if an extended over current event is detected, which requires a toggle of the Enable pin to return the device to normal operation. Contact Semtech Marketing for specific information.)

Thermal Shutdown

If the die temperature exceeds 170°C (typical), the VSW outputs will tri-state to protect the device from damage. The PG and all other protection circuitry stay active to inform the system of the failure mode. Once the device cools to 160°C (typical), the device will start up again, following the normal soft start sequence. If the die again reaches 170°C, the shutdown/restart sequence will repeat.

Reference Soft Start

The reference in this device is ramped at a rate of 4ms to prevent the output from overshoot during startup. This ramp restarts whenever there is a rising edge sensed on the Enable pin. This occurs in both the fixed and adjustable versions. During the soft start ramp, current limit is still active, and will still protect the device in case of a short on the output.

Output Overvoltage

If the FB input exceeds 103% of the regulation voltage, the VSW outputs will tri-state to protect the device from damage. This check occurs at the start of each switching cycle. If it occurs during the middle of a cycle, the switching for that cycle will complete, and the VSW outputs will tri-state at the beginning of the next cycle.

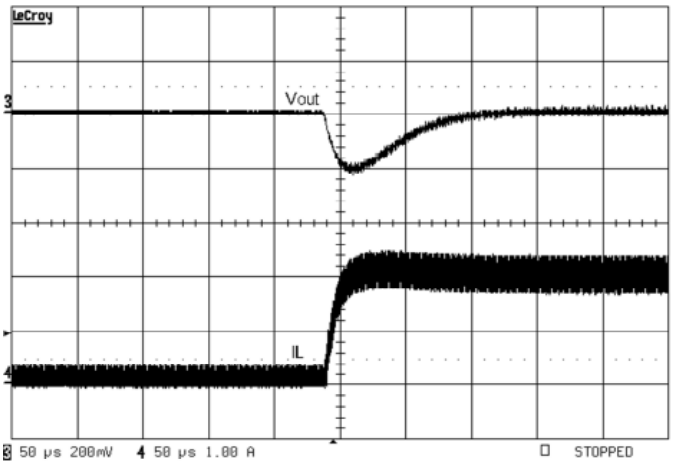
VCC Under-Voltage Lockout

The device is held in the off state until VCC reaches 4.5V (typical). There is a 500mV hysteresis on this input, which requires the input to fall below 4.0V (typical) before the device will disable.

Transient Response

TS30011/12/13 has been designed to work under a wide range of input and output voltages, supporting different values and types of output capacitance. By design, the TS30011/12/13 has a lower control loop bandwidth. For designs with a high slew rate load requirement, using a 1nF feed-forward capacitor C_{FF} (Figure 23) in parallel with R_{TOP} feedback resistor is recommended. A typical response is shown in Figure 22.

Figure 22. 100mA to 2A Load Step
(Load Slew Rate=2.5A/us, V_{CC}=12V, V_{OUT}=4V)



Typical Application Schematic

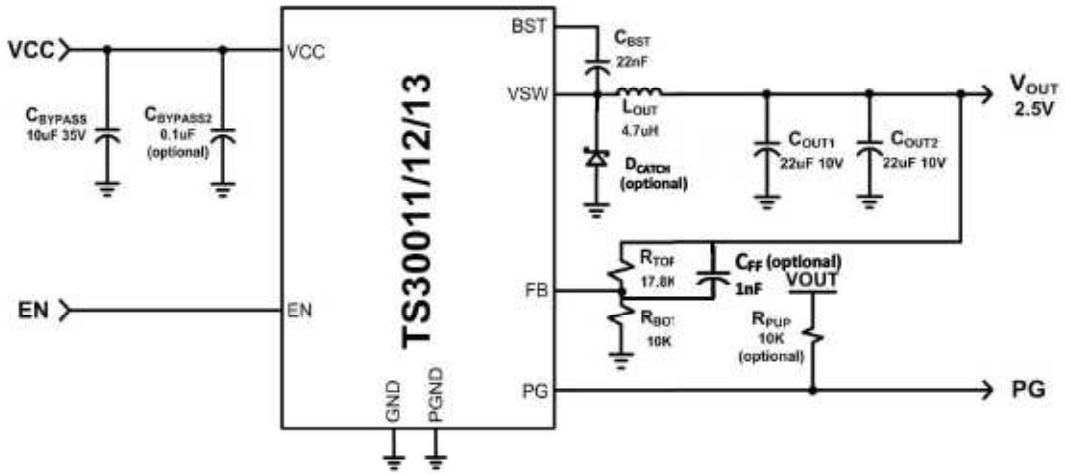


Figure 23: TS30011/12/13 Application Schematic

A minimal schematic suitable for most applications is shown on page 1. Figure 23 includes optional components that may be considered to address specific issues as listed in the External Component Selection section.

PCB Layout

For proper operation and minimum EMI, care must be taken during PCB layout. An improper layout can lead to issues such as poor stability and regulation, noise sensitivity and increased EMI radiation. (Figure 24) The main guidelines are the following:

- provide low inductive and resistive paths for loops with high di/dt or high dV/dt,
- provide low capacitive paths with respect to all the other nodes for traces with high di/dt or high dV/dt,
- sensitive nodes not assigned to power transmission should be referenced to the analog signal ground (GND) and should always be separated from the power ground (PGND).

The negative ends of C_{BYPASS}, C_{OUT} and the Schottky diode D_{CATCH} (optional) should be placed close to each other and connected using a wide trace. Vias must be used to connect the PGND node to the ground plane. The PGND node must be placed as close as possible to the TS30011/12/13 PGND pins to avoid additional voltage drop in traces.

The bypass capacitor C_{BYPASS} (optionally paralleled to a 0.1µF capacitor, $C_{BYPASS2}$) must be placed close to the VCC pins of TS30011/12/13.

The inductor must be placed close to the VSW pins and connected directly to C_{OUT} in order to minimize the area between the VSW pin, the inductor, the C_{OUT} capacitor and the PGND pins. The trace area and length of the switching nodes VSW and BST should be minimized.

For the adjustable output voltage version of the TS30011/12/13, feedback resistors R_{BOT} and R_{TOP} are required for Vout settings greater than 0.9V and should be placed close to the TS30011/12/13 in order to keep the traces of the sensitive node FB as short as possible and away from switching signals. R_{BOT} should be connected to the analog ground pin (GND) directly and should never be connected to the ground plane. The analog ground trace (GND) should be connected in only one point to the power ground (PGND). A good connection point is under the TS30011/12/13 package to the exposed thermal pad and vias which are connected to PGND. R_{TOP} will be connected to the V_{OUT} node using a trace that ends close to the actual load.

For fixed output voltage versions, R_{BOT} and R_{TOP} are not required and the FB pin should connect directly to V_{OUT}.

PCB Layout - continued

The exposed thermal pad must be soldered to the PCB for mechanical reliability and to achieve good power dissipation. Vias must be placed under the pad to transfer the heat to the ground plane.

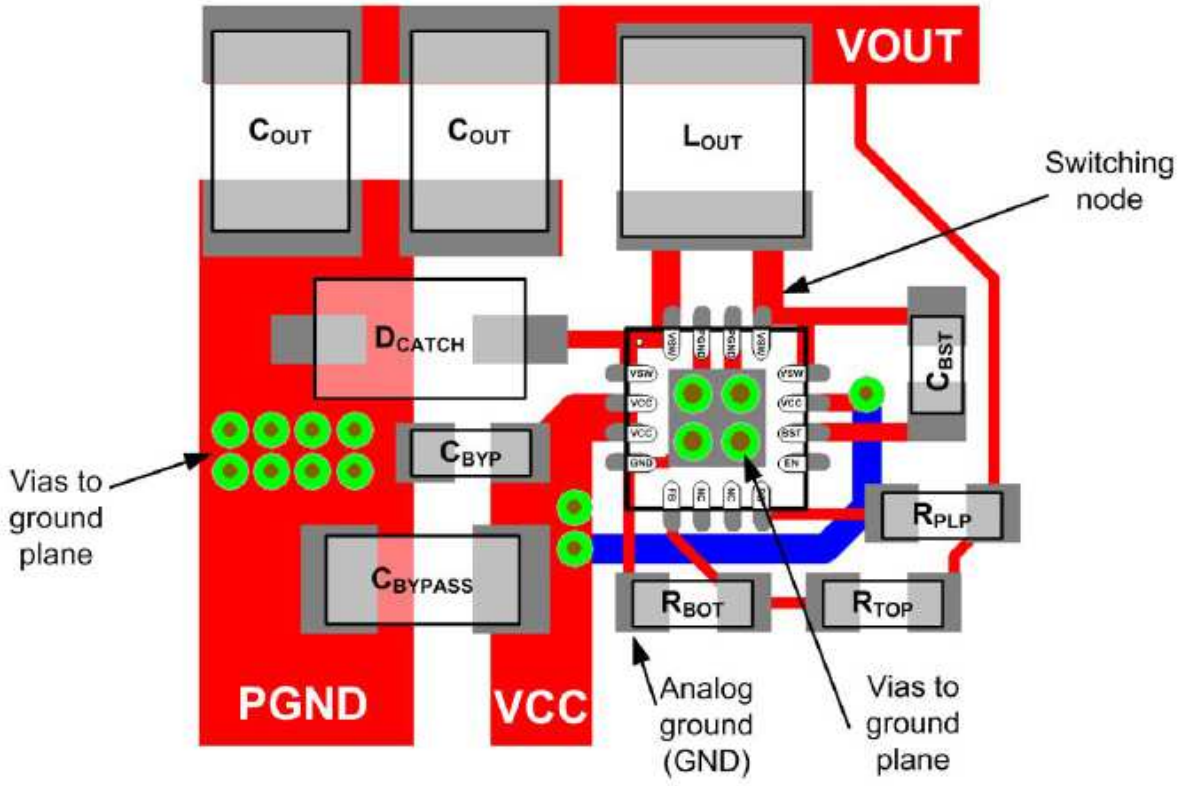


Figure 24: TS30011/12/13 PCB Layout, Top View

External Component Bill of Materials

Designator	Function	Description	Suggested Manufacturer	Manufacturer Code	Qty
C_{BYPASS}	Input Supply Bypass Capacitor	10uF 10% 35V	TDK	CGA5L3X5R1V106K160AB	1
C_{OUT}	Output Filter Capacitor	22uF 10% 10V	TDK	C2012X5R1A226K125AB	2
L_{OUT}	Output Filter Inductor (1A)	4.7uH 2A	TDK Wurth	SLF7045T-4R7M2R0-PF 7447745047	1
L_{OUT}	Output Filter Inductor (2A)	4.7uH 3A	TDK Wurth	VLC5045T-4R7M 744774047	1
L_{OUT}	Output Filter Inductor (3A)	4.7uH 4.37A	TDK Wurth	VLP6045LT-4R7M 744777004	1
C_{BST}	Boost Capacitor	15nF-200nF 10V	TDK	C1005X7R1C223K	1

Note 1: Assumes 16LD 3x3 QFN with hi-K JEDEC board and 13.5 inch2 of 1 oz Cu and 4 thermal vias connected to PAD

External Component Bill of Materials continued

Designator	Function	Description	Suggested Manufacturer	Manufacturer Code	Qty
R_{TOP}	Voltage Feedback Resistor (optional)	17.8K (Note 1)			1
R_{BOT}	Voltage Feedback Resistor (optional)	10K (Note 1)			1
R_{PLP}	PG Pin Pull-up Resistor (optional)	10K			1
D_{CATCH}	Catch Diode (optional, 1A)	30V 2A SOD-123FL	On Semiconductor	MBR230LSFT1G	1
D_{CATCH}	Catch Diode (optional, 2A)	40V 3A SOD-123	NXP Semiconductors	PMEG4030ER,115	1
D_{CATCH}	Catch Diode (optional, 3A)	40V 5A SOD-123FL	NXP Semiconductors	PMEG4050EP,1	1

Note 1: The voltage divider resistor values are calculated for an output voltage of 2.5V. For fixed output versions, the FB pin is connected directly to V_{OUT}.

External Component Selection

The 1MHz internal switching frequency of the TS30011/12/13 facilitates low cost LC filter combinations. Additionally, the fixed output versions enable a minimum external component count to provide a complete regulator with only 4 external components: an input bypass capacitor, an inductor, an output capacitor, and the bootstrap capacitor. The internal compensation is optimized for a 44uF output capacitor and a 4.7uH inductor.

For best performance, a low ESR ceramic capacitor should be used for C_{BYPASS}. If C_{BYPASS} is not a low ESR ceramic capacitor, a 0.1uF ceramic capacitor should be added in parallel to C_{BYPASS}.

The minimum allowable value for the output capacitor is 33uF. To keep the output ripple low, a low ESR (less than 35mOhm) ceramic is recommended. Multiple capacitors can be paralleled to reduce the ESR.

The inductor range is 4.7uH +/-20%. For optimal over-current protection, the inductor should be able to handle up to the regulator current limit without saturation. Otherwise, an inductor with a saturation current rating higher than the maximum IOUT load requirement plus the inductor current ripple should be used.

For high current applications, the optional Schottky diode D_{CATCH} improves overall efficiency and reduces heat. It is up to the user to determine the cost/benefit of adding this additional component in the user's application. The diode is typically not needed.

For the adjustable output versions, the output voltage can be adjusted by sizing R_{TOP} and R_{BOT} feedback resistors. The equation for the output voltage is

$$Vout = 0.9 \cdot \left(1 + \left(\frac{R_{TOP}}{R_{BOT}}\right)\right)$$

For the adjustable version, the ratio of VCC/Vout cannot exceed 16.

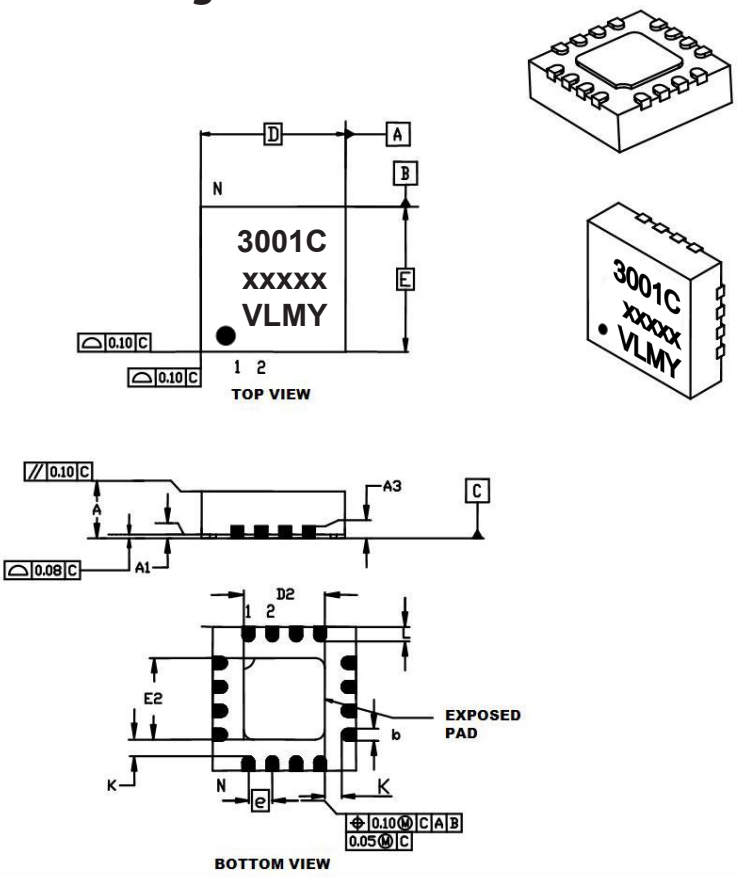
R_{PLP} is only required when the Power Good signal (PG) is utilized.

Thermal Information

TS30011/12/13 is designed for a maximum operating junction temperature Tj of 125°C. The maximum output power is limited by the power losses that can be dissipated over the thermal resistance given by the package and the PCB structures. The PCB must provide heat sinking to keep the TS30011/12/13 cool. The exposed metal on the bottom of the QFN package must be soldered to a ground plane. This ground should be tied to other copper layers with multiple thermal vias. Adding more copper to the top and the bottom layers and tying this copper to the internal planes with vias can reduce thermal resistance further. For a hi-K JEDEC

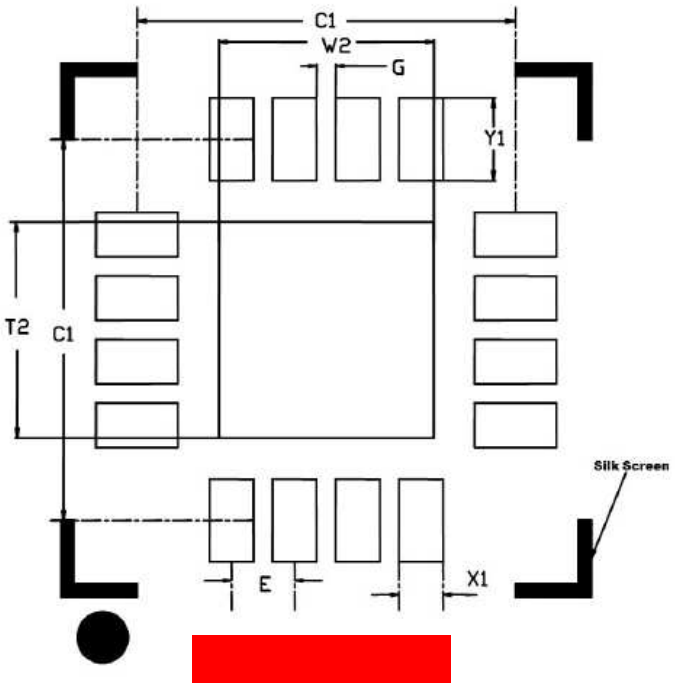
board and 13.5 square inch of 1 oz Cu, the thermal resistance from junction to ambient can be reduced to θ_{JA} = 38°C/W. The power dissipation of other power components (catch diode, inductor) cause additional copper heating and can further increase what the TS30011/12/13 sees as ambient temperature.

Package Mechanical Drawings (all dimentions in mm)



Units		Millimeters		
Dimensions Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Width	E2	1.55	1.70	1.80
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.55	1.70	1.80
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.30	0.40
Contact-to-Exposed Pad	K	0.20	-	-

Recommended PCB Land Pattern



Dimensions in Millimeters

Units		Millimeters		
Dimensions Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2	-	-	1.70
Optional Center Pad Length	T2	-	-	1.70
Contact Pad Spacing	C1	-	3.00	-
Contact Pad Spacing	C2	-	3.00	-
Contact Pad Width (X16)	X1	-	-	0.35
Contact Pad Length (X16)	Y1	-	-	0.65
Distance Between Pads	G	0.15	-	-

Notes:
Dimensions and tolerances per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact values shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information only.

Packaging Information

Pb-Free (RoHS): The TS30011/12/13 devices are fully compliant for all materials covered by European Union Directive 2011/65/EU (RoHS 2), and meet all IPC-1752 Class 5 & 6 materials declaration requirements. These devices are Pb Free, WEEE, and low Halogen.

MSL, Peak Temp: The TS30011/12/13 family has a Moisture Sensitivity Level (MSL) 1 rating per JEDEC J-STD-020D. These devices also have a Peak Profile Solder Temperature (Tp) of 260°C.

Ordering Information

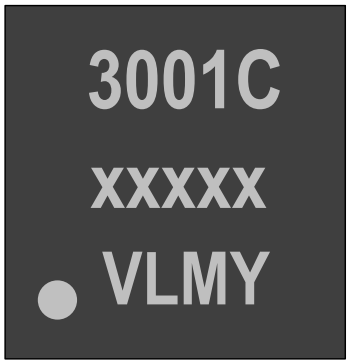
TS3001x-MvvvQFNR

x	Output Current
1	1 Amp
2	2 Amp
3	3 Amp

vvv	Output Voltage
015	1.5 V
018	1.8 V
025	2.5 V
033	3.3 V
050	5.0 V
000	Adjustable

Ordering Information

Top Mark



Top Mark: Legend

Mark Method	Laser	
Font Size:	25 Mils	
Line 1 Marking:	**3001C**	Current Level - TS30011 = 1, TS30012 = 2, TS30013 = 3 (Example: C = y for part number TS3001y-M0xxQFNR)
Line 2 Marking:	**XXXXX**	Last five digits of Lot Number, non fractional
Line 3 Marking:	**o**	Pin 1 Mark
	VL	Voltage Level; 15 - 1.5V; 18 - 1.8V; 25 - 2.5V; 33 - 3.3V, 50 - 5.0V; 00 - 0V (Example: VL = xx for part number TS3001y-M0xxQFNR)
	M	Month Code: Jan-Sept 1-9, Oct - A, Nov - B, Dec - C
	Y	Year Code: A - 2011, B - 2012, C - 20013, ...

Contact Information

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