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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

TS3005

A 1.55V to 5.25V, 1.35µA, 1.7ms to 33hrs Silicon Timer

FEATURES

- ♦ Ultra Low Supply Current: 1.35µA at 49Hz
- ♦ Supply Voltage Operation: 1.55V to 5.25V
- ♦ Single Resistor Sets FOUT at 50% Duty Cycle
- ♦ 3-pin User-Programmable FOUT Period:
  - 1.7ms ≤ t_{FOUT} ≤ 33hrs
- ♦ FOUT Period Accuracy: 3%
- ♦ FOUT Period Drift: 0.02%/ºC
- ♦ Single Resistor Sets Output Frequency
- ♦ Separate PWM Control and Buffered Output
- ♦ FOUT/PWMOUT Output Driver Resistance: 160Ω

APPLICATIONS

Portable and Battery-Powered Equipment
Low-Parts-Count Nanopower Oscillator
Compact Micropower Replacement for Crystal and Ceramic Oscillators
Micropower Pulse-width Modulation Control
Micropower Pulse-position Modulation Control
Micropower Clock Generation
Micropower Sequential Timing

DESCRIPTION

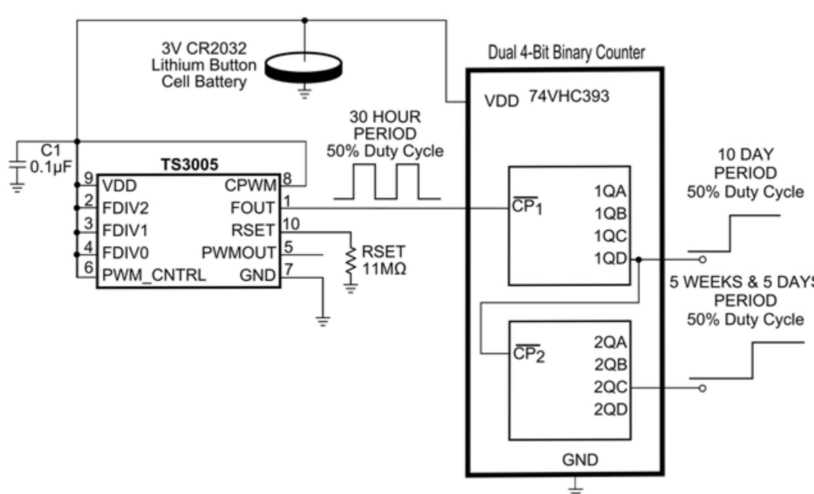
The TS3005 is a single-supply, second-generation oscillator/timer fully specified to operate at a supply voltage range of 1.55V to 5.25V while consuming less than 1.5µA(max) supply current. Requiring only a resistor to set the base output frequency (or output period) at 49Hz (or 20.5ms) with a 50% duty cycle, the TS3005 timer/oscillator is compact, easy-to-use, and versatile. Optimized for ultra-long life, low frequency, battery-powered/portable applications, the TS3005 joins the TS3001, TS3002, TS3003, TS3004, and TS3006 in the CMOS timer family of "NanoWatt Analog™" high-performance analog integrated circuits.

The TS3005 output period can be user-adjusted from 1.7ms to 33hrs without additional components. In addition, the TS3005 represents a 25% reduction in pcb area and a factor-of-10 lower power consumption over other CMOS-based integrated circuit oscillators/timers. When compared against industry-standard 555-timer-based products, the TS3005 offers up to 84% reduction in pcb area and over three orders of magnitude lower power consumption.

The TS3005 is fully specified over the -40°C to +85°C temperature range and is available in a low-profile, 10-pin 3x3mm TDFN package with an exposed back-side paddle.

TYPICAL APPLICATION CIRCUIT

TS3005, 5 Weeks and 5 Days Counter Circuit



ABSOLUTE MAXIMUM RATINGS

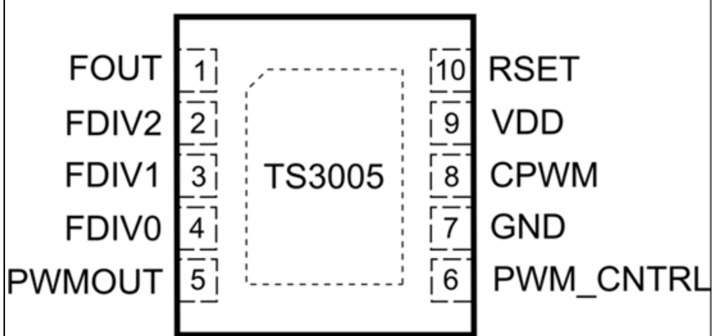
V_{DD} to GND...-0.3V to +5.5V
PWM_CNTRL to GND...-0.3V to +5.5V
FOUT, PWMOUT to GND...-0.3V to +5.5V
RSET to GND..-0.3V to +2.5V
CPWM to GND..-0.3V to +5.5V
FDIV to GND...-0.3V to +5.5V

Continuous Power Dissipation (T_A = +70°C)
10-Pin TDFN (Derate at 13.48mW/°C above +70°C)... 1078mW
Operating Temperature Range................................ -40°C to +85°C
Storage Temperature Range................................. -65°C to +150°C
Lead Temperature (Soldering, 10s).................................... +300°C

Electrical and thermal stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to any absolute maximum rating conditions for extended periods may affect device reliability and lifetime.

PACKAGE/ORDERING INFORMATION

TOP VIEW



3mm x 3mm x 0.75mm DFN-EP 10L
TD1033 Package

ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TS3005ITD1033	3005I	Tape & Reel	-----
TS3005ITD1033T		Tape & Reel	3000

Lead-free Program: Silicon Labs supplies only lead-free packaging.

Consult Silicon Labs for products specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

V_{DD} = 3V, V_{PWM_CNTRL}= V_{DD}, R_{SET} = 4.32MΩ, $R_{LOAD(FOUT)}$ = Open Circuit, $C_{LOAD(FOUT)}$ = 0pF, $C_{LOAD(PWM)}$ = 0pF, C_{PWM} = 47pF, FDIV2:0 = 000 unless otherwise noted. Values are at T_A = 25°C unless otherwise noted. See Note 1.

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}			1.55		5.25	V
Supply Current	I_{DD}	CPWM = V_{DD}			1.35	1.5	µA
			-40°C ≤ T_A ≤ 85°C			1.9	
					1.47	1.7	
			-40°C ≤ T_A ≤ 85°C			2.1	
FOUT Period	t_{FOUT}			19.95	20.5	21.05	ms
			-40°C ≤ T_A ≤ 85°C	19.4		21.5	
FOUT Period Line Regulation	$\Delta t_{FOUT}/V$	1.55V ≤ V_{DD} ≤ 5.25V			0.17		%/V
FOUT Duty cycle				49		51	%
FOUT Period Temperature Coefficient	$\Delta t_{FOUT}/\Delta T$				0.02		%/°C
PWMOUT Duty Cycle	DC(PWMOUT)			0.08		0.12	%
		V_{PWM_CNTRL}= 0V		0.02		0.03	
PWMOUT Duty Cycle Line Regulation	ΔDC(PWMOUT)/V	1.55V < V_{DD} < 5.25V, FDIV2:0 = 000			-3		%
C_{PWM} Sourcing Current	I_{CPWM}	FDIV2:0 = 000, 001		930		1050	nA
			-40°C ≤ T_A ≤ 85°C	810		1150	
		FDIV2:0 ≠ 000, 001			97		nA
UVLO Hysteresis	V_{UVLO}	(V_{DD}=1.55V) – ($V_{DD\_SHUTDOWN\ VOLTAGE}$)		150		250	mV
FOUT, PWMOUT Rise Time	t_{RISE}	See Note 2, C_L = 15pF			10		ns
FOUT, PWMOUT Fall Time	t_{FALL}	See Note 2, C_L = 15pF			10		ns
FOUT Jitter		See Note 3			0.001		%
RSET Pin Voltage	V(RSET)				0.3		V
FDIV Input Current	I_{FDIV}					10	nA
			-40°C ≤ T_A ≤ 85°C			20	
Maximum Oscillator Frequency	Fosc	RSET= 360K				586	Hz
High Level Output Voltage, FOUT and PWMOUT	V_{DD} - V_{OH}	I_{OH} = 1mA			160		mV
Low Level Output Voltage, FOUT and PWMOUT	V_{OL}	I_{OL} = 1mA			140		mV
Dead Time	T_{DT}	FOUT edge falling and PWMOUT edge rising			106		ns

Note 1: All devices are 100% production tested at T_A = +25°C and are guaranteed by characterization for T_A = T_{MIN} to T_{MAX}, as specified.

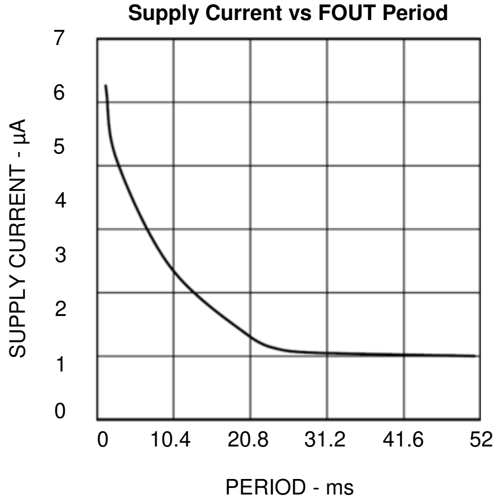
Note 2: Output rise and fall times are measured between the 10% and 90% of the V_{DD} power-supply voltage levels. The specification is based on lab bench characterization and is not tested in production.

Note 3: Timing jitter is the ratio of the peak-to-peak variation of the period to the mean of the period. The specification is based on lab bench characterization and is not tested in production.

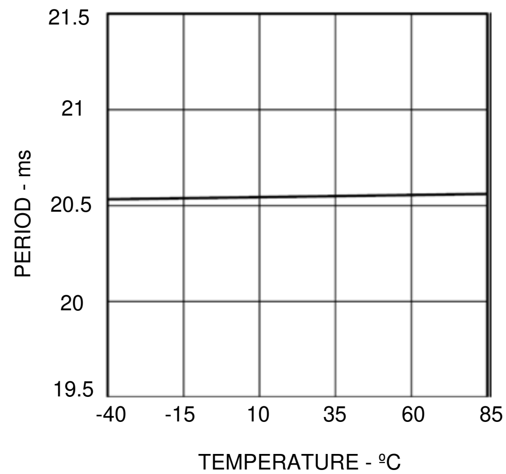
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 3V, V_{PWM_CNTRL}= V_{DD}, R_{SET} = 4.32MΩ, $R_{LOAD(FOUT)}$ = Open Circuit, $C_{LOAD(FOUT)}$ = 0pF, $C_{LOAD(PWM)}$ = 0pF, CPWM = V_{DD}, FDIV2:0 = 000 unless otherwise noted. Values are at T_A = 25°C unless otherwise noted.

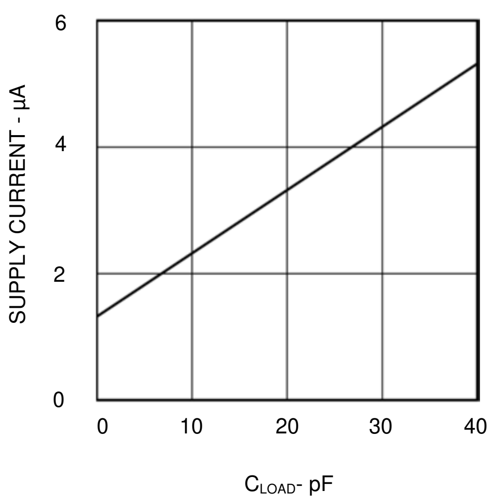
Supply Current vs FOUT Period



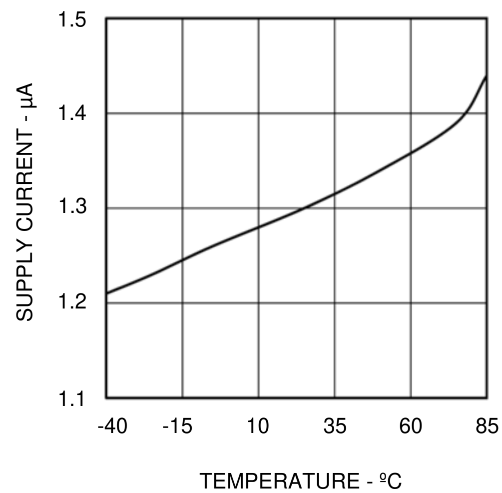
FOUT Period vs Temperature



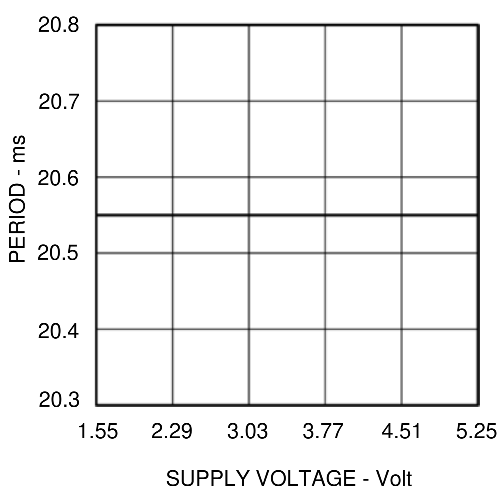
Supply Current vs $C_{LOAD(FOUT)}$



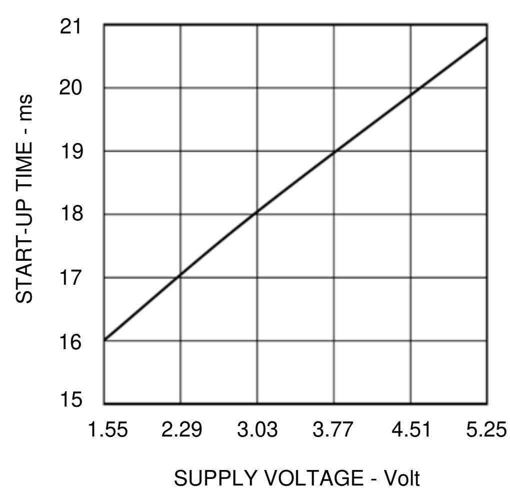
Supply Current vs Temperature



FOUT Period vs Supply Voltage



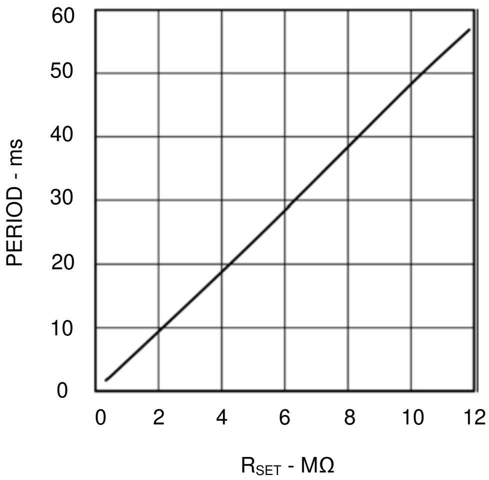
Start-up Time vs Supply Voltage



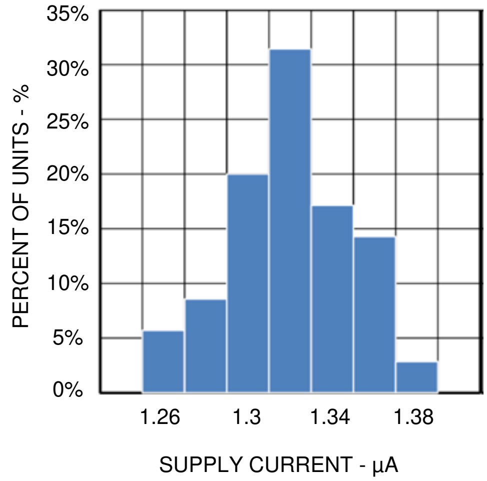
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 3V, V_{PWM_CNTRL}= V_{DD}, R_{SET} = 4.32MΩ, $R_{LOAD(FOUT)}$ = Open Circuit, $C_{LOAD(FOUT)}$ = 0pF, $C_{LOAD(PWM)}$ = 0pF, CPWM = V_{DD}, FDIV2:0 = 000 unless otherwise noted. Values are at T_A = 25°C unless otherwise noted.

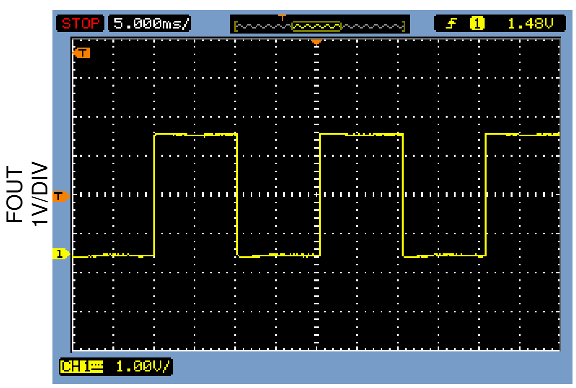
Period vs R_{SET}



Supply Current Distribution

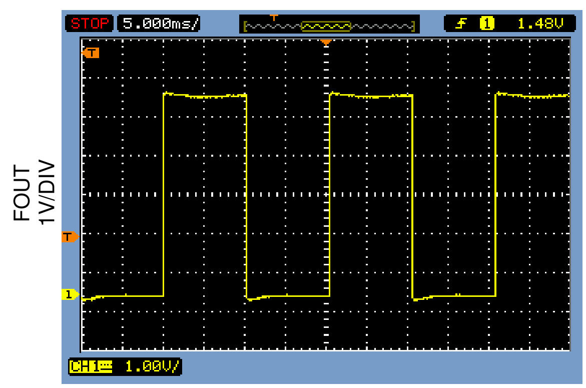


FOUT
V_{DD} = 3V, C_{LOAD} = 15pF



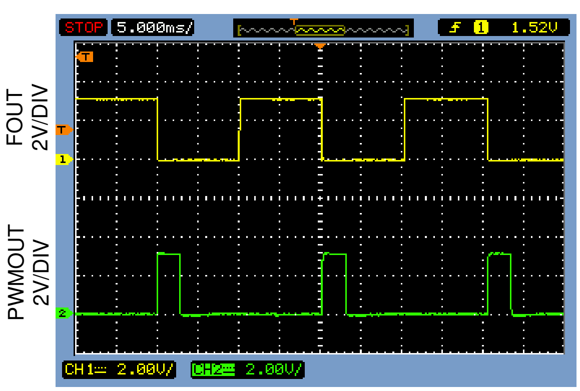
5ms/DIV

FOUT
V_{DD} = 5V, C_{LOAD} = 15pF



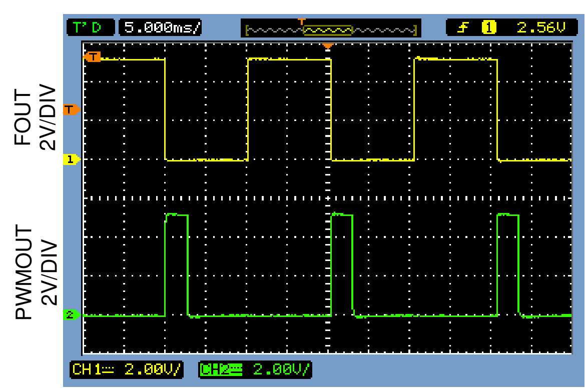
5ms/DIV

FOUT and PWMOUT
V_{DD} = 3V, C_{LOAD} = 15pF, $V_{PWM\ CNTRL}$= V_{DD}, C_{PWM} = 10nF



5ms/DIV

FOUT and PWMOUT
V_{DD} = 5V, C_{LOAD} = 15pF, $V_{PWM\ CNTRL}$= V_{DD}, C_{PWM} = 10nF

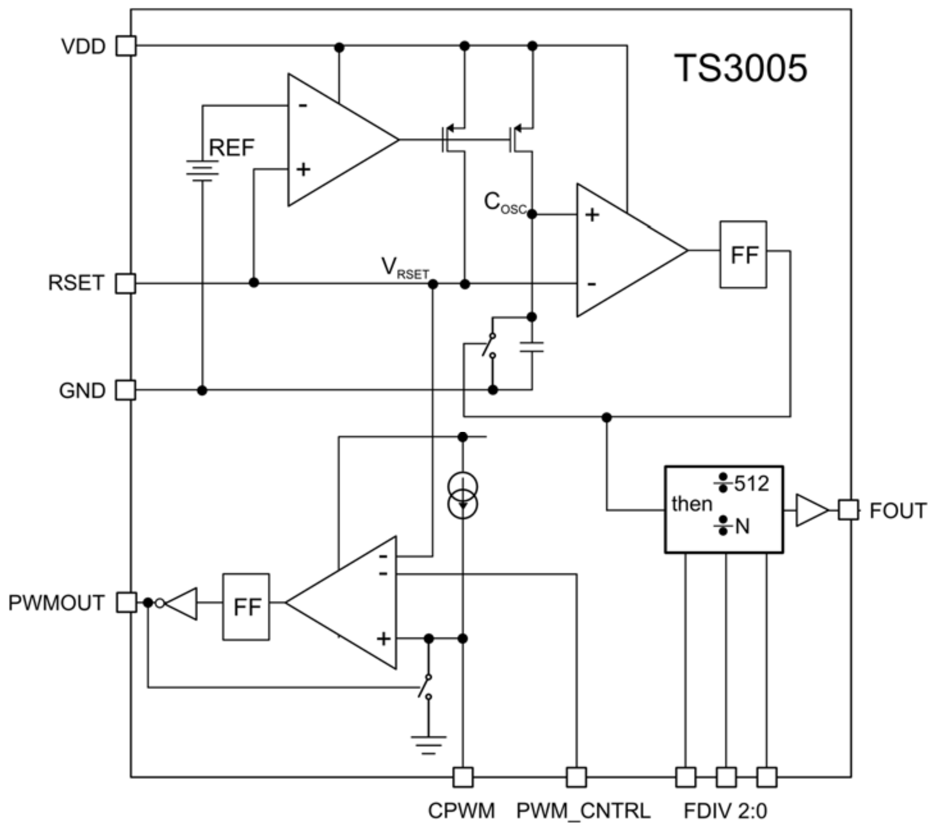


5ms/DIV

PIN FUNCTIONS

PIN	NAME	FUNCTION
1	FOUT	Fixed Frequency Output. A push-pull output stage with an output resistance of 160Ω. FOUT pin swings from GND to VDD. For lowest power operation, capacitance loads should be minimized and resistive loads should be maximized.
2,3,4	FDIV2:0	Frequency Divider Input. Various combinations of these inputs will change the FOUT frequency for a fixed value of RSET. Refer to Table 1.
5	PWMOUT	Pulse-width Modulated Output. A push-pull output stage with an output resistance of 160Ω, the PWMOUT pin is wired anti-phase with respect to FOUT and swings from GND to VDD. For lowest power operation, capacitance loads should be minimized and resistive loads should be maximized.
6	PWM_CNTRL	PWM Output Pulse Control Pin. Applying a voltage between GND and V_{RSET} will reduce the duty cycle of the PWMOUT output that is set by the capacitor connected to the CPWM pin. Connect PWM_CNTRL to VDD for fixed PWMOUT output pulse time (determined only by capacitor at CPWM).
7	GND	Ground. Connect this pin to the system's analog ground plane.
8	CPWM	PWMOUT Pulse Width Programming Capacitance Input. A target capacitance connected from this pin to GND sets the duty cycle of the PMW output. Minimize any stray capacitance on this pin. The voltage on this pin will swing from GND to V_{RSET}. Connect CPWM to VDD to disable PWM function (saves PWM current).
9	VDD	Power Supply Voltage Input. The supply voltage range is $1.55V \leq V_{DD} \leq 5.25V$. Bypass this pin with a 0.1uF ceramic coupling capacitor in close proximity to the TS3005.
10	RSET	FOUT Programming Resistor Input. A 4.32MOhm resistor connected from this pin to ground sets the T3005's internal oscillator's output period to 20ms (49Hz). For optimal performance, the composition of the RSET resistor shall be consistent with a tolerance of 1% or lower. The RSET pin voltage is approximately 0.3V.

BLOCK DIAGRAM



FDIV 2:0	t_{FOUT}(s)	FOUT (Hz)	I_{CPWM} (A)
000	1.7ms-56.88ms	586-17.578	1µ
001	13.65ms-455.16ms	73.25-2.197	1µ
010	109.17ms-3.64	9.16-0.2746	100n
011	877.19ms-29.15	1.14-0.0343	100n
100	7.01-233.1	0.143-0.00429	100n
101	55.94-31.09min	0.0178-0.536mHz	100n
110	7.49min-4.146hrs	0.0022-0.0670mHz	100n
111	59.67min-33.1hrs	0.279mHz-8.381µHz	100n

Table 1: FOUT and PWMOUT Frequency Range per FDIV2:0 Combination

THEORY OF OPERATION

The TS3005 is a user-programmable oscillator where the period of the square wave at its FOUT terminal is generated by an external resistor connected to the RSET pin. The output period is given by:

$$t_{FOUT}\ (s) = \frac{8^{FDIV2:0} \times RSET \times 512}{1.08E11}$$

Equation 1. FOUT Frequency Calculation where FDIV2:0 = 0 to 7

With an R_{SET} = 4.32MΩ and FDIV2:0=111, the FOUT period is approximately 715.88 minutes with a 50% duty cycle. As design aids, Tables 2 lists TS3004's typical FOUT period for various standard values for R_{SET} and FDIV2:0 = 111(7).

The output period can be user-adjusted from 1.7ms to 33hrs without additional components. Frequency divider inputs FDIV2:0 can be set to a logic state HIGH or LOW in order to set the desired frequency as shown in to Table 1.

The TS3005 also provides a separate PWM output signal at its PWMOUT terminal that is anti-phase with respect to FOUT. A dead time of approximately 106ns exists between FOUT and PWMOUT. To adjust the pulse width of the PWMOUT output, a single capacitor can be placed at the CPWM pin. To determine the capacitance needed for a desired pulse width, the following equation is to be used:

$$CPWM(F) = \frac{\text{Pulse Width(s)} \times I_{CPWM}}{V_{CPWM} \cong 300mV}$$

Equation 2. CPWM Capacitor Calculation

where I_{CPWM} and V_{CPWM} is the current supplied and voltage applied to the CPWM capacitor, respectively. The pulse width is determined based on the period of FOUT and should never be greater than the period at FOUT. Make sure the PWM_CNTRL pin is set to at least 400mV when calculating the pulse width of PWMOUT. Note V_{CPWM} is approximately 300mV, which is the RSET voltage. Also note that I_{CPWM} is either 1µA or 100nA. Refer to Table 1.

The PWMOUT output pulse width can be adjusted further after selecting a CPWM capacitor This can be achieved by applying a voltage to the PWM_CNTRL pin between V_{RSET} and GND. With a voltage of at least V_{RSET}, the pulse width is set based on Equation 2. For example, with a period of 20.5ms(49Hz) a 10nF capacitor at the CPWM pin generates a pulse width of approximately 3ms. This can be calculated

R_{SET} (MΩ)	t_{FOUT}
0.360	59.67min
1	1.09hrs
2.49	6.87hrs
4.32	11.93hrs
6.81	18.81hrs
9.76	26.93hrs
12	33.1hrs

Table 2: t_{FOUT} vs R_{SET} for FDIV2:0 = 111(7)

using equation 2. By reducing the PWM_CNTRL voltage from V_{RSET} ≅ 300mV to GND, the pulse width can be reduced further. Note that as the FOUT frequency increases, the amount of pulse width reduction reduces and vice versa. Furthermore, if the PWMOUT output is half the frequency of the FOUT output, this means your CPWM capacitor is too large and as a result, the pulse width is greater than the FOUT period. In this case, use Equation 2 and reduce the capacitor value to less than the period. Connect CPWM to VDD to disable the PWM function and in turn, save power. Connect PWM_CNTRL to VDD for a fixed PWMOUT output pulse width, which is determined by the CPWM pin capacitor only.

APPLICATIONS INFORMATION

Minimizing Power Consumption

To keep the TS3005's power consumption low, resistive loads at the FOUT and PWMOUT terminals increase dc power consumption and therefore should be as large as possible. Capacitive loads at the FOUT and PWMOUT terminals increase the TS3005's transient power consumption and, as well, should be as small as possible.

One challenge to minimizing the TS3005's transient power consumption is the probe capacitance of oscilloscopes and frequency counter instruments. Most instruments exhibit an input capacitance of 15pF or more. Unless buffered, the increase in transient load current can be as much as 400nA.

To minimize capacitive loading, the technique shown

$$C_{EXT} = \frac{1}{\frac{1}{C_{LOAD(EFF)}} \quad \frac{1}{C_{PROBE}}}$$

Equation 3: External Capacitor Calculation

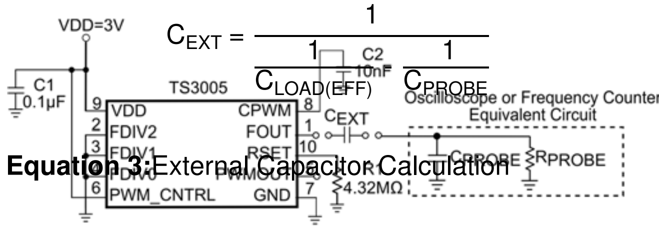


Figure 1: Using an External Capacitor in Series with Probes Reduces Effective Capacitive Load.

in Figure 1 can be used. In this circuit, the principle of series-connected capacitors can be used to reduce the effective capacitive load at the TS3005's FOUT and PWMOUT terminals.

For example, if the instrument's input probe capacitance is 15pF and the desired effective load capacitance at either or both FOUT and PWMOUT terminals is to be ≤5pF, then the value of C_{EXT} should be ≤7.5pF.

To determine the optimal value for C_{EXT} once the probe capacitance is known by simply solving for C_{EXT} using the following expression:

TS3005 Start-up Time

As the TS3005 is powered up, its FOUT terminal (and PWMOUT terminal, if enabled) is active once the applied VDD is higher than 1.55V. Once the applied VDD is higher than 1.55V, the master oscillator achieves steady-state operation within 18ms.

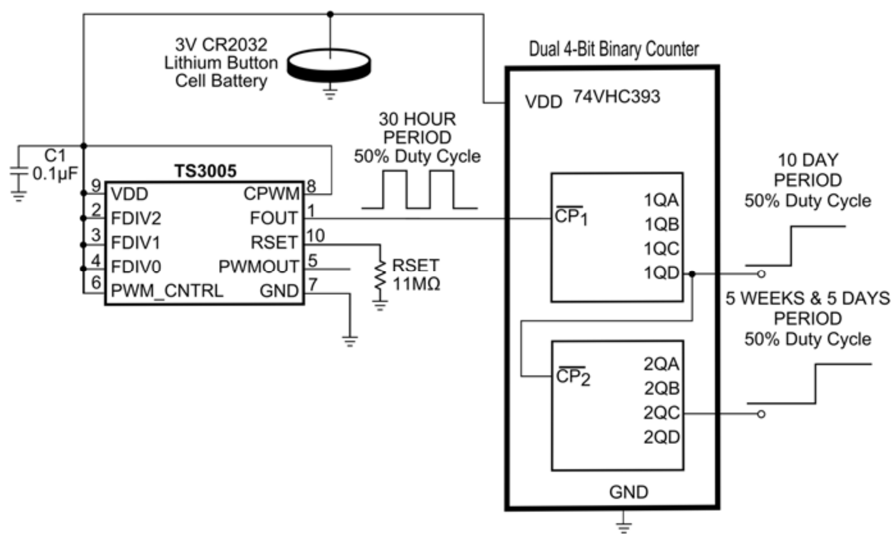


Figure 2: 5 Weeks and 5 Days Counter Circuit

5 Weeks and 5 Days Counter Circuit with TS3005

The TS3005 can be configured into a 5 Weeks and 5 Days counter as shown in Figure 2. The circuit is composed of a TS3005 timer and a dual 74VHC393 4-bit counter. The TS3005 divider inputs are set to FDIV2:0 = 111. With an RSET of 11MΩ, the FOUT period is approximately 30 hours. The complete circuit consumes approximately 4.5µA and is powered with a single 3V CR2032 lithium button cell battery. If a shorter period is desired, a 10 day period is available via output 1QD.

Divide the PWMOUT Output Frequency by Two with the TS3005

Using a single resistor and capacitor, the TS3005 can be configured to a divide by two circuit as shown in Figure 3. To achieve a divide by two function with the TS3005, the pulse width of the PWMOUT output must be at least a factor of 2 greater than the period set at FOUT by resistor RSET. The CPWM capacitor selected must meet this pulse width requirement and

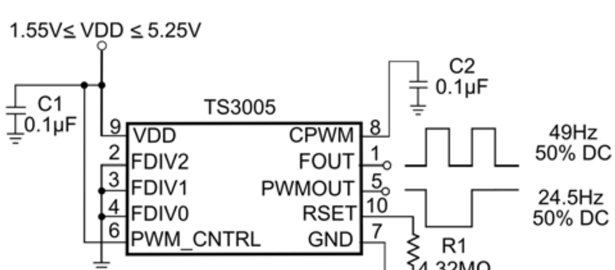


Figure 3: Configuring the TS3005 into a Divide by Two Frequency Divider

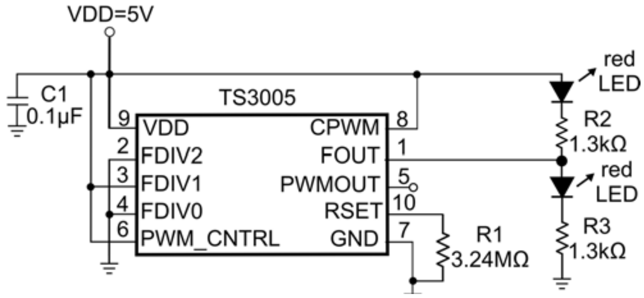


Figure 4: Flashing Railroad Lights with the TS3005

can be calculated using Equation 2. In Figure 3, a value of 4.32MΩ for RSET sets the FOUT output period to 20.5ms. A CPWM capacitor of 0.1µF was chosen, which sets the pulse width of PWMOUT to approximately 30ms. This is well above the required minimum pulse width of 20.5ms.

Flashing Railroad Lights with the TS3005

With only three resistors and two off the shelf LEDs, the TS3005 can be configured into a flashing railroad lights circuit. With the input divider set to FDIV2:0 = 010 and RSET= 3.24MΩ, the FOUT output frequency is 1Hz. Refer to Figure 4. During the time the output is HIGH, only the pull-down LED is on while when the output is LOW, only the pull-up LED is on. The supply voltage of the circuit is 5V.

Using the TS3005 and a Potentiometer to Dim an LED

The TS3005 can be configured to dim an LED by modulating the pulse width of the PWMOUT output. With the input divider set to FDIV2:0 = 000 and RSET= 2MΩ, the FOUT output frequency is approximately 100Hz (or 10ms period). Refer to Figure 5. The CPWM capacitor was calculated using Equation 2 with a pulse width of 8.1ms. To reduce the pulse width from 8.1ms and in turn, dim the LED, a 1MΩ potentiometer is used. The potentiometer is connected to the PWM_CNTRL pin in a voltage divider configuration. The supply voltage of the circuit is 5V.

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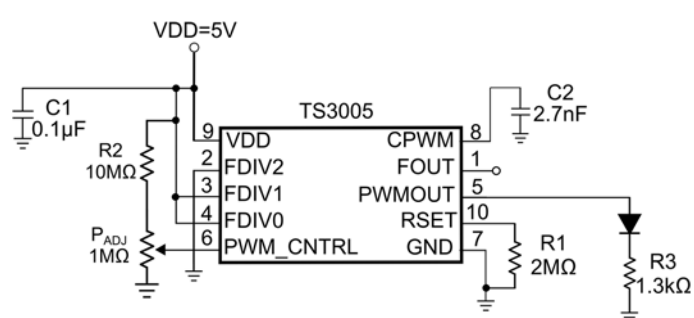
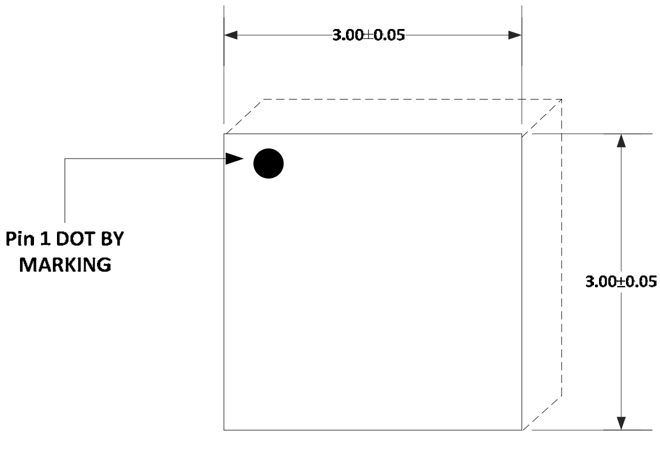


Figure 5: TS3005 Configured to Dim an LED with a Potentiometer

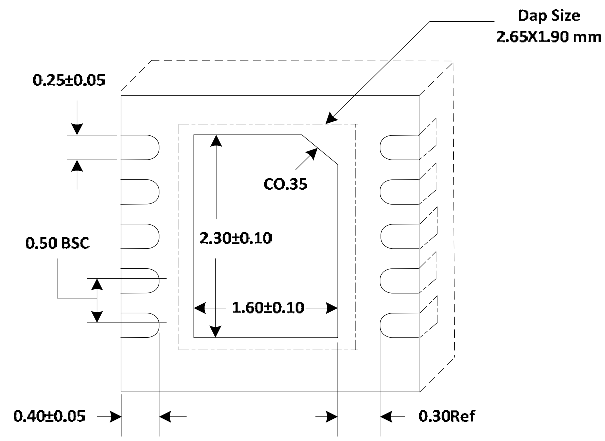
PACKAGE OUTLINE DRAWING

10-Pin TDFN33 Package Outline Drawing

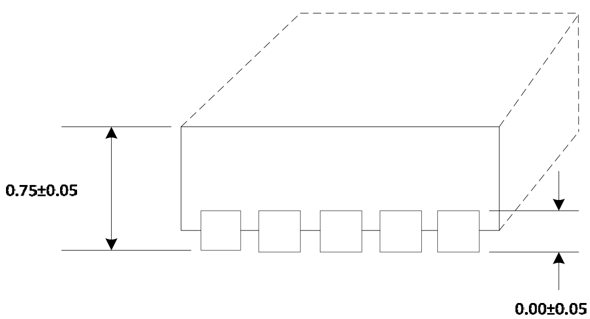
(N.B., Drawings are not to scale)



TOP VIEW



BOTTOM VIEW



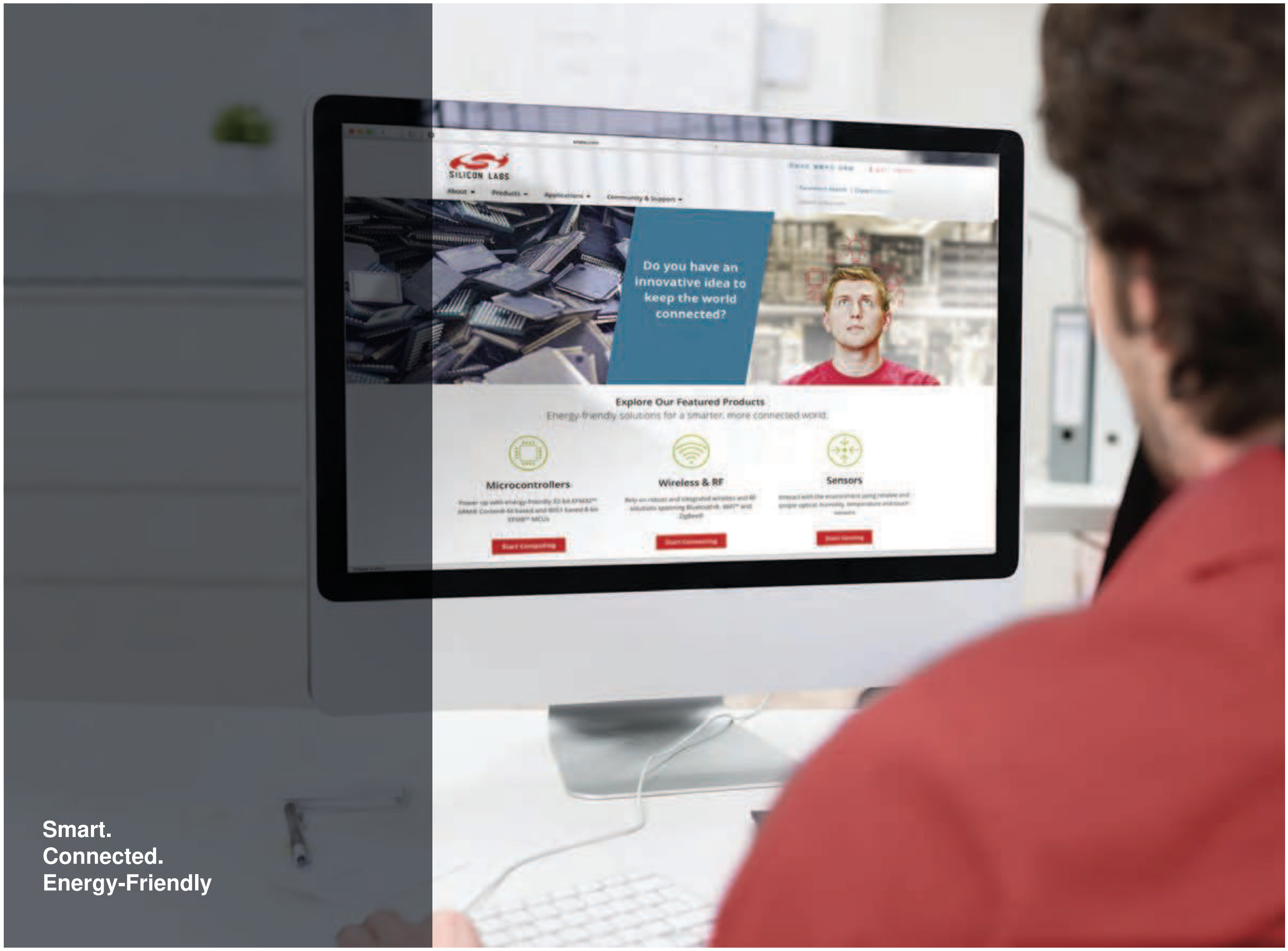
SIDE VIEW

NOTE!

- **All dimensions in mm.**
- **Compliant with JEDEC MO-229**

Patent Notice

Silicon Labs invests in research and development to help our customers differentiate in the market with innovative low-power, small size, analog-intensive mixed-signal solutions. Silicon Labs' extensive patent portfolio is a testament to our unique approach and world-class engineering team.



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