TS3006

A 1.55V to 5.25V, 1.9μA, 9kHz to 300kHz Silicon Timer

FEATURES

- Ultra Low Supply Current: 1.9μA at 25kHz
- Supply Voltage Operation: 1.55V to 5.25V
- Single Resistor Sets FOUT at 50% Duty Cycle
- FOUT Period:
    - 9kHz ≤ FOUT ≤ 300kHz
- Single Resistor Sets Output Frequency
- FOUT Period Accuracy: 3%
- FOUT Period Drift: 0.02%/ºC
- FOUT Output Driver Resistance: 160Ω

APPLICATIONS

Portable and Battery-Powered Equipment
Low-Parts-Count Nanopower Oscillator
Compact Micropower Replacement for Crystal and Ceramic Oscillators
Micropower Pulse-width Modulation Control
Micropower Pulse-position Modulation Control
Micropower Clock Generation
Micropower Sequential Timing

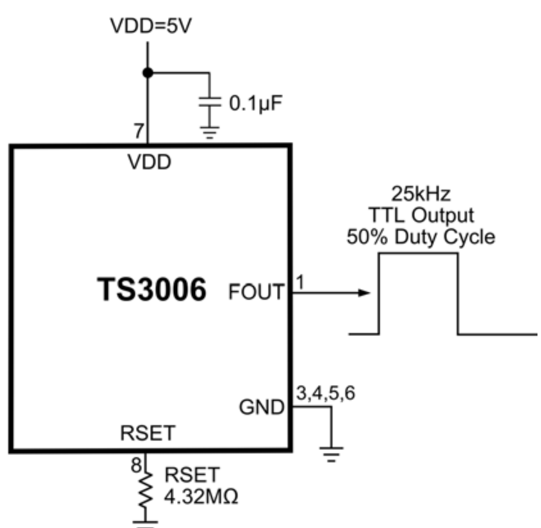
DESCRIPTION

The TS3006 is a single-supply, second-generation oscillator/timer fully specified to operate at a supply voltage range of 1.55V to 5.25V while consuming less than 2.4μA(max) supply current. Requiring only a resistor to set the base output frequency (or output period) at 25kHz (or 40μs) with a 50% duty cycle, the TS3006 timer/oscillator is compact, easy-to-use, and versatile. Optimized for ultra-long life, low frequency, battery-powered/portable applications, the TS3006 joins the TS3001, TS3002, TS3004, and TS3005 in the CMOS timer family of “NanoWatt Analog™” high-performance analog integrated circuits.

The TS3006 output frequency can be user-adjusted from 9kHz to 300kHz with a single resistor. In addition, the TS3006 represents a 25% reduction in pcb area and a factor-of-10 lower power consumption over other CMOS-based integrated circuit oscillators/timers. When compared against industry-standard 555-timer-based products, the TS3006 offers up to 84% reduction in pcb area and over three orders of magnitude lower power consumption.

The TS3006 is fully specified over the -40°C to +85°C temperature range and is available in a low-profile, 8-pin 3x3mm TDFN package with an exposed back-side paddle.

TYPICAL APPLICATION CIRCUIT



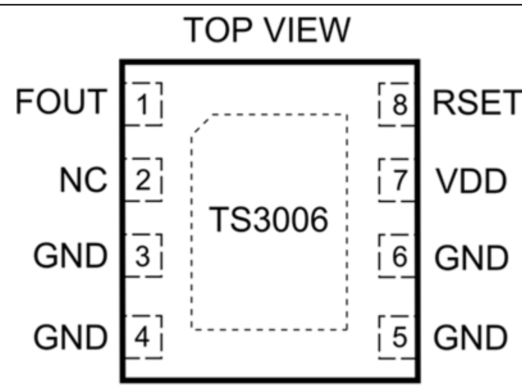
ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND...-0.3V to +5.5V
PWM_CNTRL to GND...-0.3V to +5.5V
FOUT, PWMOUT to GND...-0.3V to +5.5V
RSET to GND..-0.3V to +2.5V
CPWM to GND..-0.3V to +5.5V
FDIV to GND...-0.3V to +5.5V

Continuous Power Dissipation (T_A = +70°C)
8-Pin TDFN (Derate at 23.8mW/°C above +70°C)....... 1951mW
Operating Temperature Range................................ -40°C to +85°C
Storage Temperature Range................................. -65°C to +150°C
Lead Temperature (Soldering, 10s)..................................... +300°C

Electrical and thermal stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to any absolute maximum rating conditions for extended periods may affect device reliability and lifetime.

PACKAGE/ORDERING INFORMATION



3mm x 3mm x 0.75mm DFN-EP 8L
TD833 Package

ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TS3006ITD833	3006I	Tape & Reel	-----
TS3006ITD833T		Tape & Reel	3000

Lead-free Program: Silicon Labs supplies only lead-free packaging.

Consult Silicon Labs for products specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

V_{DD} = 3V, V_{PWM_CNTRL}= V_{DD}, R_{SET} = 4.32MΩ, $R_{LOAD(FOUT)}$ = Open Circuit, $C_{LOAD(FOUT)}$ = 0pF unless otherwise noted. Values are at T_A = 25°C unless otherwise noted. See Note 1.

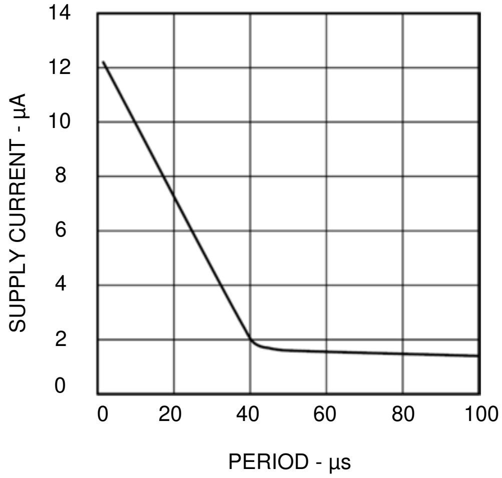
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}			1.55		5.25	V
Supply Current	I_{DD}				1.9	2.4	µA
			-40°C ≤ T_A ≤ 85°C			2.7	
FOUT Period	t_{FOUT}			39	40.1	41.2	µs
			-40°C ≤ T_A ≤ 85°C	38		42	
FOUT Period Line Regulation	$\Delta t_{FOUT}/V$	1.55V ≤ V_{DD} ≤ 5.25V			0.17		%/V
FOUT Duty cycle				49		51	%
FOUT Period Temperature Coefficient	$\Delta t_{FOUT}/\Delta T$				0.02		%/°C
UVLO Hysteresis	V_{UVLO}	(V_{DD}=1.55V) – ($V_{DD\_SHUTDOWN\ VOLTAGE}$)		150		250	mV
FOUT Rise Time	t_{RISE}	See Note 2, C_L = 15pF			10		ns
FOUT Fall Time	t_{FALL}	See Note 2, C_L = 15pF			10		ns
FOUT Jitter		See Note 3			0.001		%
RSET Pin Voltage	V(RSET)				0.3		V
Maximum Oscillator Frequency	Fosc	RSET= 360K				300	kHz
High Level Output Voltage, FOUT	V_{DD} - V_{OH}	I_{OH} = 1mA			160		mV
Low Level Output Voltage, FOUT	V_{OL}	I_{OL} = 1mA			140		mV

Note 1: All devices are 100% production tested at T_A = +25°C and are guaranteed by characterization for T_A = T_{MIN} to T_{MAX}, as specified.
Note 2: Output rise and fall times are measured between the 10% and 90% of the V_{DD} power-supply voltage levels. The specification is based on lab bench characterization and is not tested in production.
Note 3: Timing jitter is the ratio of the peak-to-peak variation of the period to the mean of the period. The specification is based on lab bench characterization and is not tested in production.

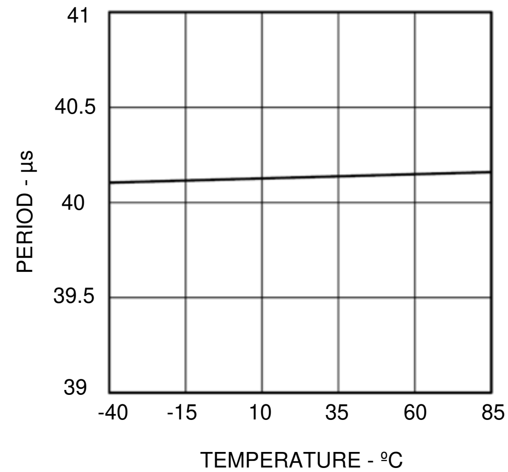
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 3V, V_{PWM_CNTRL}= V_{DD}, R_{SET} = 4.32MΩ, $R_{LOAD(FOUT)}$ = Open Circuit, $C_{LOAD(FOUT)}$ = 0pF unless otherwise noted. Values are at T_A = 25°C unless otherwise noted.

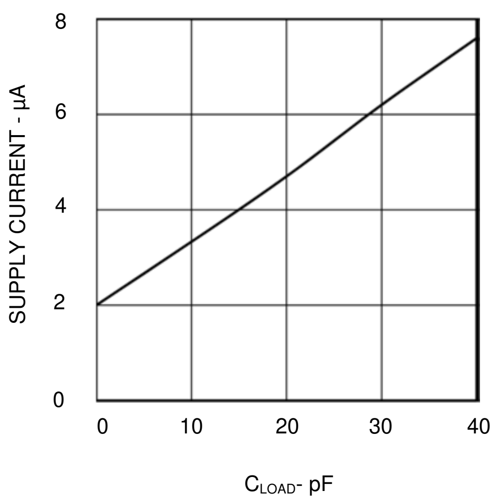
Supply Current vs FOUT Period



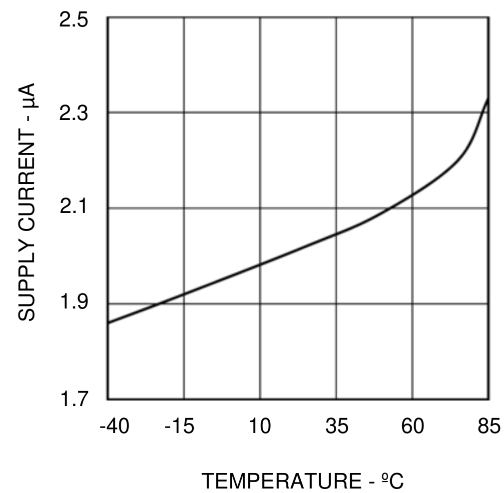
FOUT Period vs Temperature



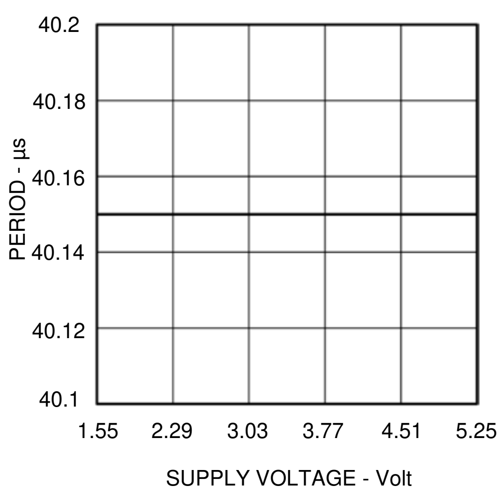
Supply Current vs $C_{LOAD(FOUT)}$



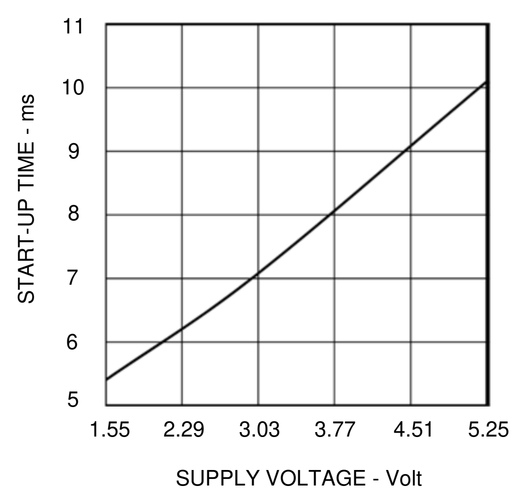
Supply Current vs Temperature



FOUT Period vs Supply Voltage



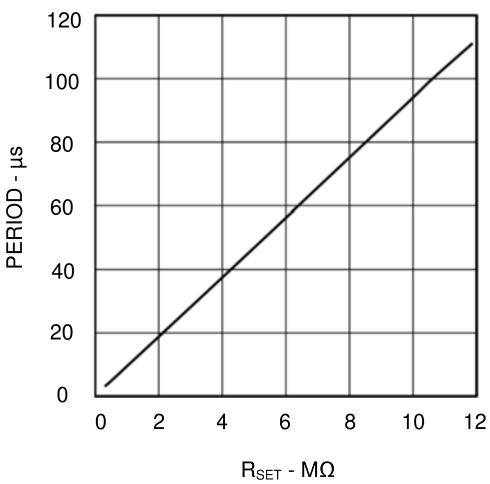
Start-up Time vs Supply Voltage



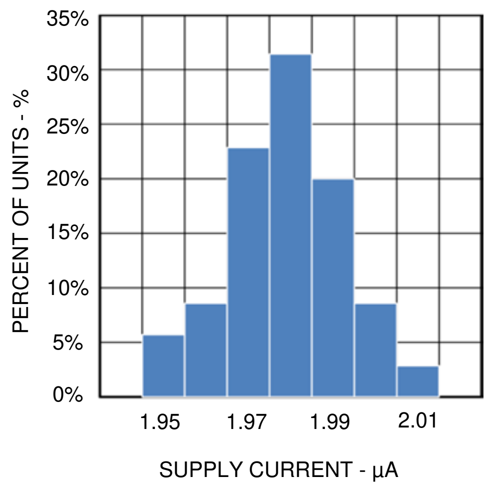
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 3V, V_{PWM_CNTRL}= V_{DD}, R_{SET} = 4.32MΩ, $R_{LOAD(FOUT)}$ = Open Circuit, $C_{LOAD(FOUT)}$ = 0pF unless otherwise noted. Values are at T_A = 25°C unless otherwise noted.

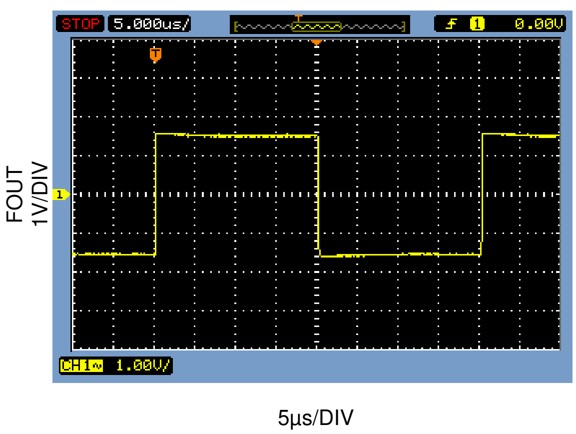
Period vs R_{SET}



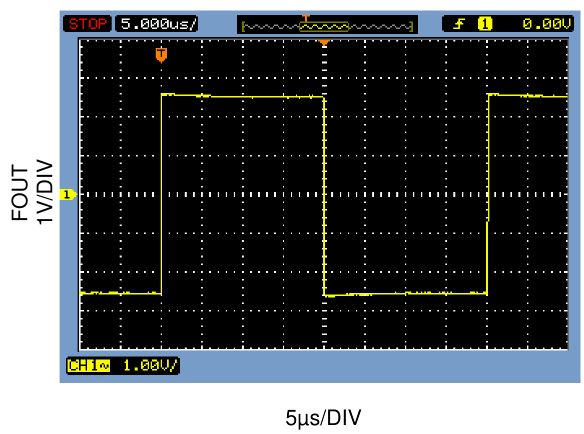
Supply Current Distribution



FOUT
V_{DD} = 3V, C_{LOAD} = 15pF



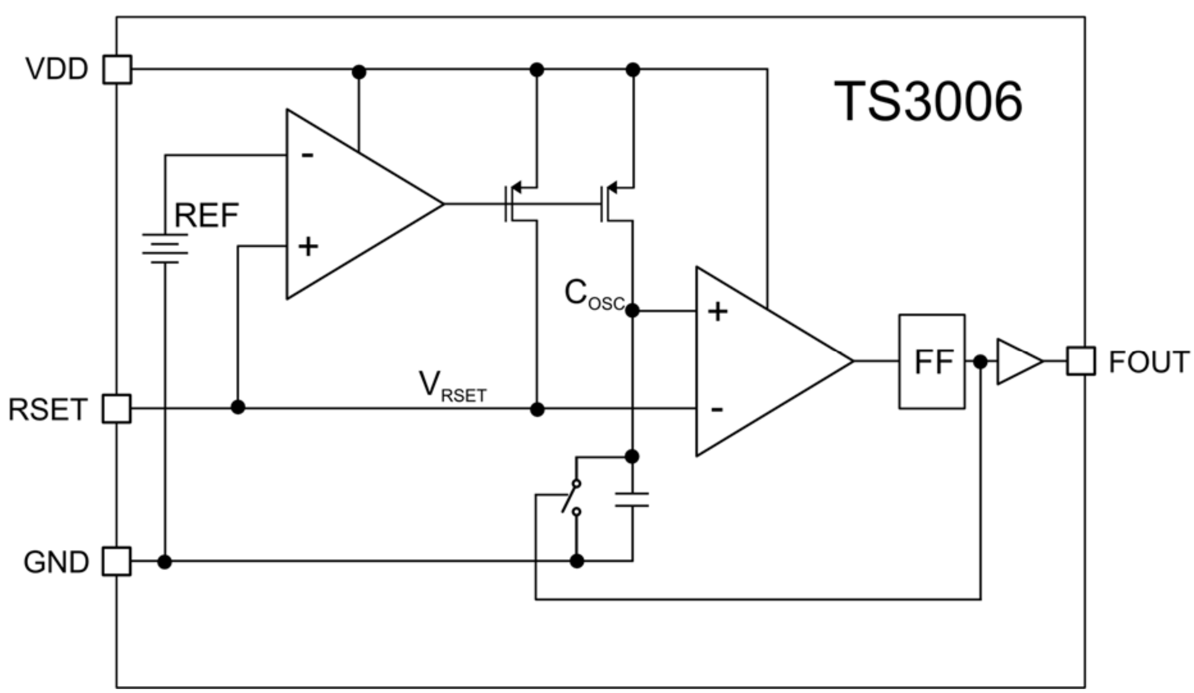
FOUT
V_{DD} = 5V, C_{LOAD} = 15pF



PIN FUNCTIONS

PIN	NAME	FUNCTION
1	FOUT	Fixed Frequency Output. A push-pull output stage with an output resistance of 160Ω. FOUT pin swings from GND to VDD. For lowest power operation, capacitance loads should be minimized and resistive loads should be maximized.
2	NC	Non-Connect.
3,4,5,6	GND	Ground. Connect this pin to the system's analog ground plane.
7	VDD	Power Supply Voltage Input. The supply voltage range is $1.55V \leq V_{DD} \leq 5.25V$. Bypass this pin with a 0.1uF ceramic coupling capacitor in close proximity to the TS3006.
8	RSET	FOUT Programming Resistor Input. A 4.32MOhm resistor connected from this pin to ground sets the T3003's internal oscillator's output period to 40µs (25KHz). For optimal performance, the composition of the RSET resistor shall be consistent with a tolerance of 1% or lower. The RSET pin voltage is approximately 0.3V.

BLOCK DIAGRAM



THEORY OF OPERATION

The TS3006 is a user-programmable oscillator where the period of the square wave at its FOUT terminal is generated by an external resistor connected to the RSET pin. The output frequency is given by:

$$\text{FOUT (kHz)} = \frac{1.08E11}{\text{RSET}}$$

Equation 1. FOUT Frequency Calculation

With an R_{SET} = 4.32MΩ, the output frequency is approximately 25kHz with a 50% duty cycle. As design aids, Tables 1 lists TS3006's typical FOUT for various standard values for R_{SET}.

R_{SET} (MΩ)	FOUT (kHz)
0.360	300
1	108
2.49	43.37
4.32	25
6.81	15.86
9.76	11.07
12	9

Table 1: FOUT vs R_{SET}

Connect CPWM to VDD to disable the PWM function and in turn, save power. Connect PWM_CNTRL to VDD for a fixed PWMOUT output pulse width, which is determined by the CPWM pin capacitor only.

APPLICATIONS INFORMATION

Minimizing Power Consumption

To keep the TS3006's power consumption low, resistive loads at the FOUT and PWMOUT terminals increase dc power consumption and therefore should be as large as possible. Capacitive loads at the FOUT and PWMOUT terminals increase the TS3006's transient power consumption and, as well, should be as small as possible.

One challenge to minimizing the TS3006's transient power consumption is the probe capacitance of oscilloscopes and frequency counter instruments. Most instruments exhibit an input capacitance of 15pF or more. Unless buffered, the increase in transient load current can be as much as 400nA.

To minimize capacitive loading, the technique shown in Figure 1 can be used. In this circuit, the principle of series-connected capacitors can be used to reduce the effective capacitive load at the TS3006's FOUT and PWMOUT terminals.

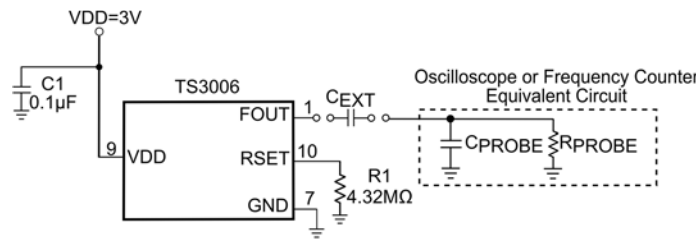


Figure 1: Using an External Capacitor in Series with Probes Reduces Effective Capacitive Load.

To determine the optimal value for C_{EXT} once the probe capacitance is known by simply solving for C_{EXT} using the following expression:

$$C_{EXT} = \frac{1}{\frac{1}{C_{LOAD(EFF)}} - \frac{1}{C_{PROBE}}}$$

Equation 2: External Capacitor Calculation

For example, if the instrument's input probe capacitance is 15pF and the desired effective load capacitance at either or both FOUT and PWMOUT terminals is to be ≤5pF, then the value of C_{EXT} should be ≤7.5pF.

TS3006 Start-up Time

As the TS3006 is powered up, its FOUT terminal (and PWMOUT terminal, if enabled) is active once the applied VDD is higher than 1.55V. Once the applied VDD is higher than 1.55V, the master oscillator achieves steady-state operation within 8ms.

Using a Potentiometer to Trim the TS3006's Output Frequency

By using a fixed resistor and a potentiometer, the output frequency of the TS3006 can be trimmed as shown in Figure 2. By selecting a fixed resistor R1 with a tolerance of 0.1% and a potentiometer P1 with a 5% tolerance, the output frequency can be trimmed to provide a ±2% trimming range

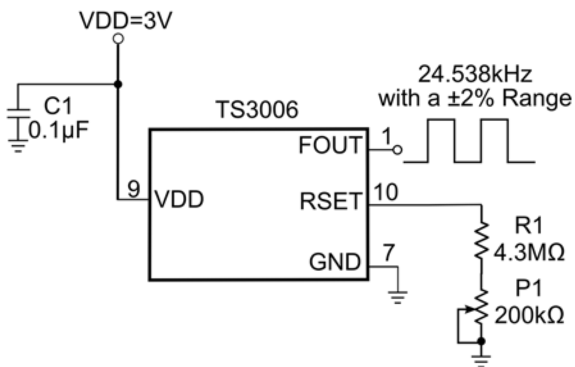
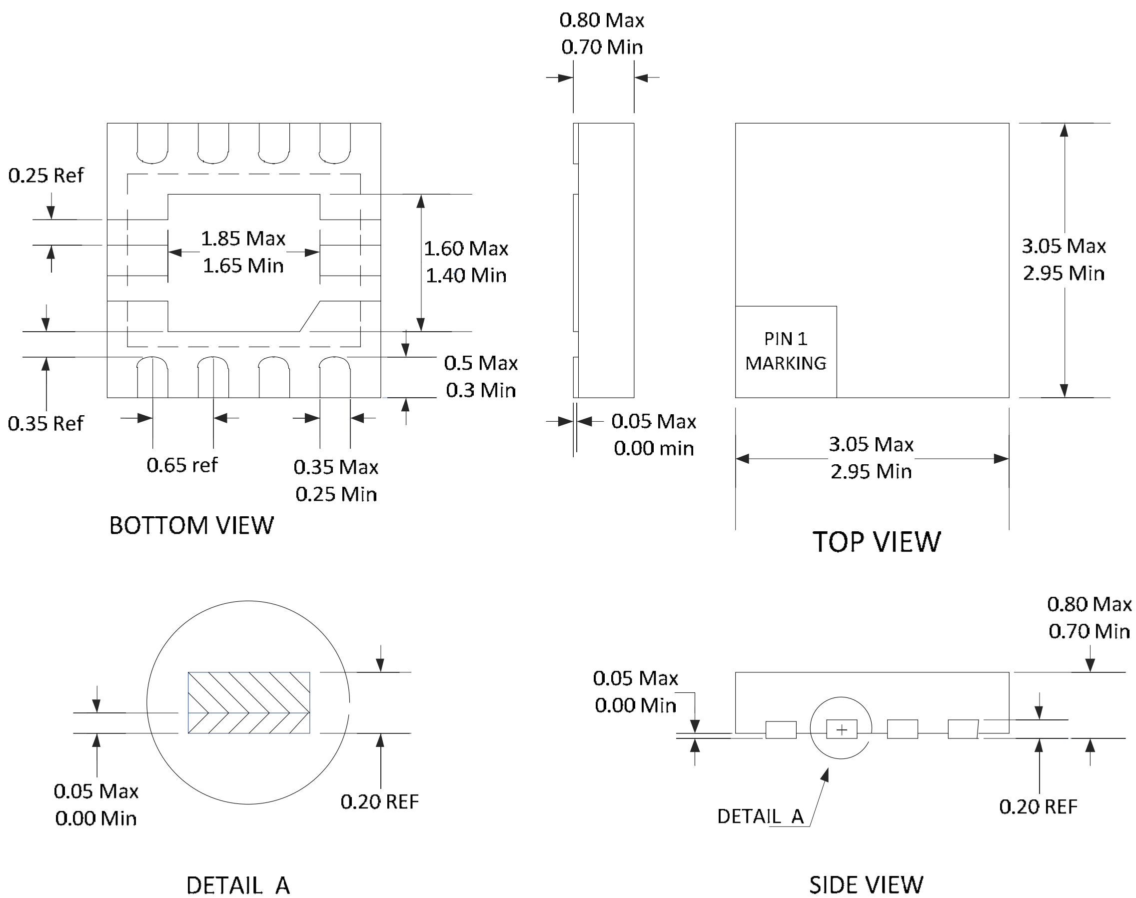


Figure 2: Using a Fixed Resistor and a Potentiometer to Trim the TS3006's Output Frequency.

PACKAGE OUTLINE DRAWING

8-Pin TDFN33 Package Outline Drawing

(N.B., Drawings are not to scale)



NOTE: CONTROLLING DIMENTIONS IN MILIMETERS
Compliant with JEDEC MO-229

Patent Notice

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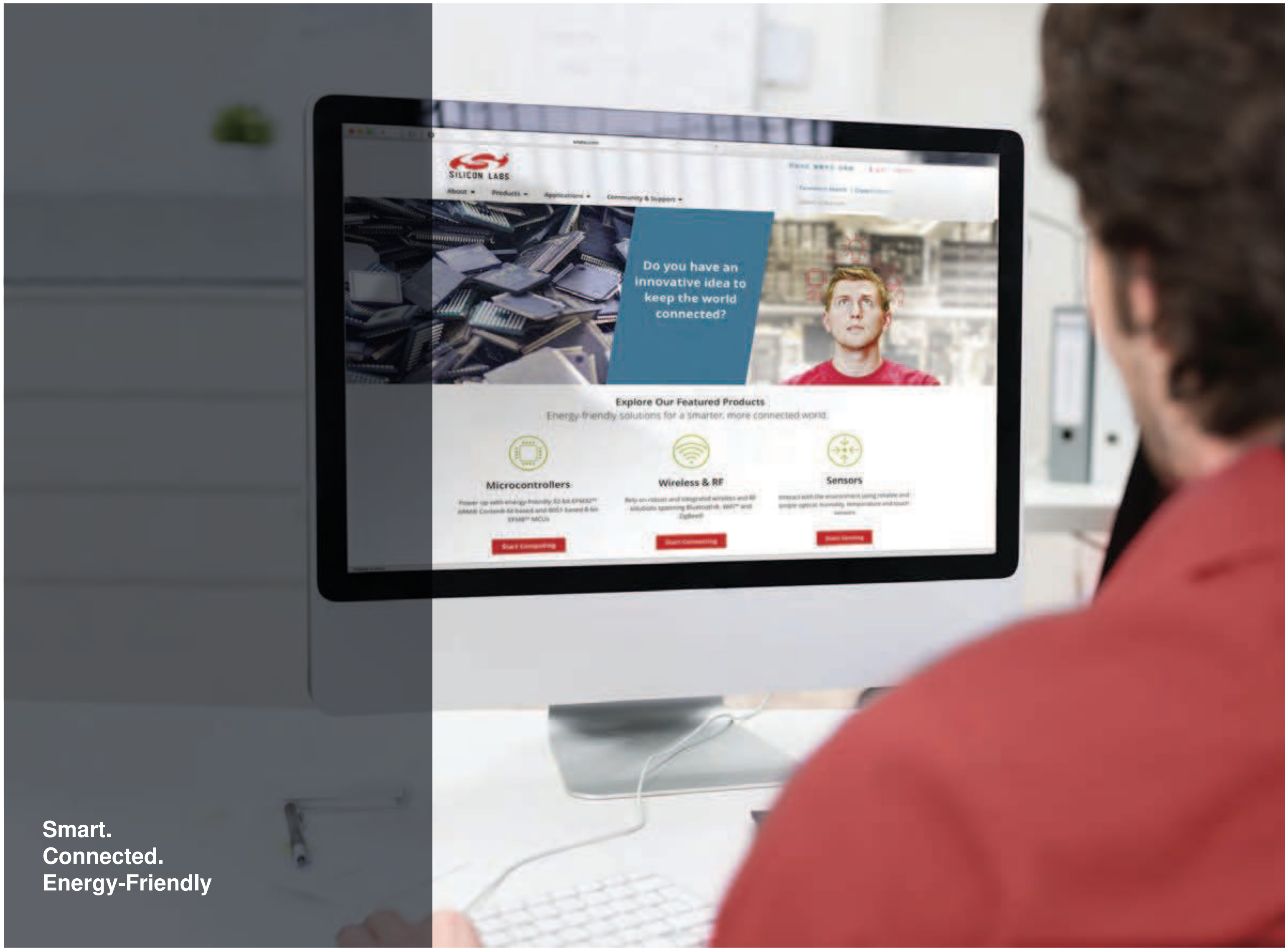

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