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TS4621B

High-performance class-G stereo headphone amplifier with I²C volume control

Features

- Power supply range: 2.3 V to 4.8 V
- 0.6 mA/channel quiescent current
- 2.1 mA current consumption with 100 µW/channel (10 dB crest factor)
- 0.006% typical THD+N at 1 kHz
- 100 dB typical PSRR at 217 Hz
- 100 dB of SNR A-weighted at G = 0 dB
- Zero pop and click
- I²C interface for volume control
- Digital volume control range from -60 dB to +4 dB
- Independent right and left channel shutdown control
- Integrated high-efficiency step-down converter
- Low software standby current: 5 µA max
- Output-coupling capacitors removed
- Thermal shutdown
- Flip-chip package: 1.65 mm x 1.65 mm, 400 µm pitch, 16 bumps

Applications

- Cellular phones, smart phones
- Mobile internet devices
- PMP/MP3 players

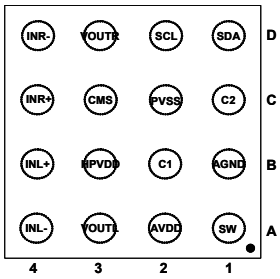
Description

The TS4621B is a class-G stereo headphone driver dedicated to high audio performance, high power efficiency and space-constrained applications.

It is based on the core technology of a low power dissipation amplifier combined with a high-efficiency step-down DC/DC converter for supplying this amplifier.

TS4621BEIJT - flip-chip

Pinout (top view)



Balls are underneath

When powered by a battery, the internal step-down DC/DC converter generates the appropriate voltage to the amplifier depending on the amplitude of the audio signal to supply the headsets. It achieves a total 2.1 mA current consumption at 100 µW output power (10 dB crest factor).

THD+N is 0.02 % maximum at 1 kHz and PSRR is 100 dB at 217 Hz, which ensures a high audio quality of the device in a wide range of environments.

The traditionally bulky output coupling capacitors can be removed.

A dedicated common-mode sense pin removes parasitic ground noise.

The TS4621B is designed to be used with an output serial resistor. It ensures unconditional stability over a wide range of capacitive loads.

The TS4621B is packaged in a tiny 16-bump flip-chip package with a pitch of 400 µm.

Contents

List of figures

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1) during 1ms.	5.5	V
V_{in+},V_{in-}	Input voltage referred to ground	+/- 1.2	V
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature(2)	150	°C
R_{thja}	Thermal resistance junction to ambient (3)	200	°C/W
P_d	Power dissipation	Internally limited(4)	
ESD	Human body model (HBM)(5) All pins VOUTR, VOUTL vs. AGND	 2 4	kV
	Machine model (MM), min. value(6)	100	V
	Charge device model (CDM) All pins VOUTR, VOUTL	 500 750	V
	IEC61000-4-2 level 4, contact(7) IEC61000-4-2 level 4, air discharge(7)	+/- 8 +/- 15	kV
	Lead temperature (soldering, 10 sec)	260	°C

1. All voltage values are measured with respect to the ground pin.
2. Thermal shutdown is activated when maximum junction temperature is reached.
3. The device is protected from over-temperature by a thermal shutdown mechanism, active at 150° C.
4. Exceeding the power derating curves for long periods may provoke abnormal operation.
5. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
6. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
7. The measurement is performed on an evaluation board, with ESD protection EMIF02-AV01F3.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.3 to 4.8	V
HPVDD	internal step-down DC output voltages High rail voltage Low rail voltage	 1.9 1.2	V
SDA, SCL	Input voltage range	GND to V_{cc}	V
R_L	Load resistor	≥ 16	Ω
C_L	Load capacitor Serial resistor of 12 Ω minimum, $R_L \geq 16$ Ω	 0.8 to 100	nF
T_{oper}	Operating free air temperature range	-40 to +85	°C
R_{thja}	Flip-chip thermal resistance junction to ambient	90	°C/W

2 Typical application schematics

Figure 1. Typical application schematics for the TS4621B

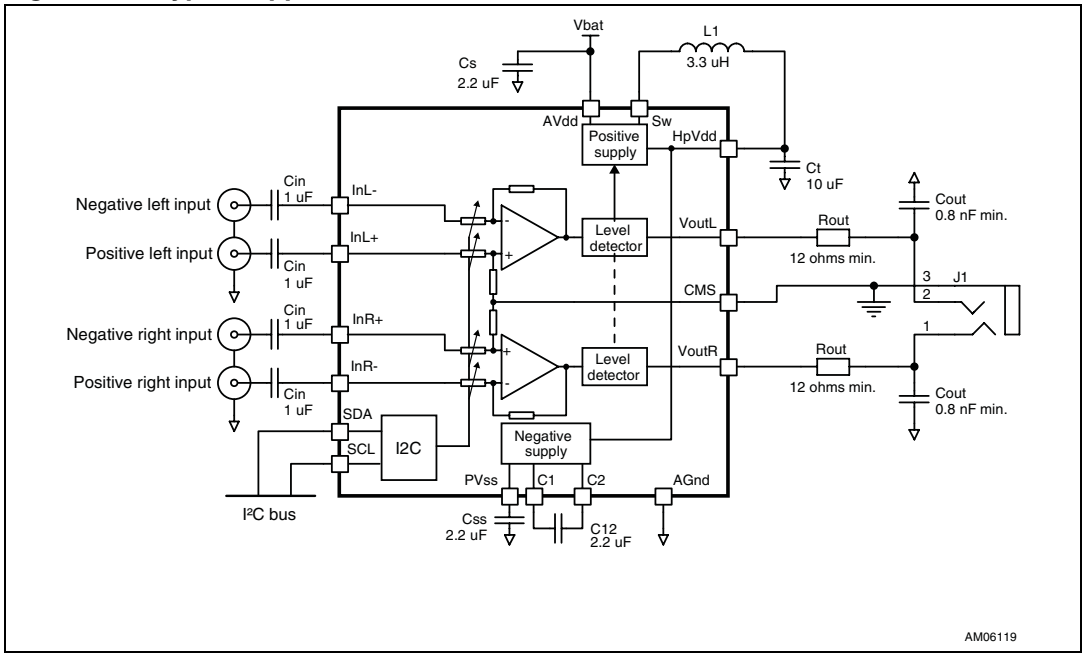


Table 3. TS4621B pin description

Pin number	Pin name	Pin definition
A1	SW	Switching node of the buck converter
A2	AVDD	Analog supply voltage, connect to battery
A3	VOUTL	Output signal for left audio channel
A4	INL-	Negative input signal for left audio channel
B1	AGND	Device ground
B2	C1	Flying capacitor terminal for internal negative supply generator
B3	HPVDD	Buck converter output, power supply for amplifier
B4	INL+	Positive input signal for left audio channel
C1	C2	Flying capacitor terminal for internal negative supply generator
C2	PVSS	Negative supply generator output
C3	CMS	Common mode sense, to be connected as close as possible to the ground of headphone/line out plug
C4	INR+	Positive input signal for right audio channel
D1	SDA	I²C data signal, up to V_{CC} tolerant input
D2	SCL	I²C clock signal, up to V_{CC} tolerant input
D3	VOUTR	Output signal for right audio channel
D4	INR-	Negative input signal for right audio channel

Table 4. TS4621B component description(1)

Component	Value	Description
Cs	2.2 µF	Decoupling capacitors for V_{CC}. A 2.2 µF capacitor is sufficient for proper decoupling of the TS4621B. An X5R dielectric and 10 V rating voltage is recommended to minimize $\Delta C/\Delta V$ when V_{CC} = 4.8 V. Must be placed as close as possible to the TS4621B to minimize parasitic inductance and resistance.
C12	2.2 µF	Capacitor for internal negative power supply operation. An X5R dielectric and 6.3 V rating voltage is recommended to minimize $\Delta C/\Delta V$ when HPVDD = 1.9 V. Must be placed as close as possible to the TS4621B to minimize parasitic inductance and resistance.
C_{SS}	2.2 µF	Filtering capacitor for internal negative power supply. An X5R dielectric and 6.3 V rating voltage is recommended to minimize $\Delta C/\Delta V$ when HPVDD = 1.9 V.
C_{in}	$Cin = \frac{1}{2 \times \pi \times Rin \times Fc}$	Input coupling capacitor that forms with Rin ≈ Rindiff/2 a first-order high-pass filter with a -3 dB cutoff frequency Fc. For example, at maximum gain G = 4 dB, Rin = 12.5 kΩ, C_{in} = 1 µF, therefore Fc = 13 Hz.
C_{out}	0.8 to 100 nF	Output capacitor of 0.8 nF minimum to 100 nF maximum. This capacitor is mandatory for operation of the TS4621B.
R_{out}	12 Ω min.	Output resistor in-series with the TS4621B output. This 12 Ω minimum resistor is mandatory for operation of the TS4621B.
L1	3.3 µH	Inductor for internal DC/DC step-down converter. References of inductors: refer to *Section 4.4.1* for more information.
C_t	10 µF	Tank capacitor for internal DC/DC step-down converter. An X5R dielectric and 6.3 V rating voltage is recommended to minimize $\Delta C/\Delta V$ when HPVDD = 1.9 V. Refer to *Section 4.4.2* for more information.

1. Refer to *Section 4.4* for a complete description of each component.

3 Electrical characteristics

Table 5. Electrical characteristics of the I²C interface for V_{CC} = +3.6 V, AGND = 0 V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage on SDA, SCL pins			0.6	V
V_{IH}	High level input voltage on SDA, SCL pins	1.2			V
V_{OL}	Low level output voltage, SDA pin, I_{sink} = 3mA			0.4	V
I_{in}	Input current on SDA, SCL		$\frac{V_{SDA, SCL}}{600k\Omega}$	10	µA

Table 6. Electrical characteristics of the amplifier for V_{CC} = +3.6 V, AGND = 0 V, R_L= 32 Ω + 15 Ω, T_{amb} = 25° C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Quiescent supply current, no input signal, both channels enabled		1.2	1.5	mA
I_s	Supply current, with input modulation, both channels enabled, HPVDD = 1.2 V, output power per channel, F=1kHz Pout = 100 µW at 3 dB crest factor Pout = 500 µW at 3 dB crest factor Pout = 1 mW at 3 dB crest factor Pout = 100 µW at 10 dB crest factor Pout = 500 µW at 10 dB crest factor Pout = 1 mW at 10 dB crest factor		 2.3 3.7 4.7 2.1 3.1 3.9	 3.5 5 6.5	mA
I_{STBY}	Standby current, no input signal, I²C CR1 = 01h V_{SDA} = 0 V, V_{SCL} = 0 V		0.6	5	µA
V_{in}	Input differential voltage range(1)			1	V_{rms}
V_{oo}	Output offset voltage No input signal	-500		+500	µV
V_{out}	Maximum output voltage, in-phase signals R_L = 16 Ω, THD+N = 1% max, f = 1 kHz R_L = 47 Ω, THD+N = 1% max, f = 1 kHz R_L = 10 kΩ, R_s = 15 Ω, C_L = 1 nF, THD+N = 1% max, f = 1 kHz	 0.6 1.0 1.0	 0.8 1.1 1.3		V_{rms}
THD+N	Total harmonic distortion + noise, G = 0 dB V_{out} = 700 mVrms, F = 1 kHz V_{out} = 700 mVrms, 20 Hz < F < 20 kHz		 0.006 0.05	0.02	%
PSRR	Power supply rejection ratio(1), V_{ripple} = 200 mV_{pp}, grounded inputs F = 217 Hz, G = 0 dB, R_L ≥16 Ω F = 10 kHz, G = 0 dB, R_L ≥16 Ω	 90	 100 70		dB

Table 6. Electrical characteristics of the amplifier for V_{CC} = +3.6 V, AGND = 0 V, R_L= 32 Ω + 15 Ω, T_{amb} = 25° C (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
CMRR	Common mode rejection ratio F = 1 kHz, G = 0 dB, V_{ic} = 200 mV_{pp} F = 20 Hz to 20 kHz, G = 0 dB, V_{ic} = 200 mV_{pp}		 65 45		dB
Crosstalk	Channel separation R_L = 32 Ω + 15 Ω , G = 0 dB, F = 1 kHz, P_o = 10 mW R_L = 10 kΩ, G = 0 dB, F = 1 kHz, V_{out} = 1 Vrms	 60 80	 100 110		dB
SNR	Signal-to-noise ratio, A-weighted, V_{out} = 1 V_{rms}, THD+N < 1%, F = 1 kHz(1) G = +4 dB G = +0 dB	 99 100			dB
ONoise	Output noise voltage, A-weighted (1) G = +4 dB G = +0 dB		9	 11 9	µVrms
G	Gain range with gain (dB) = 20 x log[(V_{out}L/R)/(InL/R+ - InL/R-)]	-60		+4	dB
Mute	InL/R+ - InL/R- = 1 V_{rms}			-80	dB
-	Gain step size error	-0.5		+0.5	step-size
-	Gain error (G = +4 dB)	-0.45		+0.42	dB
R_{indiff}	Differential input impedance	25	34		kΩ
	Input impedance during wake-up phase (referred to ground)		2		kΩ
Z_{out}	Output impedance when CR1 = 00h (negative supply is ON and amplifier output stages are OFF)(1) F < 40 kHz F = 6 MHz F = 36 MHz	 10 500 75			 kΩ Ω Ω
t_{wu}	Wake-up time(2)		12	16	ms
t_{stby}	Standby time		100		µs
t_{atk}	Attack time. Setup time between low rail and high rail voltages of internal step-down DC/DC converter		100		µs
t_{dcy}	Decay time		50		ms

1. Guaranteed by design and parameter correlation.
2. Refer to the application information in *Section 4.2 on page 30*.

Table 7. Timing characteristics of the I²C interface for I²C interface signals over recommended operating conditions (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{SCL}	Frequency, SCL			400	kHz
$t_{d(H)}$	Pulse duration, SCL high	0.6			µs
$t_{d(L)}$	Pulse duration, SCL low	1.3			µs
t_{st1}	Setup time, SDA to SCL	100			ns
t_{h1}	Hold time, SCL to SDA	0			ns
t_f	Bus free time between stop and start condition	1.3			µs
t_{st2}	Setup time, SCL to start condition	0.6			µs
t_{h2}	Hold time, start condition to SCL	0.6			µs
t_{st3}	Setup time, SCL to stop condition	0.6			µs

Figure 2. SCL and SDA timing diagram

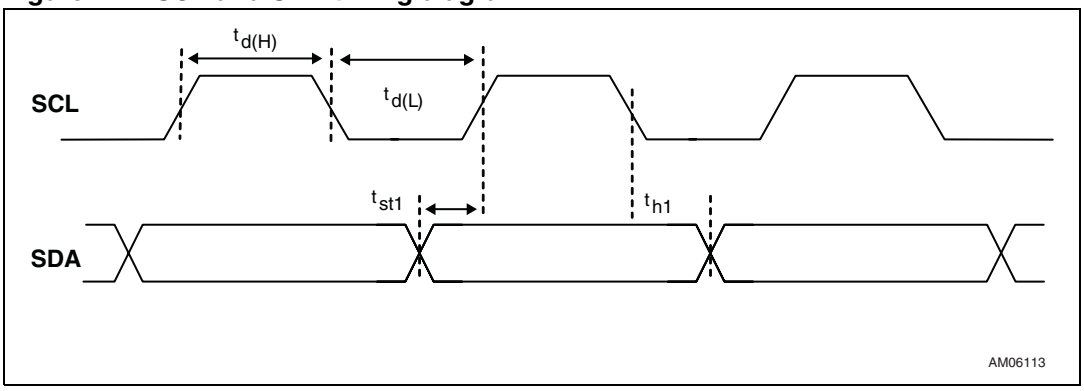


Figure 3. Start and stop condition timing diagram

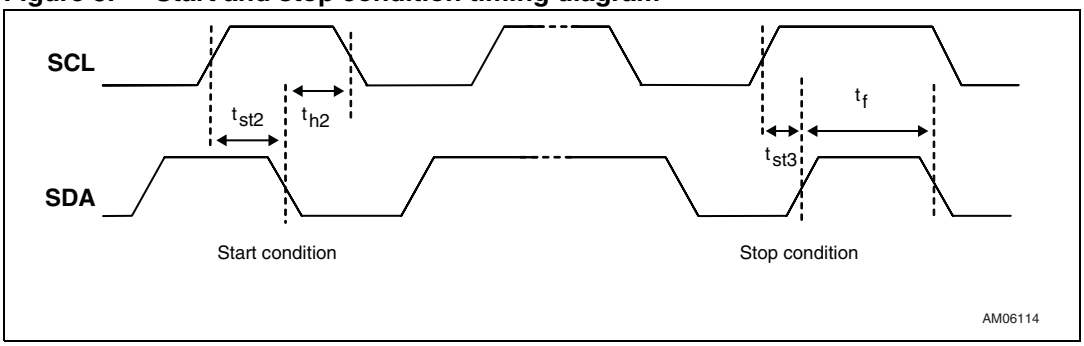


Figure 4. Current consumption vs. power supply voltage

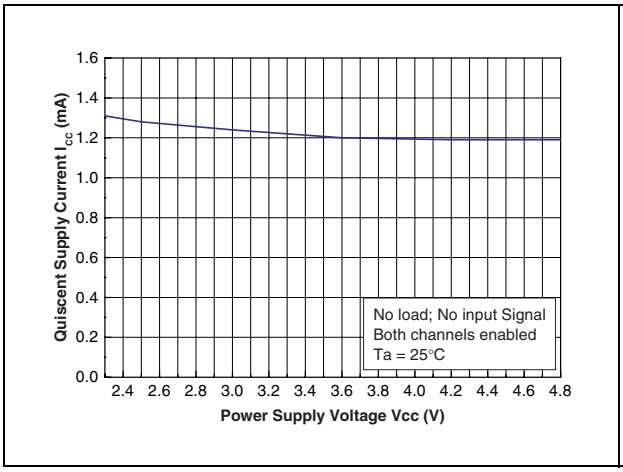


Figure 5. Standby current consumption vs. power supply voltage

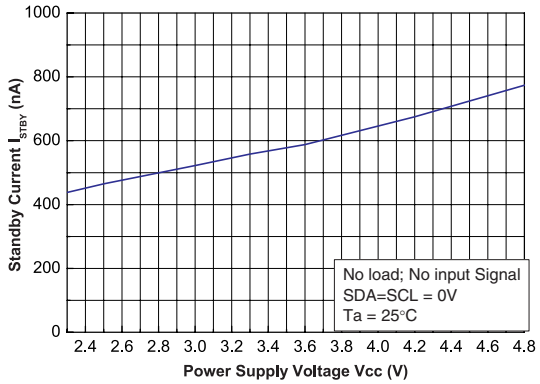


Figure 6. Maximum output power vs. load in-phase

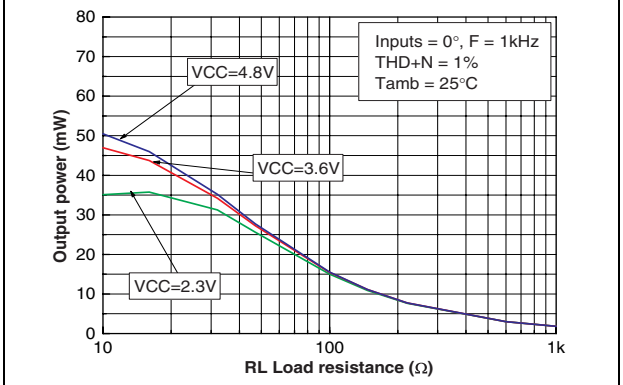


Figure 7. Maximum output power vs. load out-of-phase

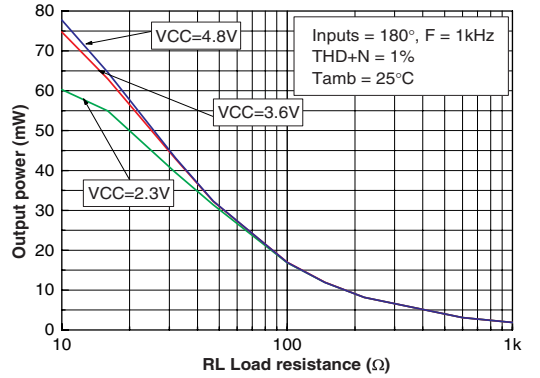


Figure 8. Maximum output power vs. power supply voltage, RL = 16 Ω

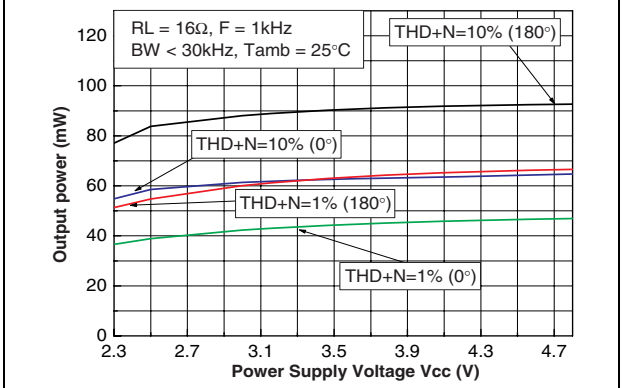


Figure 9. Maximum output power vs. power supply voltage, RL = 32 Ω

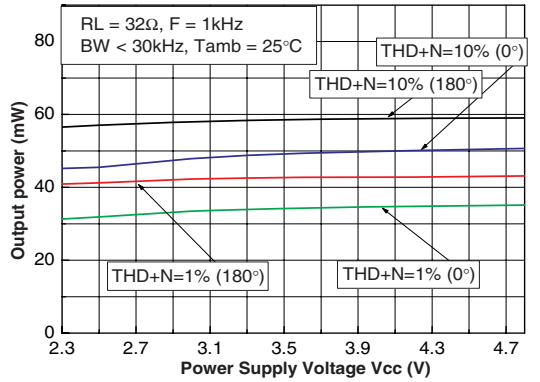


Figure 10. Maximum output power vs. power supply voltage, RL = 47 Ω

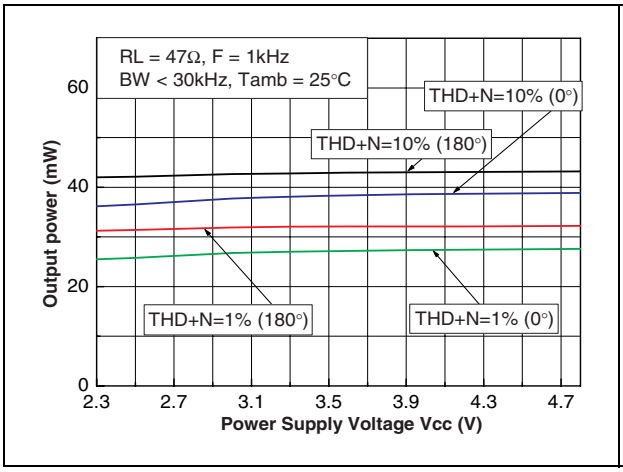


Figure 11. Maximum output voltage vs. power supply voltage, in-phase

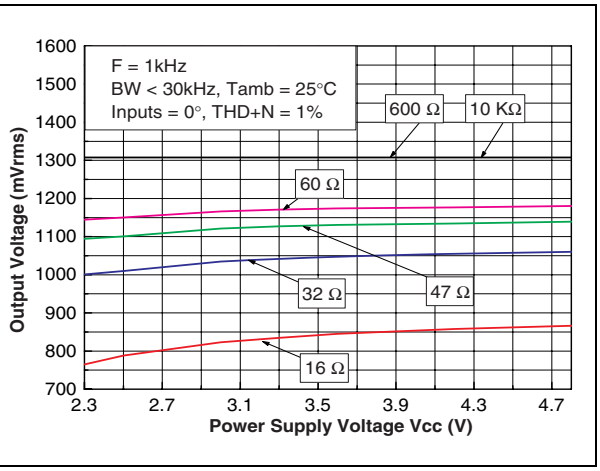


Figure 12. Maximum output voltage vs. power supply voltage, out-of-phase

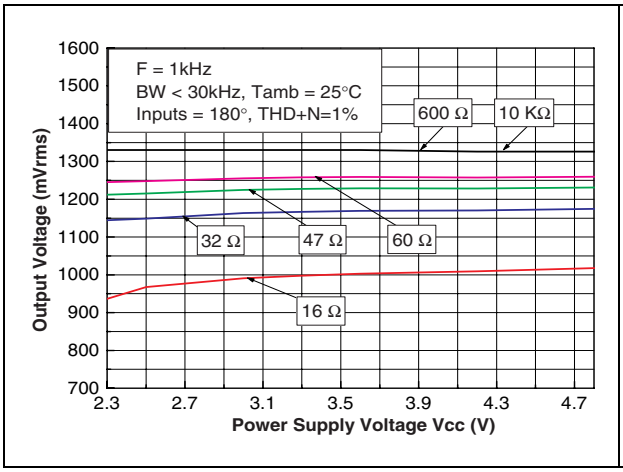


Figure 13. Current consumption vs. total output power, RL = 16 Ω

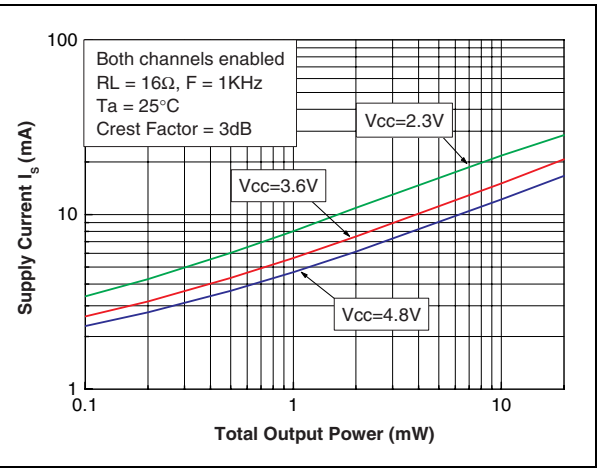


Figure 14. Current consumption vs. total output power, RL = 32 Ω

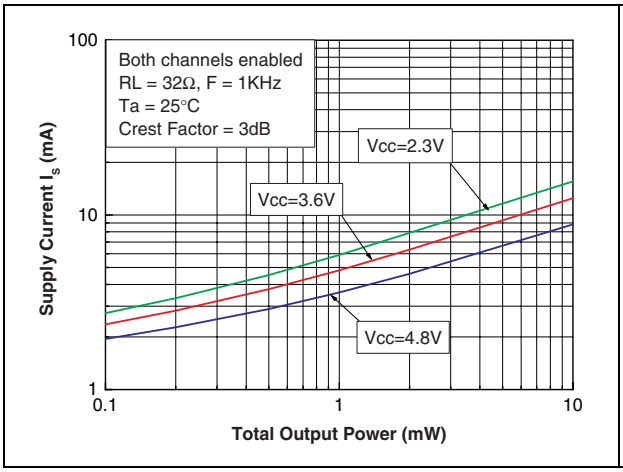


Figure 15. Current consumption vs. total output power, RL = 47 Ω

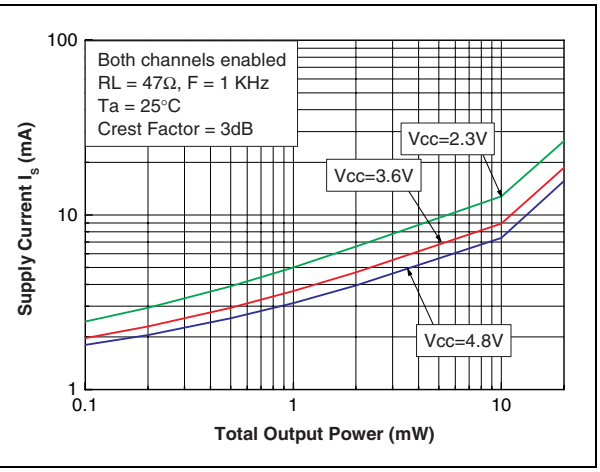


Figure 16. Current consumption vs. total output power

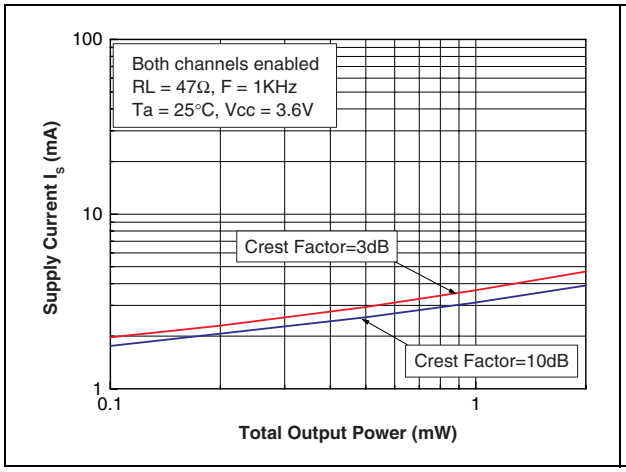


Figure 17. Power dissipation vs. total output power

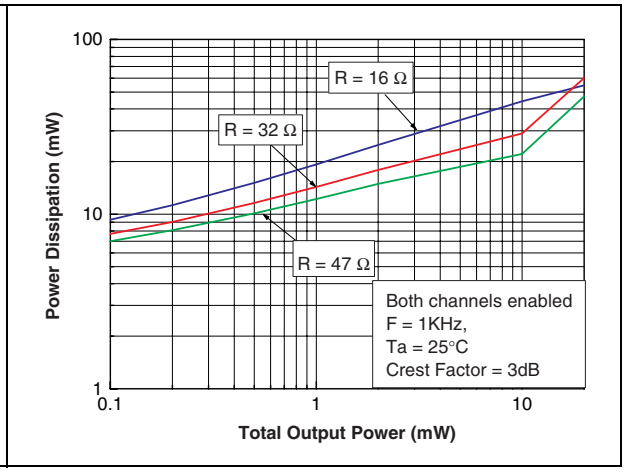


Figure 18. Output impedance vs. frequency in HiZ mode

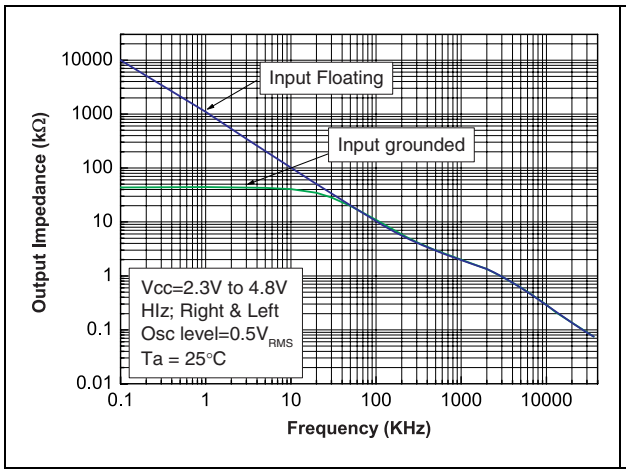


Figure 19. Differential input impedance vs. gain

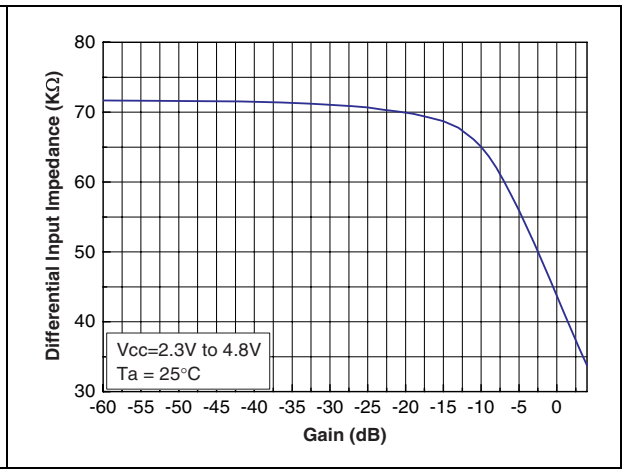


Figure 20. THD+N vs. output power RL = 16 Ω, in-phase, V_{CC} = 2.5 V

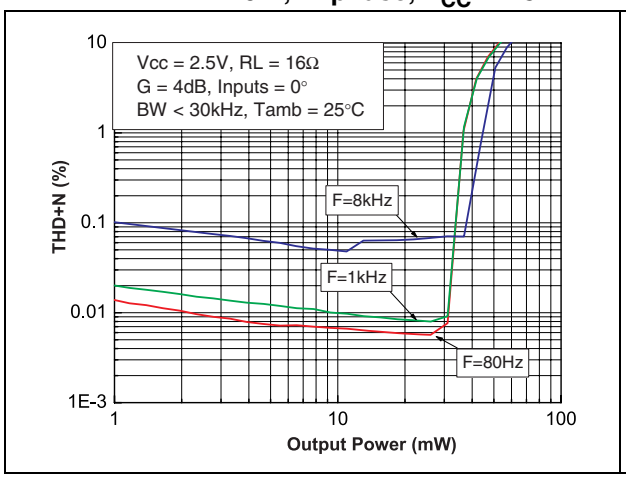


Figure 21. THD+N vs. output power RL = 16 Ω, out-of-phase, V_{CC} = 2.5 V

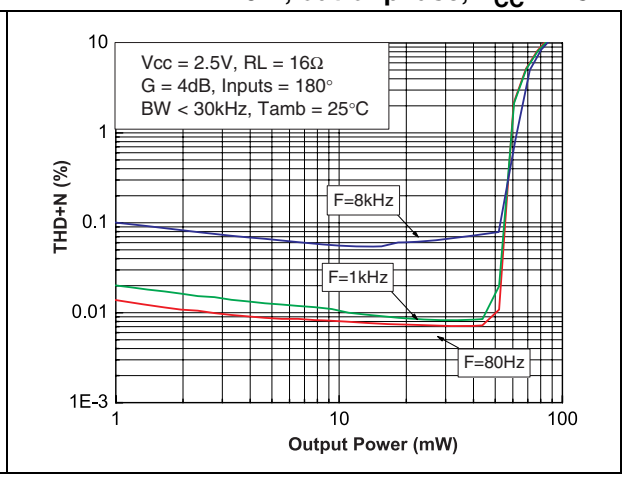


Figure 22. THD+N vs. output power RL = 16 Ω, in-phase, V_{CC} = 3.6 V

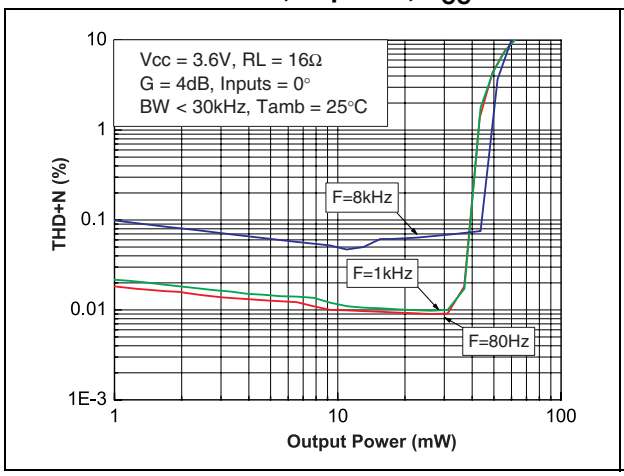


Figure 23. THD+N vs. output power RL = 16 Ω, out-of-phase, V_{CC} = 3.6 V

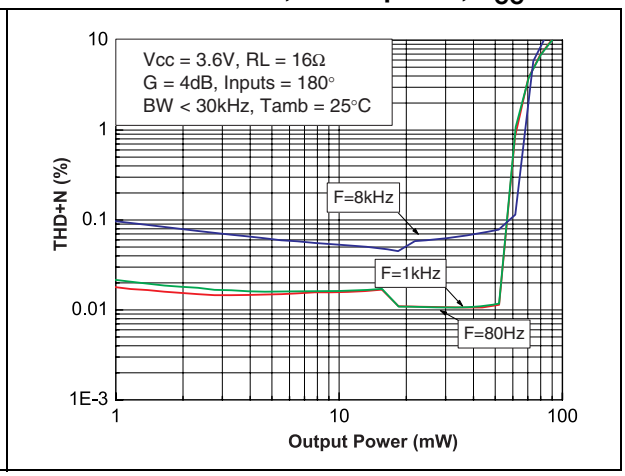


Figure 24. THD+N vs. output power RL = 16 Ω, in-phase, V_{CC} = 4.8 V

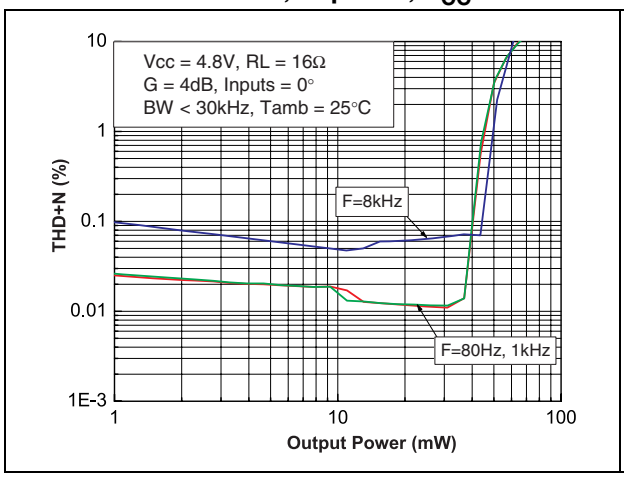


Figure 25. THD+N vs. output power RL = 16 Ω, out-of-phase, V_{CC} = 4.8 V

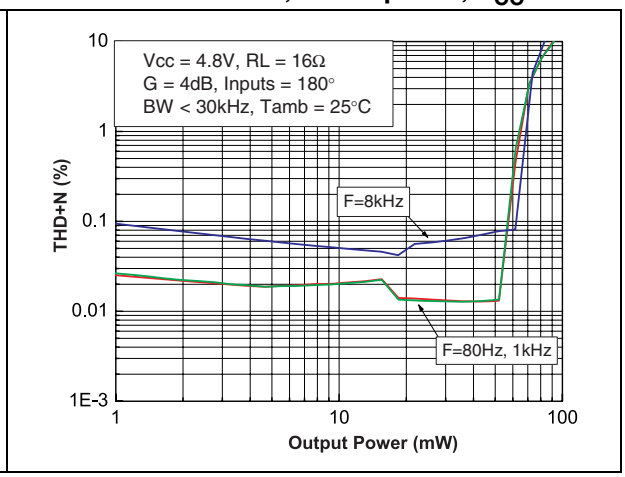


Figure 26. THD+N vs. output power RL = 32 Ω, in-phase, V_{CC} = 2.5 V

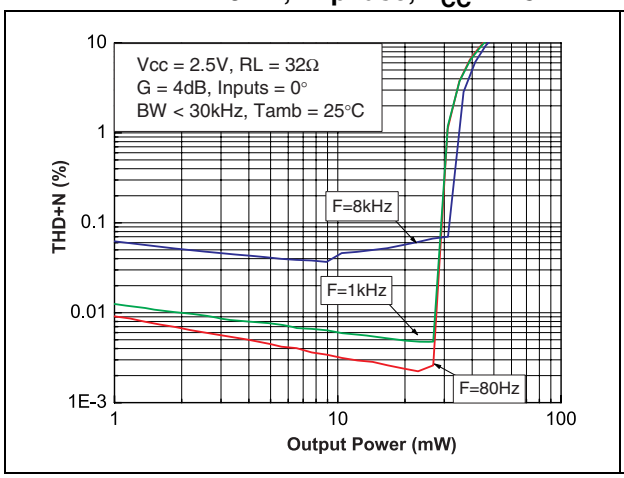


Figure 27. THD+N vs. output power RL = 32 Ω, out-of-phase, V_{CC} = 2.5 V

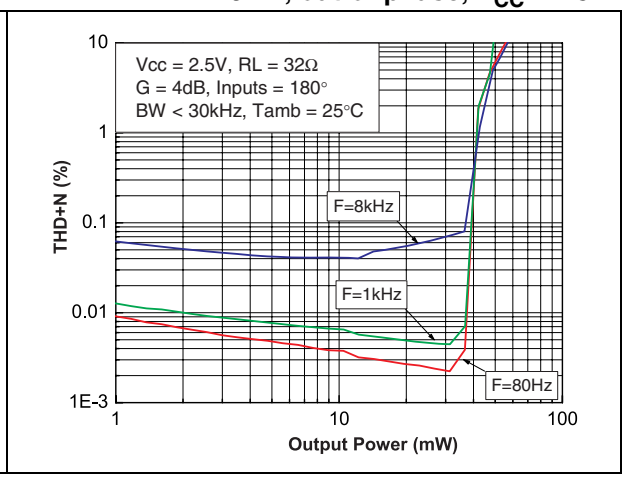


Figure 28. THD+N vs. output power RL = 32 Ω, in-phase, V_{CC} = 3.6 V

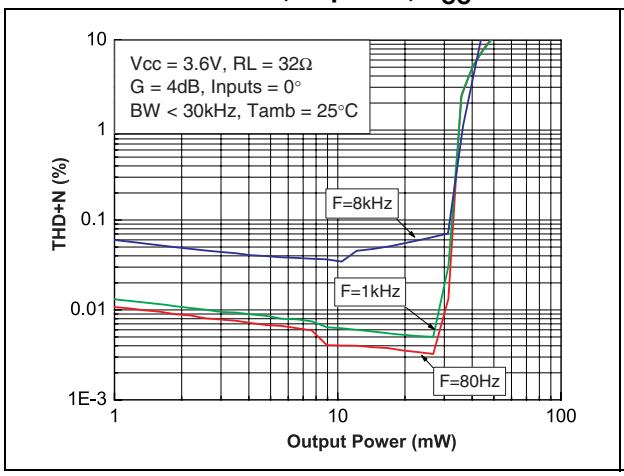


Figure 29. THD+N vs. output power RL = 32 Ω, out-of-phase, V_{CC} = 3.6 V

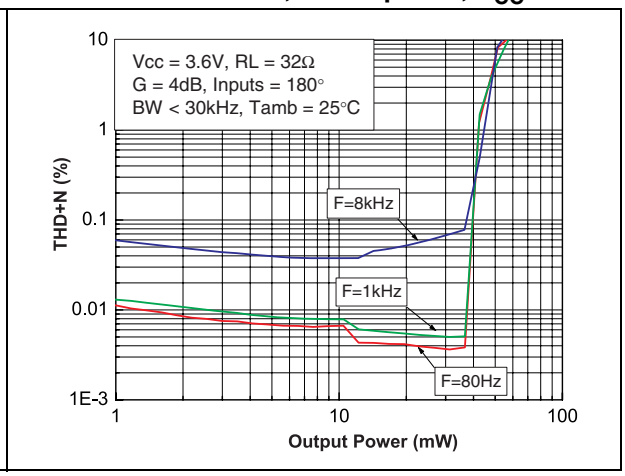


Figure 30. THD+N vs. output power RL = 32 Ω, in-phase, V_{CC} = 4.8 V

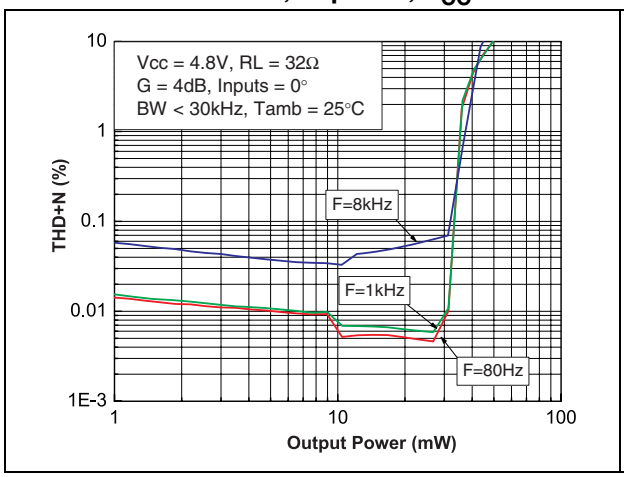


Figure 31. THD+N vs. output power RL = 32 Ω, out-of-phase, V_{CC} = 4.8 V

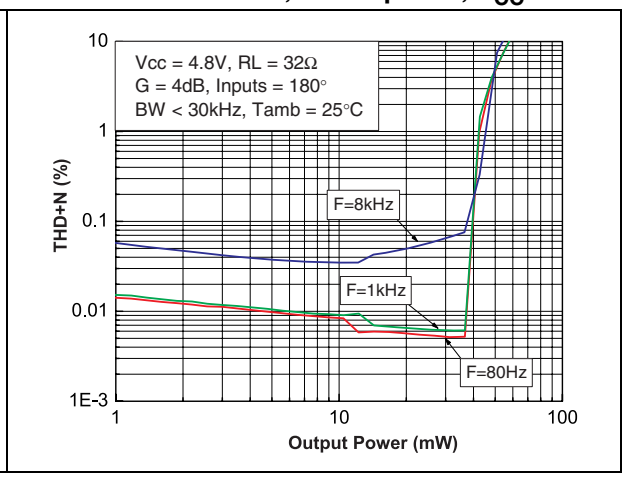


Figure 32. THD+N vs. output power RL = 47 Ω, in-phase, V_{CC} = 2.5 V

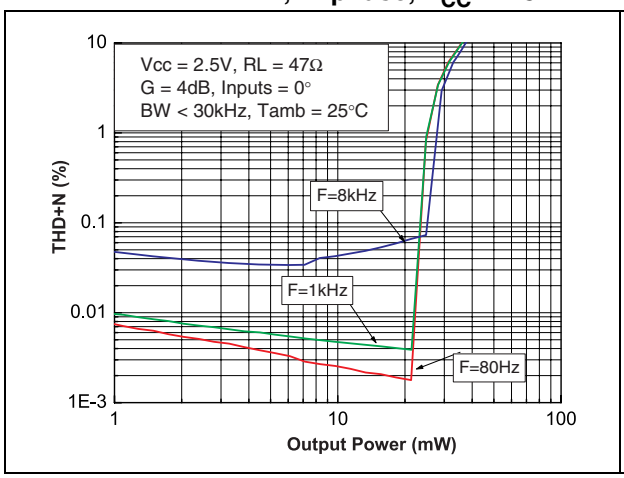


Figure 33. THD+N vs. output power RL = 47 Ω, out-of-phase, V_{CC} = 2.5 V

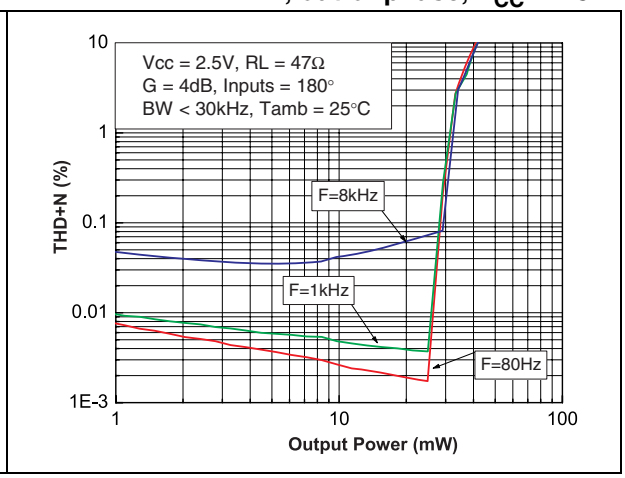


Figure 34. THD+N vs. output power RL = 47 Ω, in-phase, V_{CC} = 3.6 V

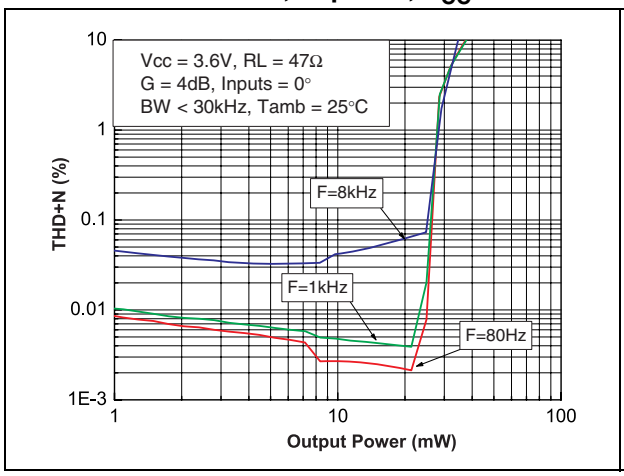


Figure 35. THD+N vs. output power RL = 47 Ω, out-of-phase, V_{CC} = 3.6 V

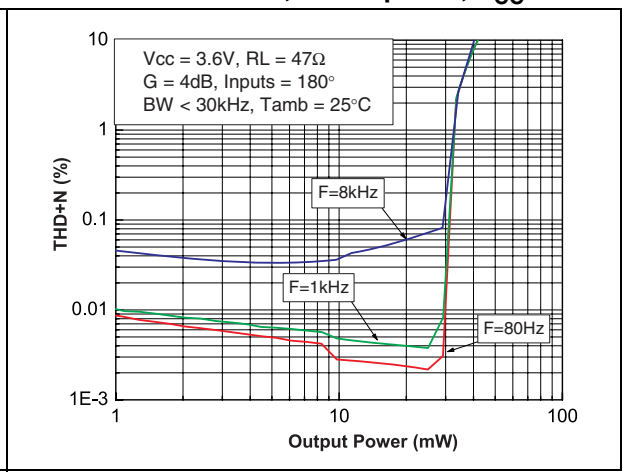


Figure 36. THD+N vs. output power RL = 47 Ω, in-phase, V_{CC} = 4.8 V

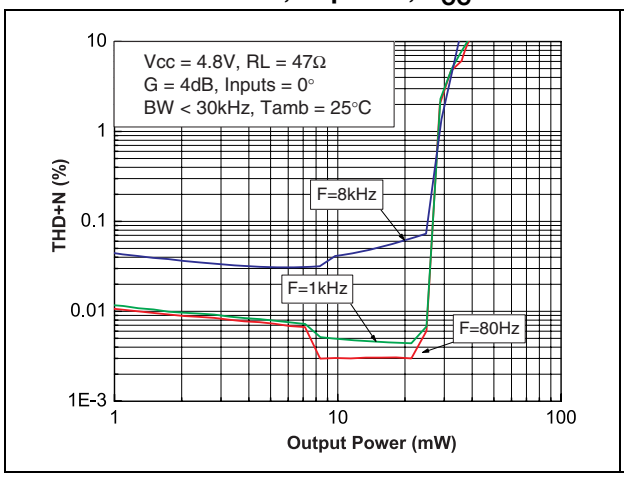


Figure 37. THD+N vs. output power RL = 47 Ω, out-of-phase, V_{CC} = 4.8 V

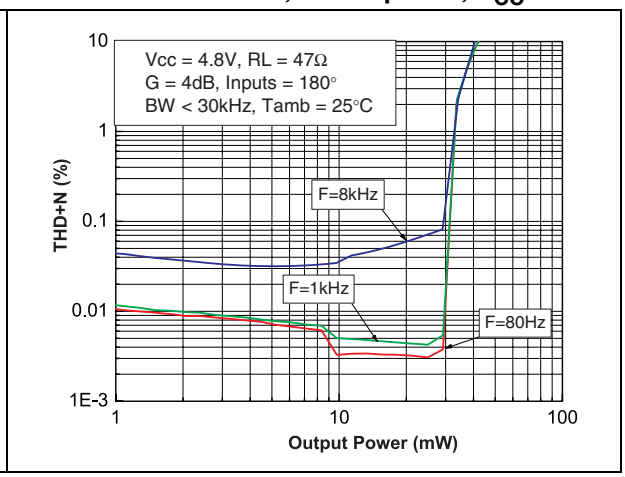


Figure 38. THD+N vs. frequency RL = 16 Ω, in-phase, V_{CC} = 2.5 V

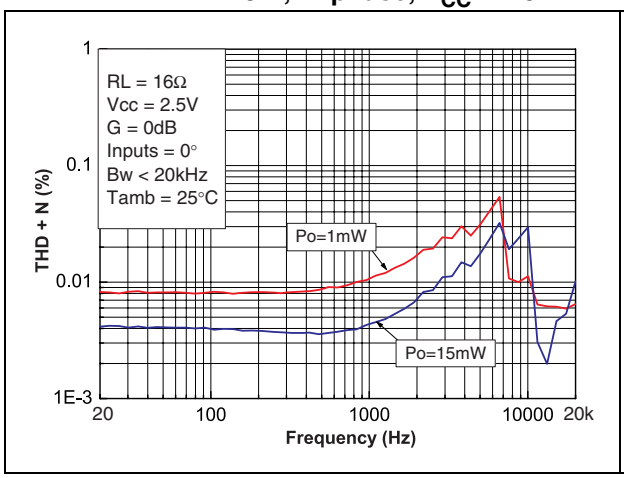


Figure 39. THD+N vs. frequency RL = 16 Ω, out-of-phase, V_{CC} = 2.5 V

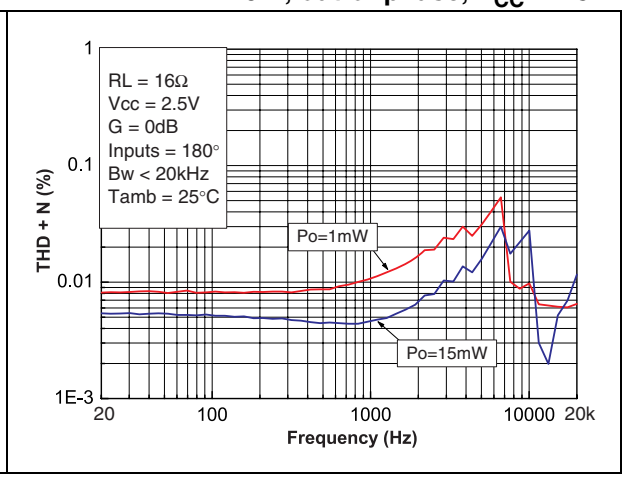


Figure 40. THD+N vs. frequency RL = 16 Ω, in-phase, V_{CC} = 3.6 V

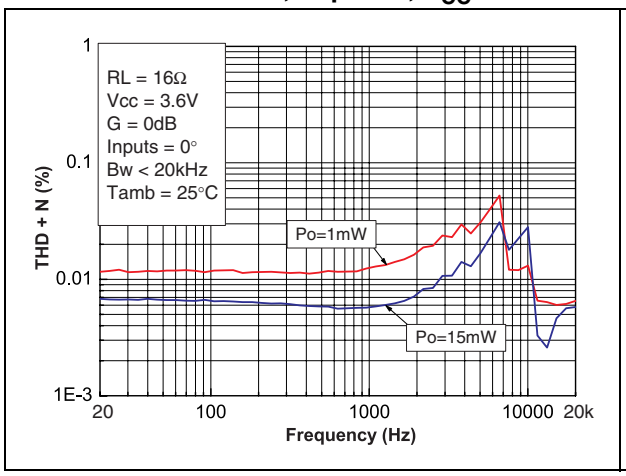


Figure 41. THD+N vs. frequency RL = 16 Ω, out-of-phase, V_{CC} = 3.6 V

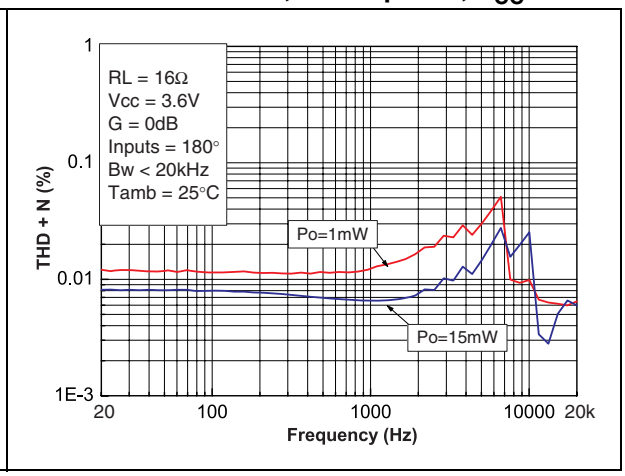


Figure 42. THD+N vs. frequency RL = 16 Ω, in-phase, V_{CC} = 4.8 V

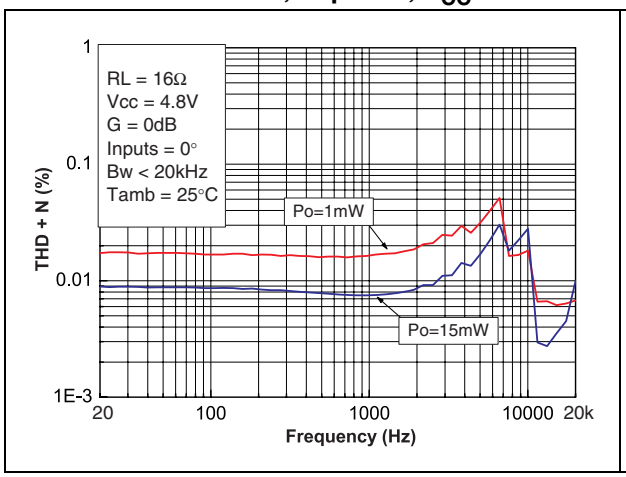


Figure 43. THD+N vs. frequency RL = 16 Ω, out-of-phase, V_{CC} = 4.8 V

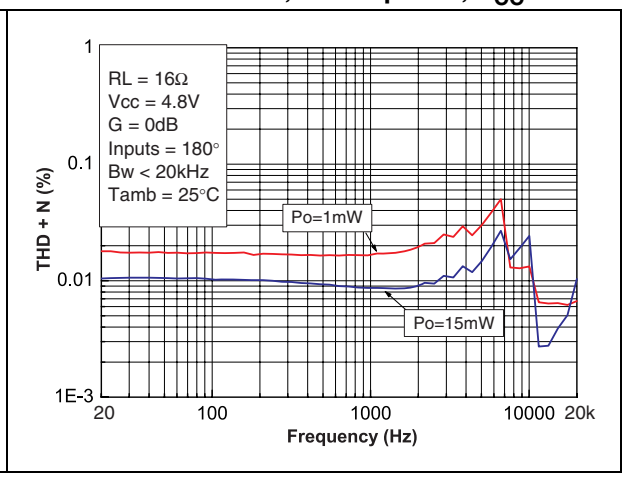


Figure 44. THD+N vs. frequency RL = 32 Ω, in-phase, V_{CC} = 2.5 V

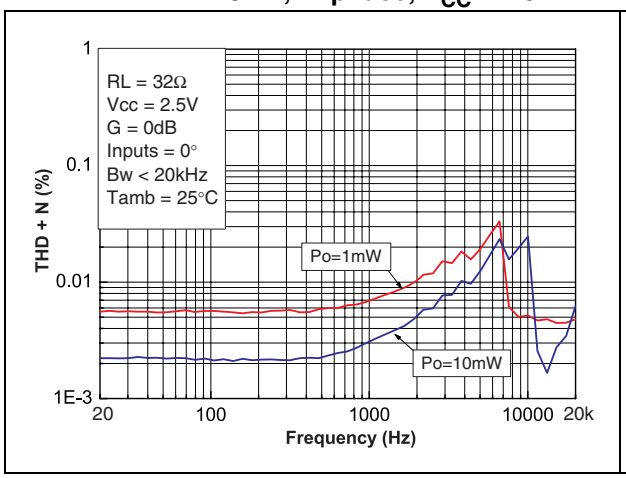


Figure 45. THD+N vs. frequency RL = 32 Ω, out-of-phase, V_{CC} = 2.5 V

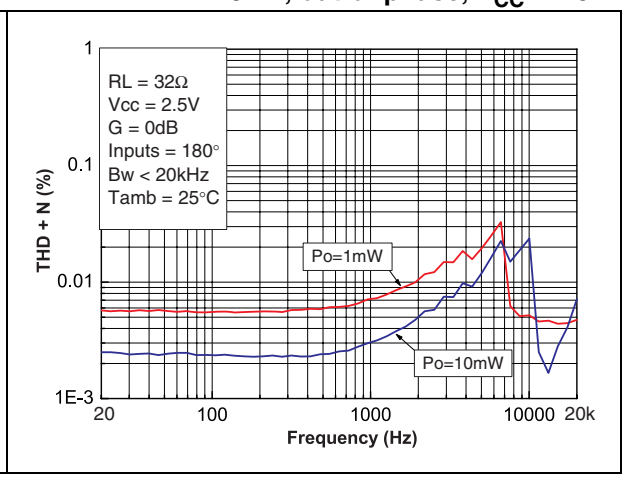


Figure 46. THD+N vs. frequency RL = 32 Ω, in-phase, V_{CC} = 3.6 V

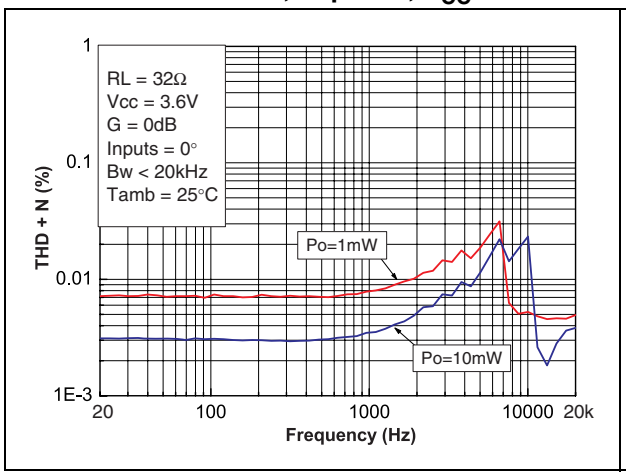


Figure 47. THD+N vs. frequency RL = 32 Ω, out-of-phase, V_{CC} = 3.6 V

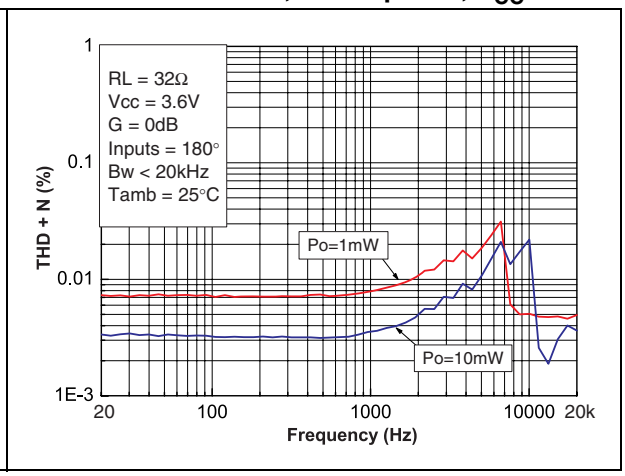


Figure 48. THD+N vs. frequency RL = 32 Ω, in-phase, V_{CC} = 4.8 V

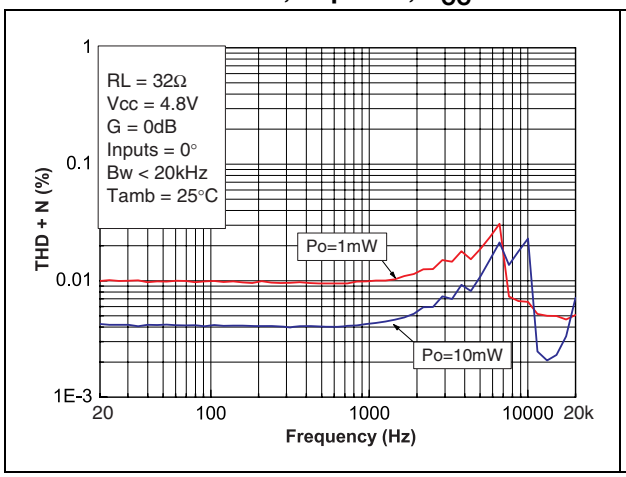


Figure 49. THD+N vs. frequency RL = 32 Ω, out-of-phase, V_{CC} = 4.8 V

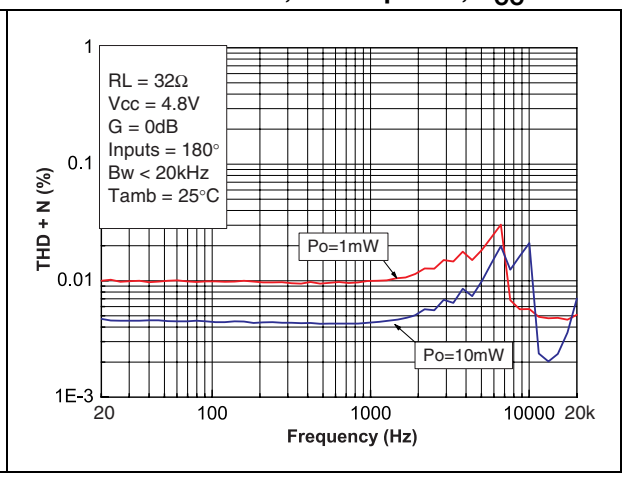


Figure 50. THD+N vs. frequency RL = 47 Ω, in-phase, V_{CC} = 2.5 V

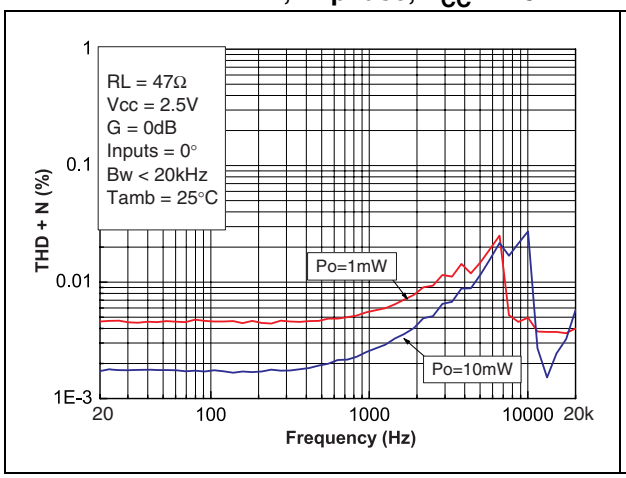


Figure 51. THD+N vs. frequency RL = 47 Ω, out-of-phase, V_{CC} = 2.5 V

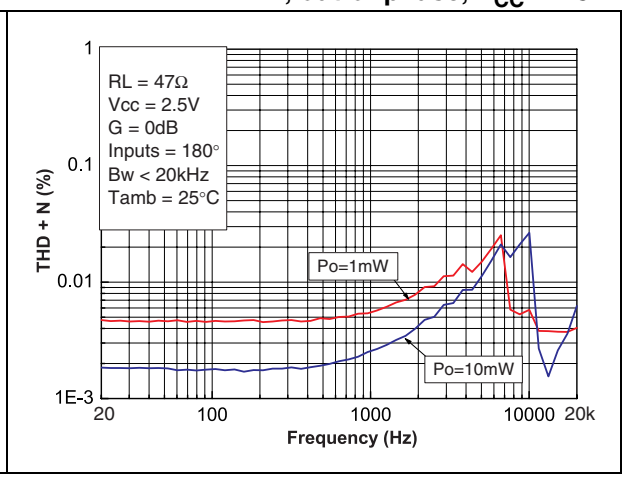


Figure 52. THD+N vs. frequency RL = 47 Ω, in-phase, V_{CC} = 3.6 V

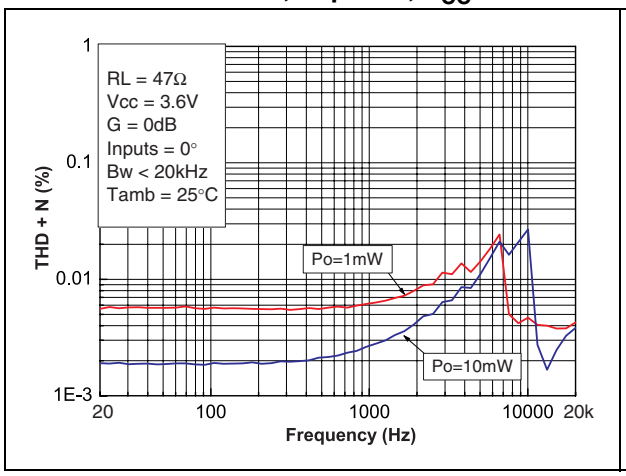


Figure 53. THD+N vs. frequency RL = 47 Ω, out-of-phase, V_{CC} = 3.6 V

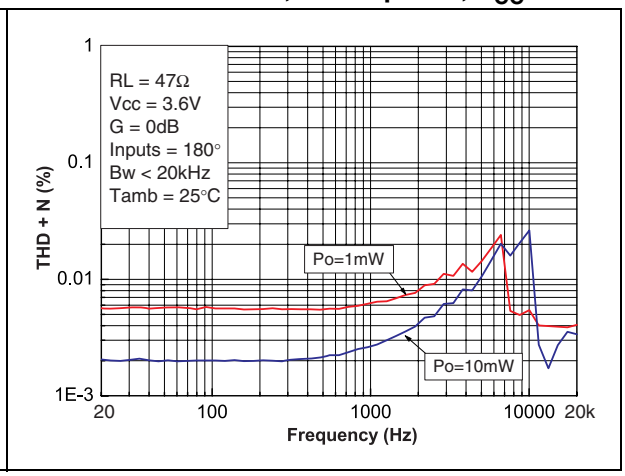


Figure 54. THD+N vs. frequency RL = 47 Ω, in-phase, V_{CC} = 4.8 V

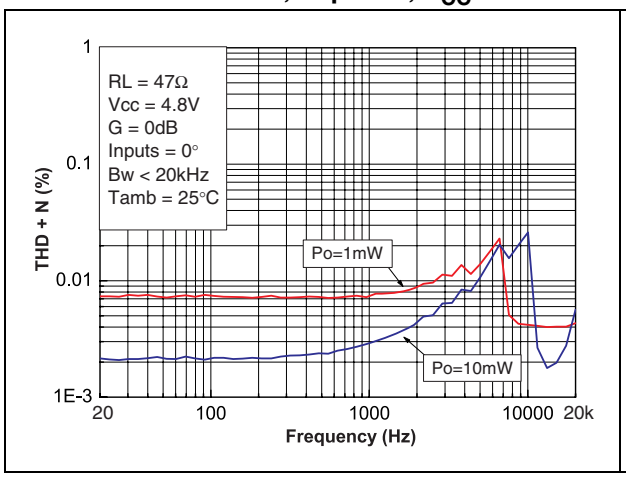


Figure 55. THD+N vs. frequency RL = 47 Ω, out-of-phase, V_{CC} = 4.8 V

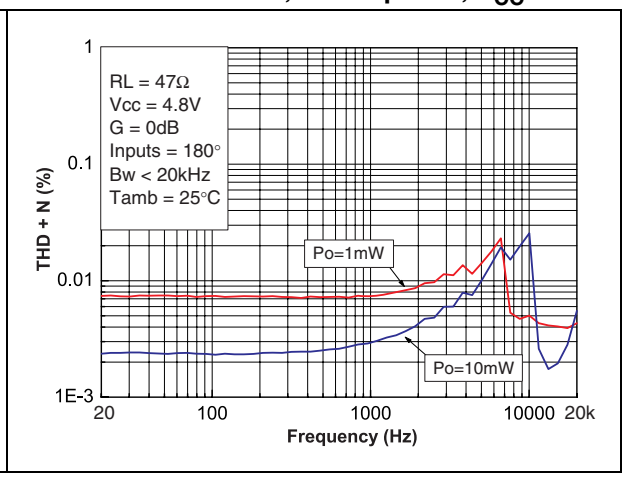


Figure 56. THD+N vs. frequency RL = 10 kΩ

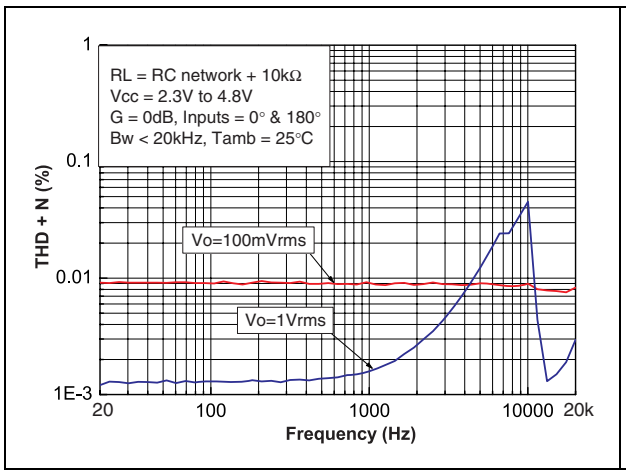


Figure 57. THD+N vs. frequency RL = 600 Ω

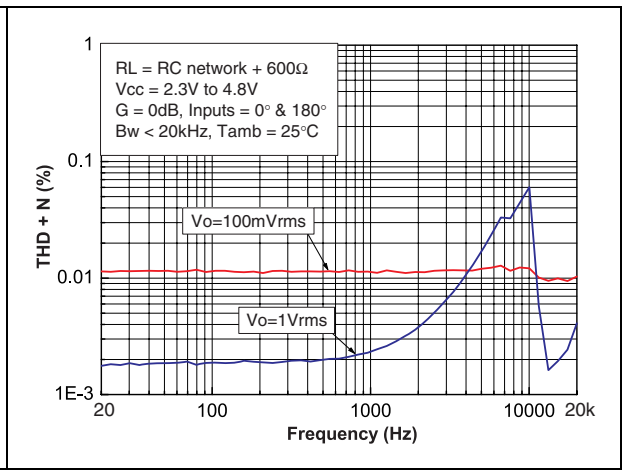


Figure 58. THD+N vs. output voltage RL = 10 kΩ

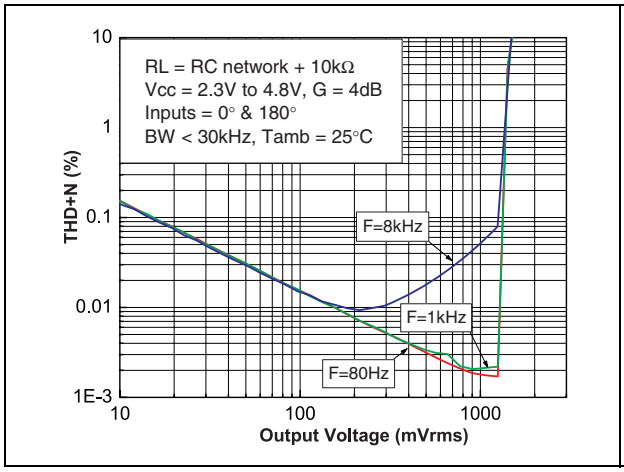


Figure 59. THD+N vs. output voltage RL = 600 Ω

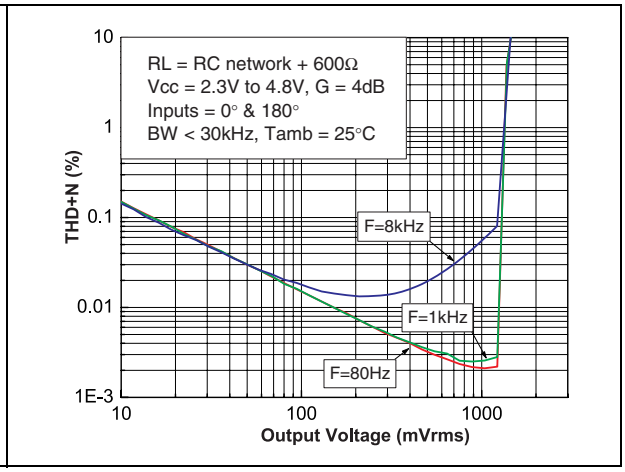


Figure 60. THD+N vs. input voltage, HiZ left and right

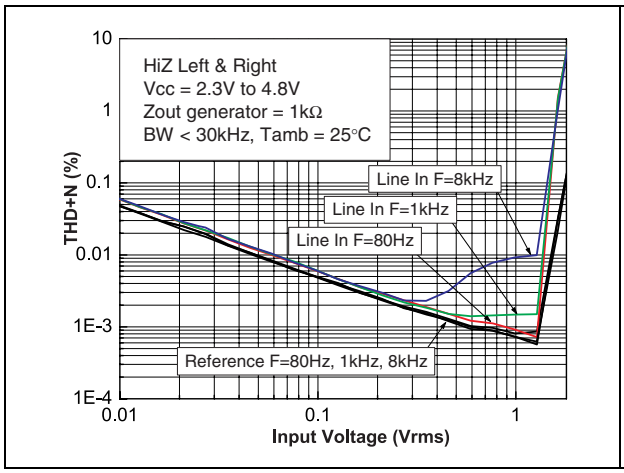


Figure 61. CMRR vs. frequency

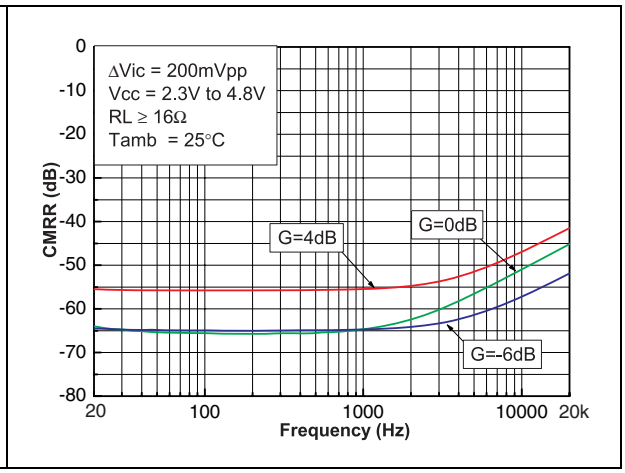


Figure 62. PSRR vs. frequency V_{CC} = 2.5 V

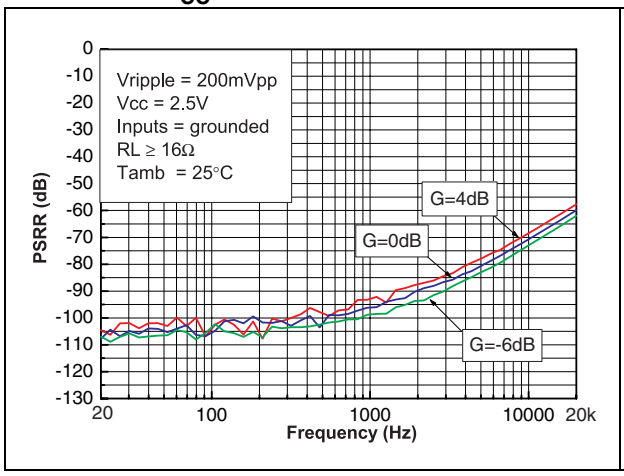


Figure 63. PSRR vs. frequency V_{CC} = 3.6 V

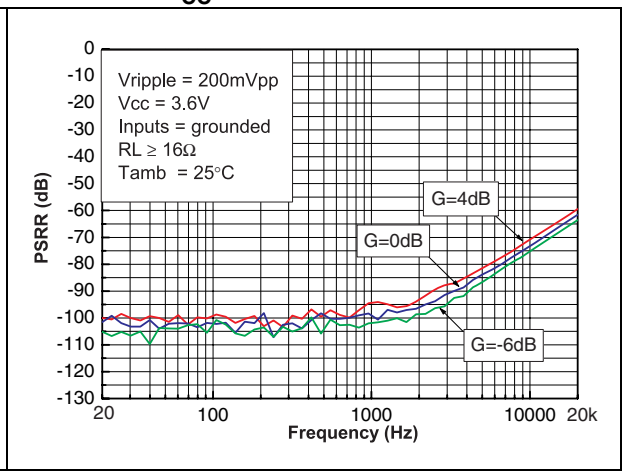


Figure 64. PSRR vs. frequency V_{CC} = 4.8 V

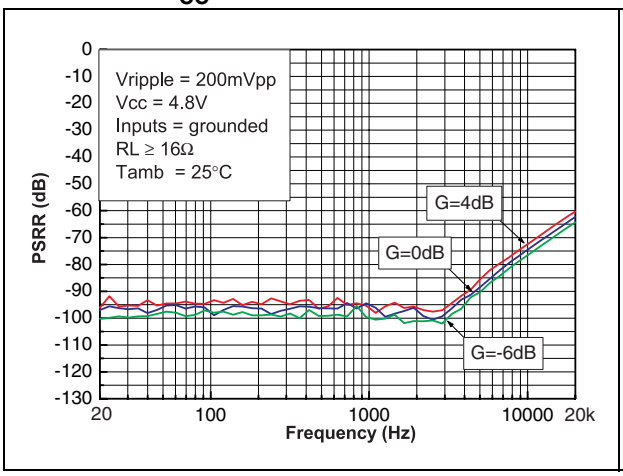


Figure 65. Output signal spectrum

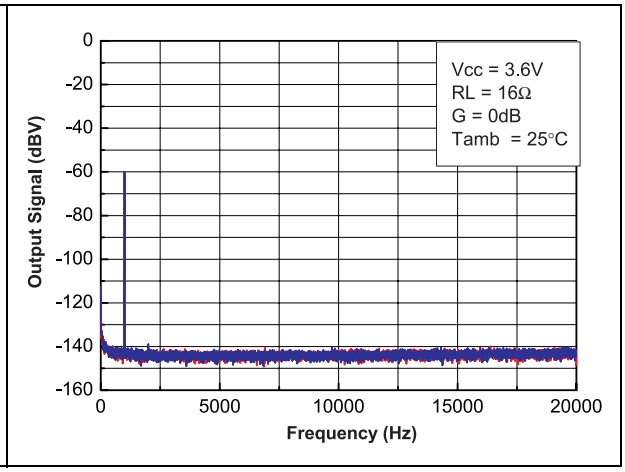


Figure 66. Crosstalk vs. frequency RL = 16 Ω

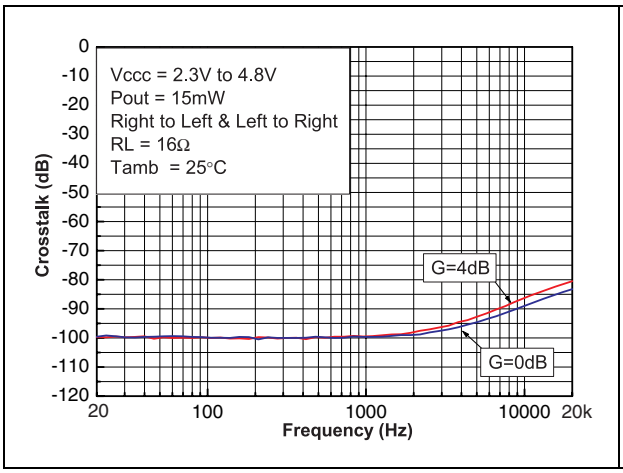


Figure 67. Crosstalk vs. frequency RL = 32 Ω

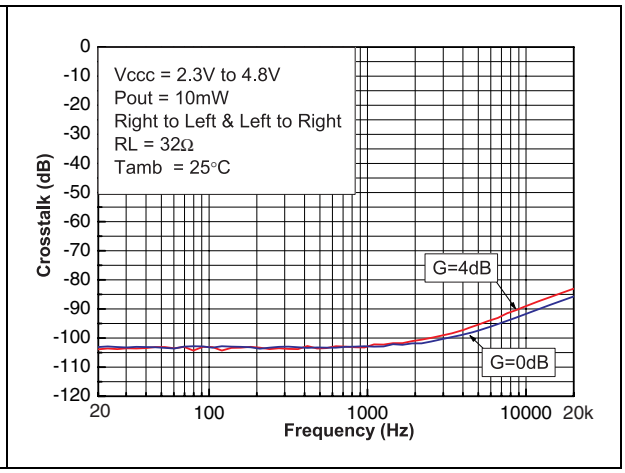


Figure 68. Crosstalk vs. frequency RL = 47 Ω

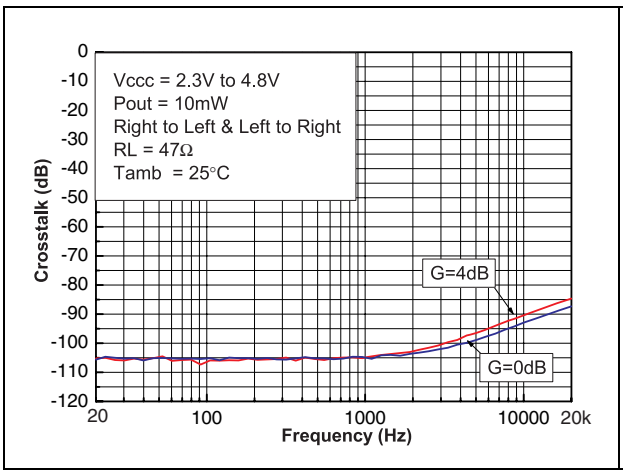


Figure 69. Crosstalk vs. frequency RL = 10 kΩ

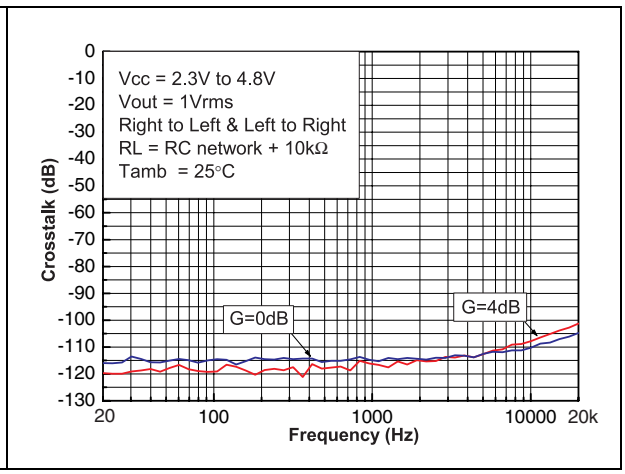


Figure 70. Wake-up time

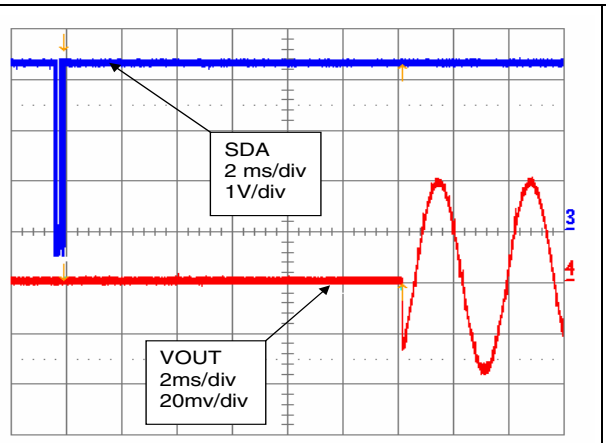
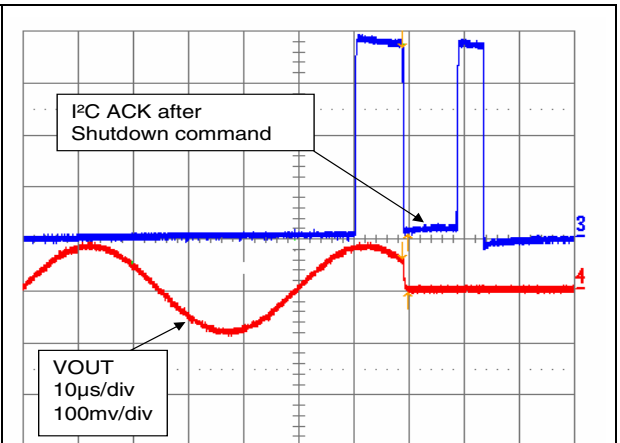


Figure 71. Shutdown time



4 Application information

4.1 I²C bus interface

In compliance with the I²C protocol, the TS4621B uses a serial bus to control the chip's functions with the clock (SCL) and data (SDA) wires. These two lines are bi-directional (open collector) and require an external pull-up resistor (typically 10 kΩ). The maximum clock frequency in fast mode specified by the I²C standard is 400 kHz, which the TS4621B supports. In this application, the TS4621B is always the slave device and the controlling microcontroller MCU is the master device.

The slave address of the TS4621B is 1100 000x (C0h).

Table 8 summarizes the pin descriptions for the I²C bus interface.

Table 8. Pin description of the I²C bus interface

Pin	Functional description
SDA	Serial data pin
SCL	Clock input pin

4.1.1 I²C bus operation

The host MCU can write to the TS4621B control register to control the TS4621B, and read from the control register to obtain a configuration from the TS4621B. The TS4621B is addressed by the byte consisting of the 7-bit slave address and the R/$\overline{W}$ bit.

Table 9. First byte after the START message for addressing the device

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	1	0	0	0	0	0	X

There are four control registers (*Table 10*) named CR1 to CR4. In read mode, all the control registers can be accessed. In write mode, only CR1, CR2 and CR3 can be addressed.

Table 10. Summary of control registers

Description	Register address	D7	D6	D5	D4	D3	D2	D1	D0
CR1	1	HP_EN_L	HP_EN_R	0	0	SC_L	SC_R	T_SH	SWS
CR2 volume control	2	Mute_L	Mute_R	Volume control					0
CR3	3	0	0	0	0	0	0	HiZ_L	HiZ_R
CR4 identification	4	0	1	0	0	0	0	0	0