Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

TS4621ML

High-performance class-G stereo headphone amplifier

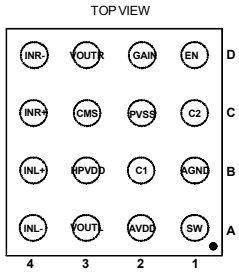
Datasheet – production data

Features

- Power supply range: 2.3 V to 4.8 V
- 0.6 mA/channel quiescent current
- 2.1 mA current consumption with 100 µW/channel (10 dB crest factor)
- 0.006% typical THD+N at 1 kHz
- 100 dB typical PSRR at 217 Hz
- 100 dB of SNR A-weighted at G = 0 dB
- Zero "pop and click"
- Gain settings : 0 dB and 6 dB
- Integrated high efficiency step-down converter
- Low standby current: 5 µA max
- Output-coupling capacitors removed
- Thermal shutdown
- Flip-chip package: 1.65 mm x 1.65 mm, 400 µm pitch, 16 bumps

TS4621MLEIJT - flip-chip

Pinout (top view)



Balls are underneath

Applications

- Cellular phones, smartphones
- Mobile internet devices
- PMP/MP3 players
- Portable CD/DVD players

Description

The TS4621ML is a class-G stereo headphone driver dedicated to high-performance audio, high-power efficiency and space-constrained applications.

It is based on the core technology of a low power dissipation amplifier combined with a high-efficiency step-down DC/DC converter for supplying this amplifier.

When powered by a battery, the internal step-down DC/DC converter generates the appropriate voltage to the amplifier depending on the amplitude of the audio signal to supply the headsets. It achieves a total 2.1 mA current consumption at 100 µW output power (10 dB crest factor).

THD+N is 0.02 % maximum at 1 kHz and PSRR is 100 dB at 217 Hz, which ensures a high audio quality of the device in a wide range of environments.

The traditionally bulky output coupling capacitors can be removed.

A dedicated common-mode sense pin removes parasitic ground noise.

The TS4621ML is designed to be used with an output serial resistor. It ensures unconditional stability over a wide range of capacitive loads.

The TS4621ML is packaged in a tiny 16-bump flip-chip package with a pitch of 400 µm.

Contents

List of figures

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1) during 1 ms.	5.5	V
V_{in+},V_{in-}	Input voltage referred to ground	+/- 1.2	V
Control input voltage	EN, Gain	-0.3 to VDD	V
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature(2)	150	°C
R_{thja}	Thermal resistance junction to ambient (3)	200	°C/W
P_d	Power dissipation	Internally limited(4)	
ESD	Human body model (HBM)(5) All pins VOUTR, VOUTL vs. AGND	 2 4	kV
	Machine model (MM), min. value(6)	100	V
	Charge device model (CDM) All pins VOUTR, VOUTL	 500 750	V
	IEC61000-4-2 level 4, contact(7) IEC61000-4-2 level 4, air discharge(7)	+/- 8 +/- 15	kV
	Lead temperature (soldering, 10 sec)	260	°C

1. All voltage values are measured with respect to the ground pin.
2. Thermal shutdown is activated when maximum junction temperature is reached.
3. The device is protected from overtemperature by a thermal shutdown mechanism, active at 150° C.
4. Exceeding the power derating curves for long periods may provoke abnormal operation.
5. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
6. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
7. The measurement is performed on an evaluation board, with ESD protection EMIF02-AV01F3.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.3 to 4.8	V
HPVDD	internal step-down DC output voltages High rail voltage Low rail voltage	 1.9 1.2	V
EN,GAIN	Input voltage low level	0.6 V max	V
EN,GAIN	Input voltage high level	1.3 V min	
R_L	Load resistor	≥ 16	Ω
C_L	Load capacitor Serial resistor of 12 Ω minimum, R_L ≥ 16 Ω	 0.8 to 100	nF
T_{oper}	Operating free air temperature range	-40 to +85	°C
R_{thja}	Flip-chip thermal resistance junction to ambient	90	°C/W

2 Typical application schematic

Figure 1. Typical application schematic for the TS4621ML

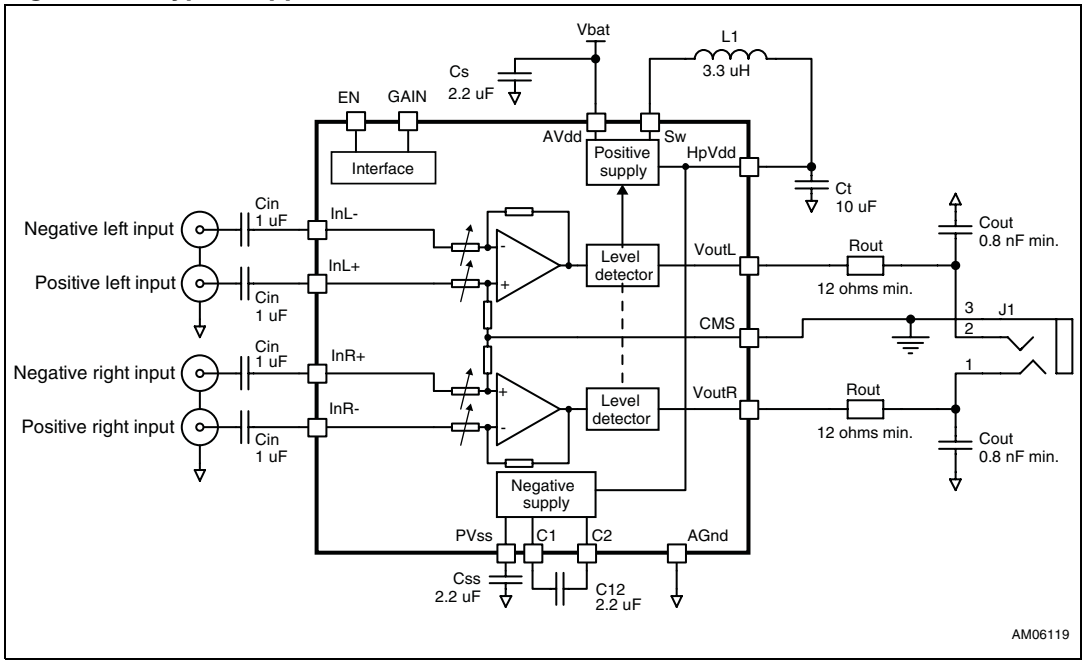


Table 3. TS4621ML pin description

Pin number	Pin name	Pin definition
A1	SW	Switching node of the buck converter
A2	AVDD	Analog supply voltage, connect to battery
A3	VOUTL	Output signal for left audio channel
A4	INL-	Negative input signal for left audio channel
B1	AGND	Device ground
B2	C1	Flying capacitor terminal for internal negative supply generator
B3	HPVDD	Buck converter output, power supply for amplifier
B4	INL+	Positive input signal for left audio channel
C1	C2	Flying capacitor terminal for internal negative supply generator
C2	PVSS	Negative supply generator output
C3	CMS	Common-mode sense, to be connected as close as possible to the ground of headphone/line out plug
C4	INR+	Positive input signal for right audio channel
D1	EN	Amplifier enable
D2	GAIN	Amplifier gain select
D3	VOUTR	Output signal for right audio channel
D4	INR-	Negative input signal for right audio channel

Table 4. TS4621ML component description

Component(1)	Value	Description
Cs	2.2 µF	Decoupling capacitors for V_{CC}. A 2.2 µF capacitor is sufficient for proper decoupling of the TS4621ML. An X5R dielectric and 10 V rating voltage is recommended to minimize ΔC/ΔV when V_{CC} = 4.8 V. Must be placed as close as possible to the TS4621ML to minimize parasitic inductance and resistance.
C12	2.2 µF	Capacitor for internal negative power supply operation. An X5R dielectric and 6.3 V rating voltage is recommended to minimize ΔC/ΔV when HPVDD = 1.9 V. Must be placed as close as possible to the TS4621ML to minimize parasitic inductance and resistance.
C_{SS}	2.2 µF	Filtering capacitor for internal negative power supply. An X5R dielectric and 6.3 V rating voltage is recommended to minimize ΔC/ΔV when HPVDD = 1.9 V.
C_{in}	$Cin = \frac{1}{2 \times \pi \times Rin \times Fc}$	Input coupling capacitor that forms with $R_{in} \approx R_{indiff}/2$ a first-order high-pass filter with a -3 dB cut-off frequency Fc.
C_{out}	0.8 to 100 nF	Output capacitor of 0.8 nF minimum to 100 nF maximum. This capacitor is mandatory for operation of the TS4621ML.
R_{out}	12 Ω min.	Output resistor in-series with the TS4621ML output. This 12 Ω minimum resistor is mandatory for operation of the TS4621ML.
L1	3.3 µH	Inductor for internal DC/DC step-down converter. References of inductors: refer to *Section 4.3.1* for more information.
C_t	10 µF	Tank capacitor for internal DC/DC step-down converter. An X5R dielectric and 6.3 V rating voltage is recommended to minimize ΔC/ΔV when HPVDD = 1.9 V. Refer to *Section 4.3.2* for more information.

1. Refer to *Section 4.3* for a complete description of each component.

3 Electrical characteristics

The values given in the following table are for the conditions V_{CC} = +3.6 V, AGND = 0 V, GAIN = 0 dB, R_L= 32 Ω + 15 Ω, T_{amb} = 25° C, unless otherwise specified.

Table 5. Electrical characteristics of the amplifier

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Quiescent supply current, no input signal, both channels enabled		1.2	1.5	mA
I_s	Supply current, with input modulation, both channels enabled, HPVDD = 1.2 V, output power per channel, F= 1 kHz Pout = 100 µW at 3 dB crest factor Pout = 500 µW at 3 dB crest factor Pout = 1 mW at 3 dB crest factor Pout = 100 µW at 10 dB crest factor Pout = 500 µW at 10 dB crest factor Pout = 1 mW at 10 dB crest factor		 2.3 3.7 4.7 2.1 3.1 3.9	 3.5 5 6.5	mA
I_{STBY}	Standby current, no input signal, V_{EN} = 0 V, V_{GAIN}=0V		0.6	5	µA
V_{in}	Input differential voltage range(1)			1	V_{rms}
V_{oo}	Output offset voltage No input signal	-500		+500	µV
V_{out}	Maximum output voltage, in-phase signals R_L = 16 Ω, THD+N = 1% max, f = 1 kHz R_L = 47 Ω, THD+N = 1% max, f = 1 kHz R_L = 10 kΩ, R_s = 15 Ω, C_L = 1 nF, THD+N = 1% max, f = 1 kHz	 0.6 1.0 1.0	 0.8 1.1 1.3		V_{rms}
THD+N	Total harmonic distortion + noise, G = 0 dB V_{out} = 700 mVrms, F = 1 kHz V_{out} = 700 mVrms, 20 Hz < F < 20 kHz		 0.006 0.05	0.02	%
PSRR	Power supply rejection ratio(1), V_{ripple} = 200 mV_{pp}, grounded inputs F = 217 Hz, G = 0 dB, R_L ≥16 Ω F = 10 kHz, G = 0 dB, R_L ≥16 Ω	90	100 70		dB
CMRR	Common mode rejection ratio F = 1 kHz, G = 0 dB, V_{ic} = 200 mV_{pp} F = 20 Hz to 20 kHz, G = 0 dB, V_{ic} = 200 mV_{pp}		 65 45		dB
Crosstalk	Channel separation R_L = 32 Ω + 15 Ω , G = 0 dB, F = 1 kHz, P_o = 10 mW	60	100		dB
SNR	Signal-to-noise ratio, A-weighted, V_{out} = 1 V_{rms}, THD+N < 1%, F = 1 kHz(1) G = +0 dB	 100			dB
ONoise	Output noise voltage, A-weighted (1) G = +0 dB			9	µVrms

Table 5. Electrical characteristics of the amplifier (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
AV	Closed loop voltage gain, GAIN=L		0		dB
	Closed loop voltage gain, GAIN=H		6		dB
ΔAV	Gain matching between left and right channels	-0.5		+0.5	dB
R_{indiff}	Differential input impedance at 6 dB	24	33.2		kΩ
V_{IL}	Low level input voltage on EN, GAIN pins			0.6	V
V_{IH}	High level input voltage on EN, GAIN pins	1.3			V
I_{in}	Input current on EN,GAIN			10	µA

1. Guaranteed by design and parameter correlation.

Figure 2. Current consumption vs. power supply voltage

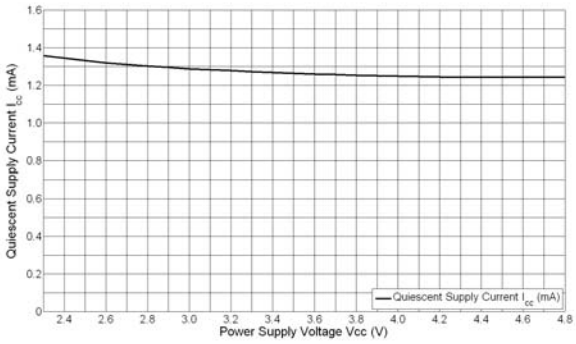


Figure 3. Standby current consumption vs. power supply voltage

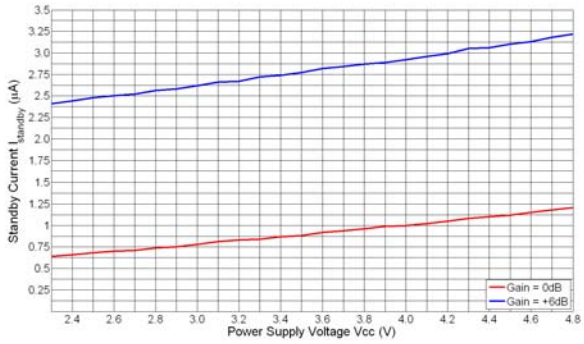


Figure 4. Maximum output power vs. power supply voltage, R_L = 16 Ω

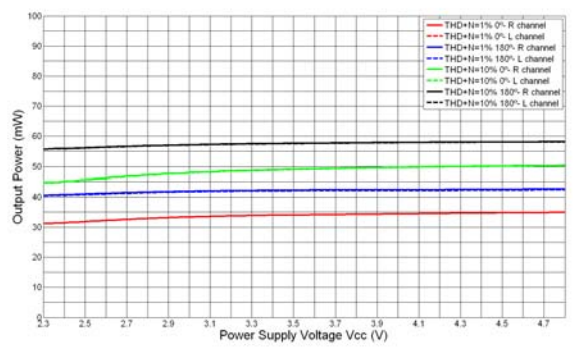


Figure 5. Maximum output power vs. power supply voltage, R_L = 32 Ω

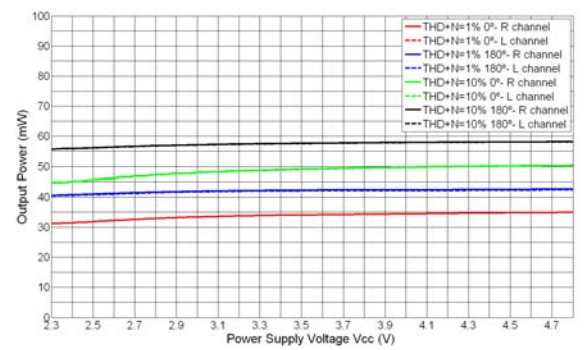


Figure 6. Maximum output power vs. power supply voltage, R_L = 47 Ω

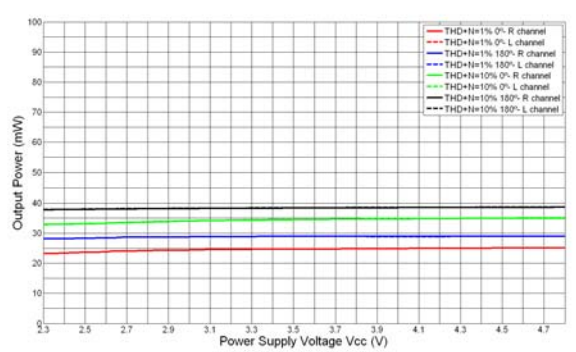


Figure 7. Current consumption vs. total output power, R_L = 16 Ω

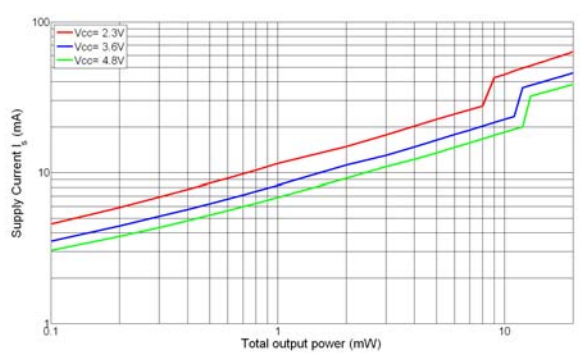


Figure 8. Current consumption vs. total output power, R_L = 32 Ω

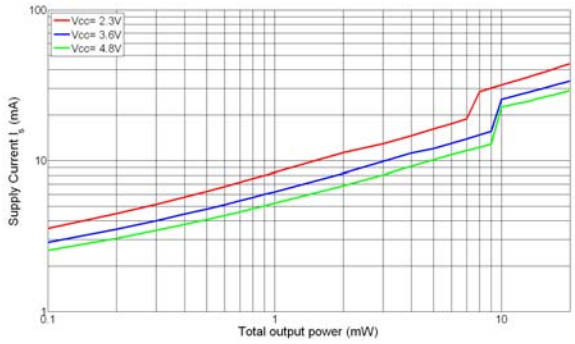


Figure 9. Current consumption vs. total output power, R_L = 47 Ω

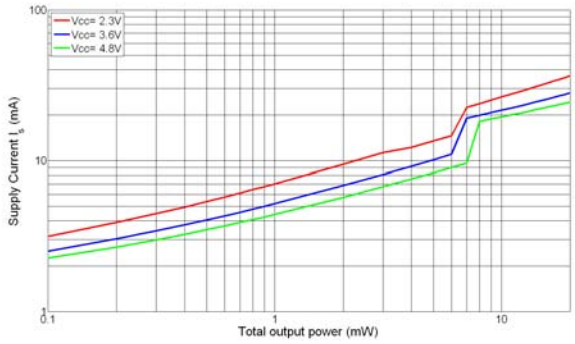


Figure 10. Differential input impedance vs. gain

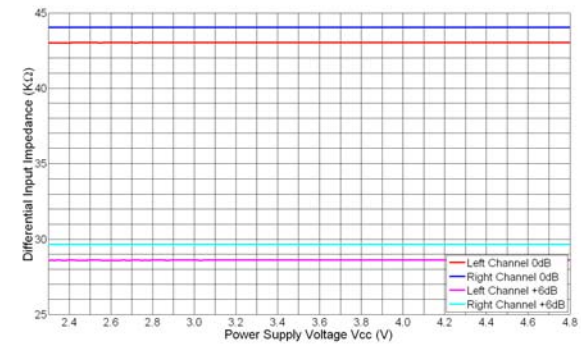


Figure 11. THD+N vs. output power - R_L = 16 Ω, in-phase, V_{CC} = 2.5 V

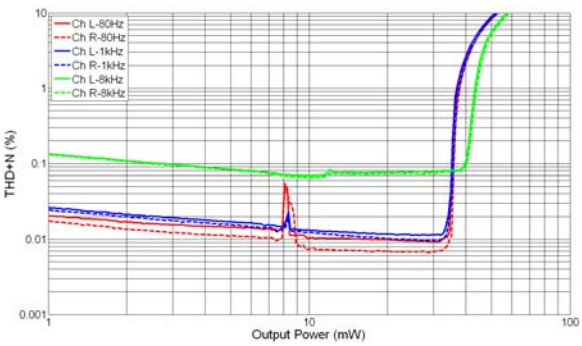


Figure 12. THD+N vs. output power - R_L = 16 Ω, out-of-phase, V_{CC} = 2.5 V

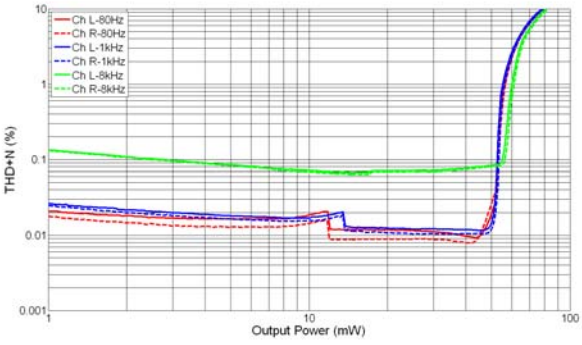


Figure 13. THD+N vs. output power - R_L = 16 Ω, in-phase, V_{CC} = 3.6 V

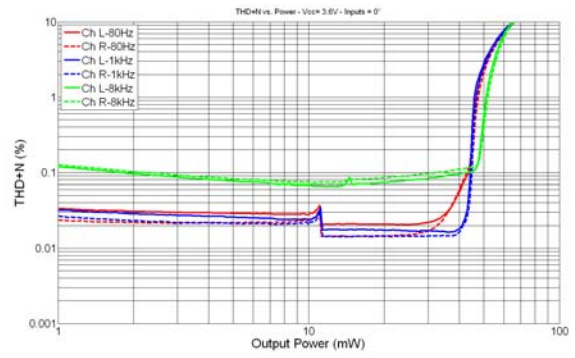


Figure 14. THD+N vs. output power - R_L = 16 Ω, out-of-phase, V_{CC} = 3.6 V

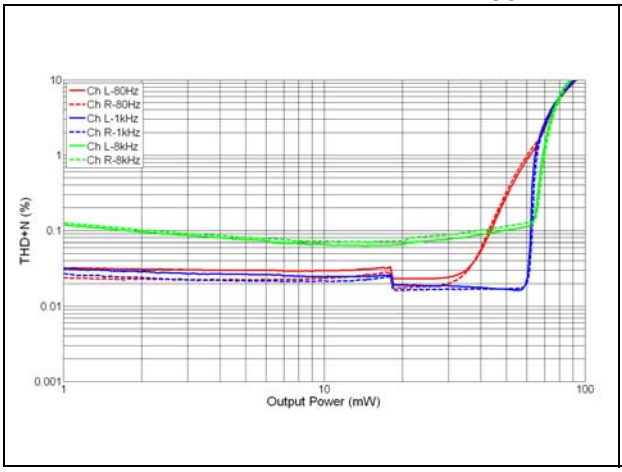


Figure 15. THD+N vs. output power - R_L = 16 Ω, in-phase, V_{CC} = 4.8 V

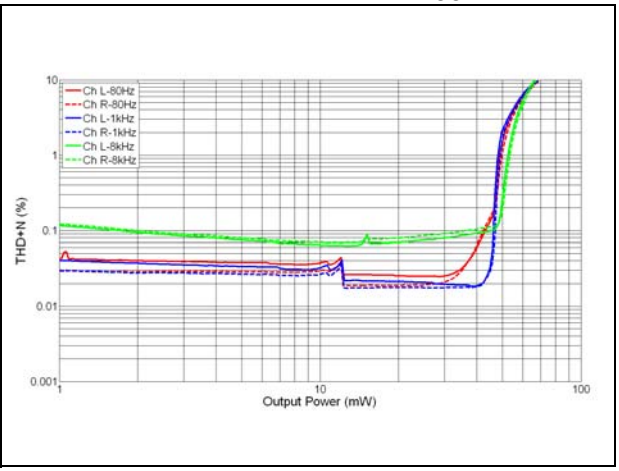


Figure 16. THD+N vs. output power - R_L = 16 Ω, out-of-phase, V_{CC} = 4.8 V

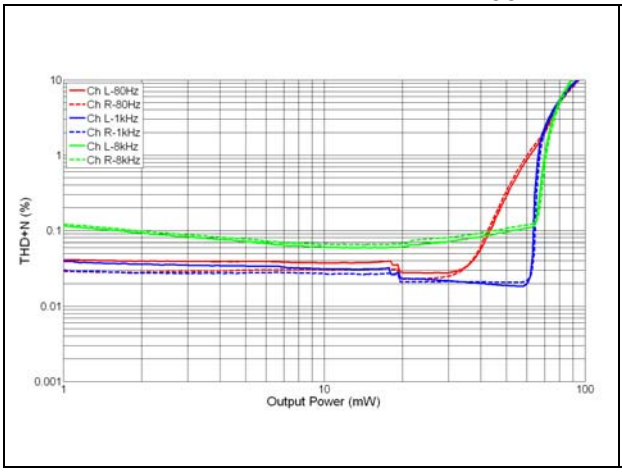


Figure 17. THD+N vs. output power - R_L = 32 Ω, in-phase, V_{CC} = 2.5 V

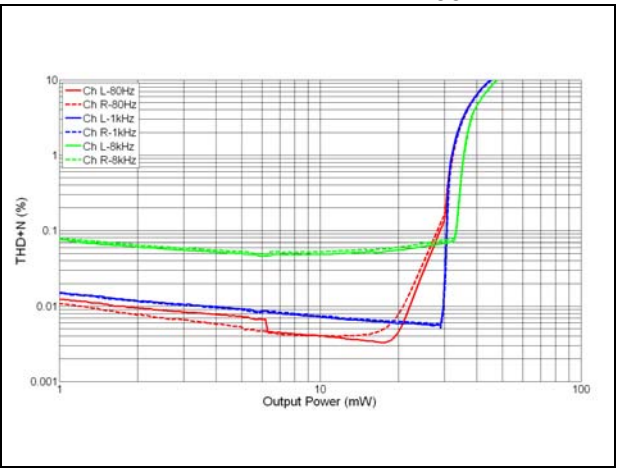


Figure 18. THD+N vs. output power - R_L = 32 Ω, out-of-phase, V_{CC} = 2.5 V

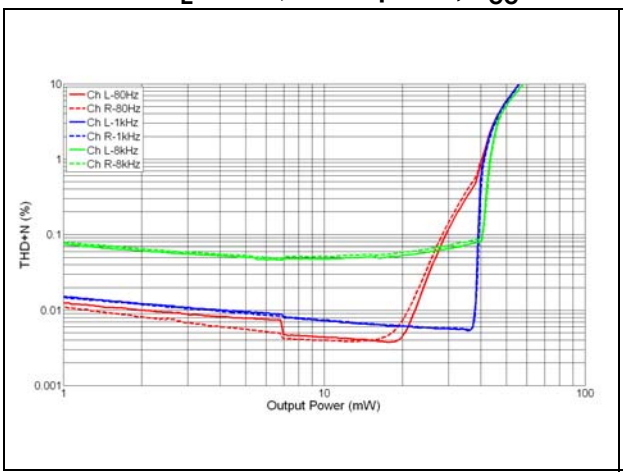


Figure 19. THD+N vs. output power - R_L = 32 Ω, in-phase, V_{CC} = 3.6 V

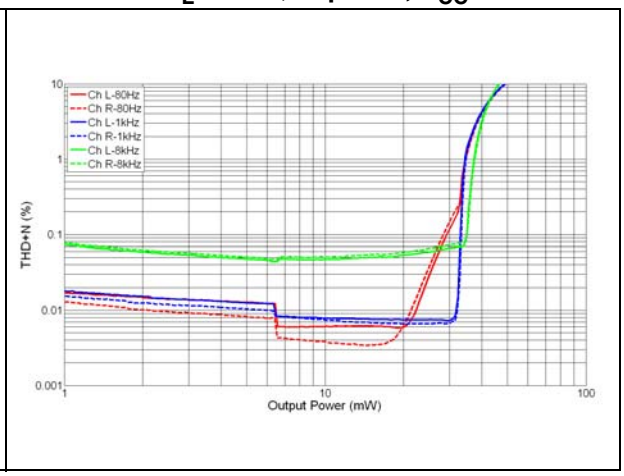


Figure 20. THD+N vs. output power - R_L = 32 Ω, out-of-phase, V_{CC} = 3.6 V

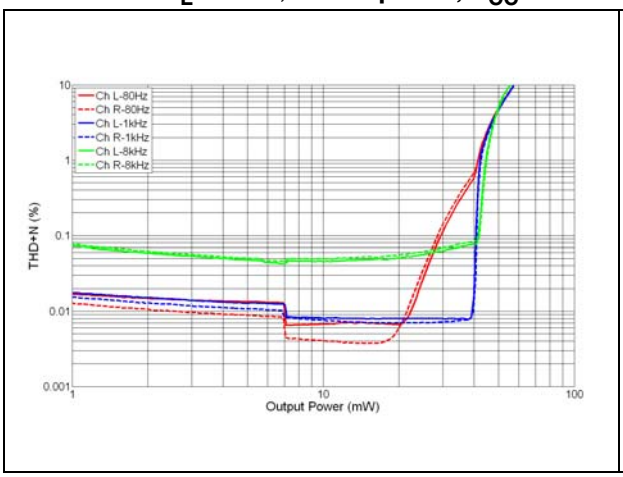


Figure 21. THD+N vs. output power - R_L = 32 Ω, in-phase, V_{CC} = 4.8 V

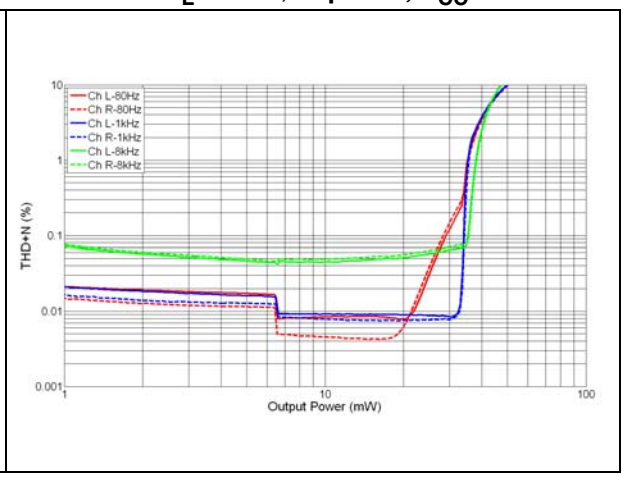


Figure 22. THD+N vs. output power - R_L = 32 Ω, out-of-phase, V_{CC} = 4.8 V

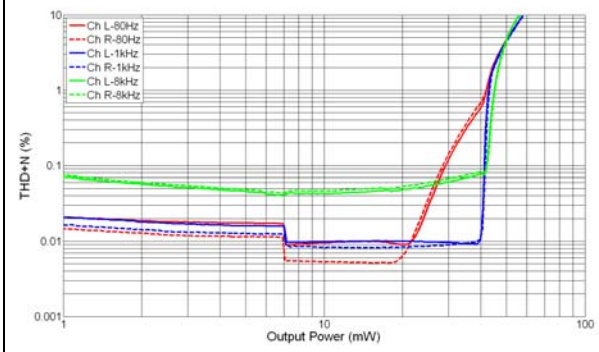


Figure 23. THD+N vs. output power - R_L = 32 Ω+IPad, in-phase, V_{CC} = 2.5 V

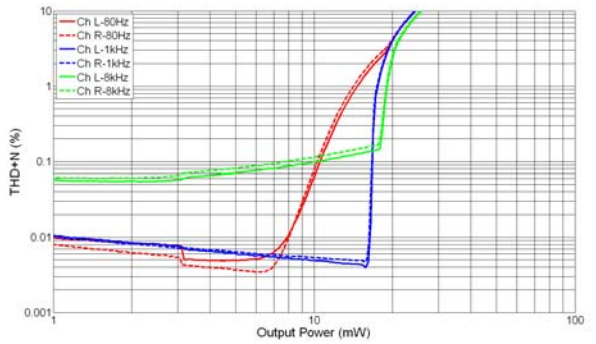


Figure 24. THD+N vs. output power - R_L = 32 Ω+IPad, out-of-phase, V_{CC} = 2.5 V

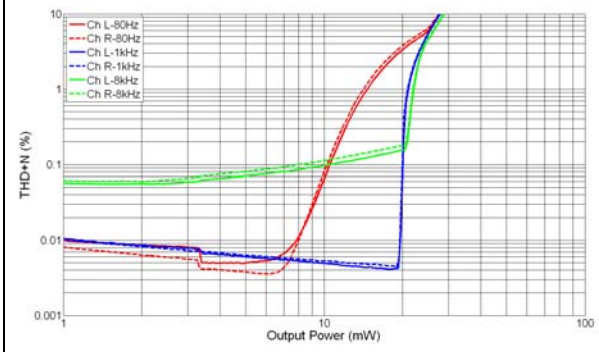


Figure 25. THD+N vs. output power - R_L = 32 Ω+IPad, in-phase, V_{CC} = 3.6 V

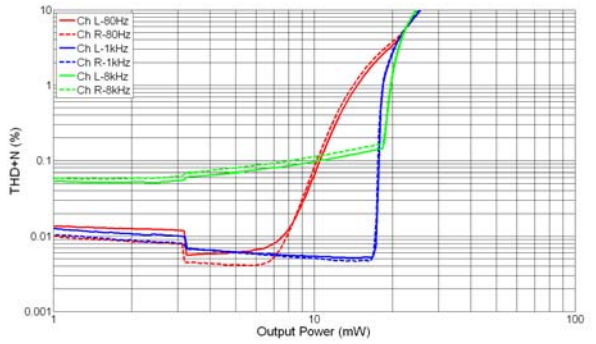


Figure 26. THD+N vs. output power - R_L = 32 Ω+IPad, out-of-phase, V_{CC} = 3.6 V

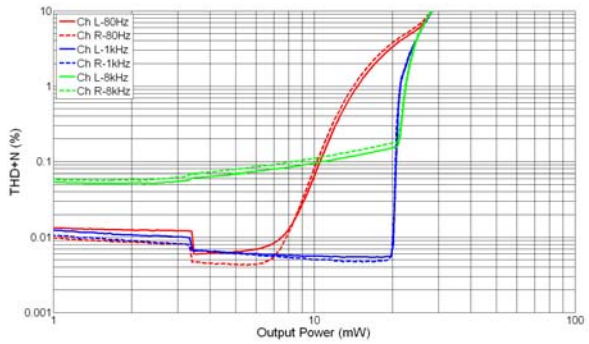


Figure 27. THD+N vs. output power - R_L = 32 Ω+IPad, in-phase, V_{CC} = 4.8 V

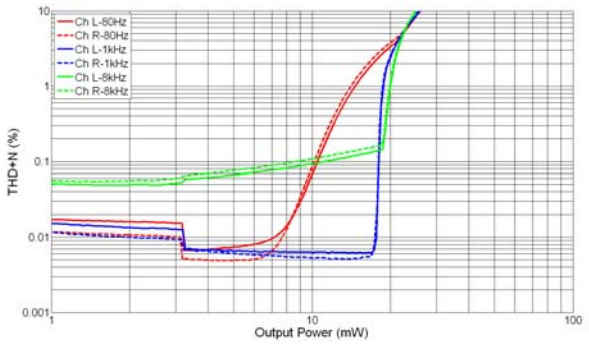


Figure 28. THD+N vs. output power - R_L = 32 Ω+IPad, out-of-phase, V_{CC} = 4.8 V

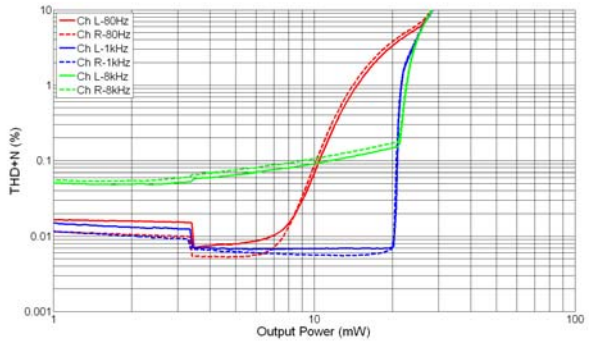


Figure 29. THD+N vs. output power - R_L = 47 Ω, in-phase, V_{CC} = 2.5 V

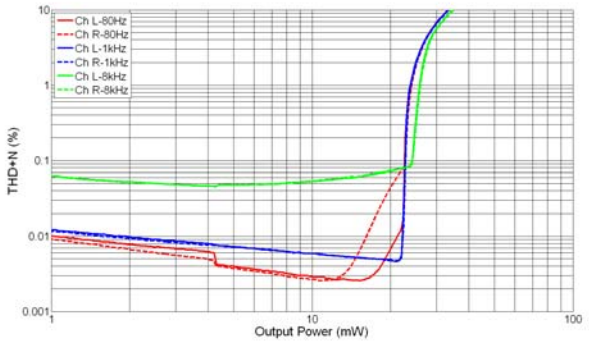


Figure 30. THD+N vs. output power - R_L = 47 Ω, out-of-phase, V_{CC} = 2.5 V

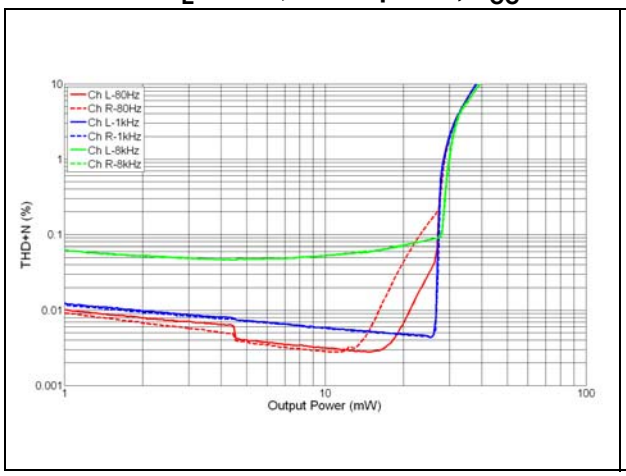


Figure 31. THD+N vs. output power - R_L = 47 Ω, in-phase, V_{CC} = 3.6 V

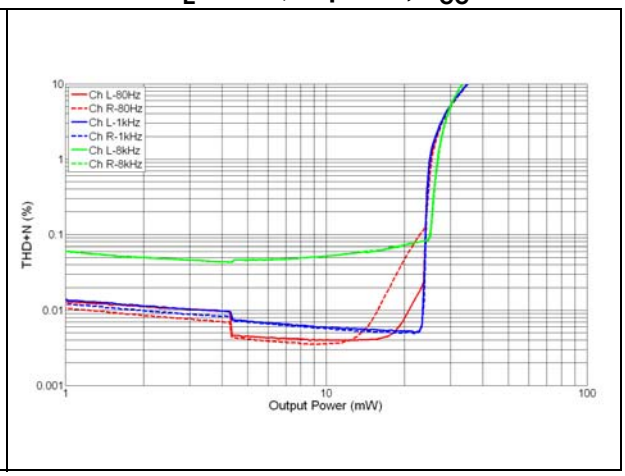


Figure 32. THD+N vs. output power - R_L = 47 Ω, out-of-phase, V_{CC} = 3.6 V

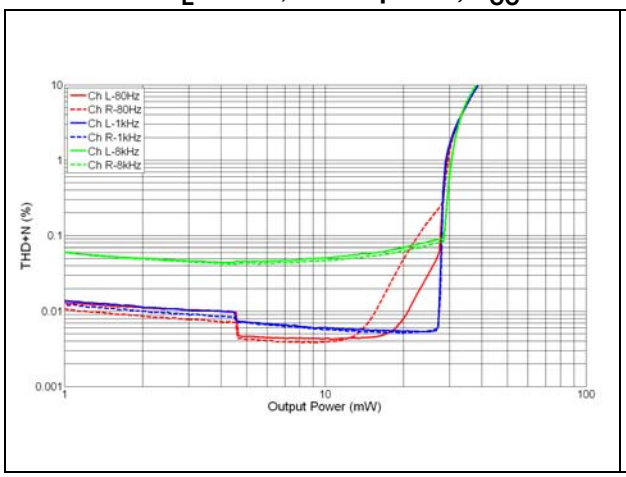


Figure 33. THD+N vs. output power - R_L = 47 Ω, in-phase, V_{CC} = 4.8 V

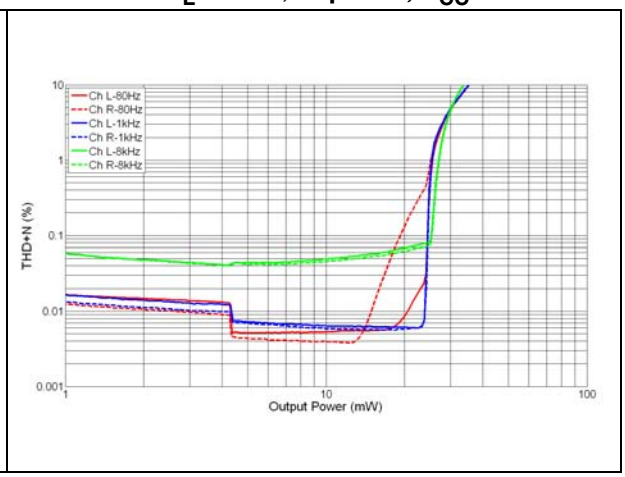


Figure 34. THD+N vs. output power - R_L = 47 Ω, out-of-phase, V_{CC} = 4.8 V

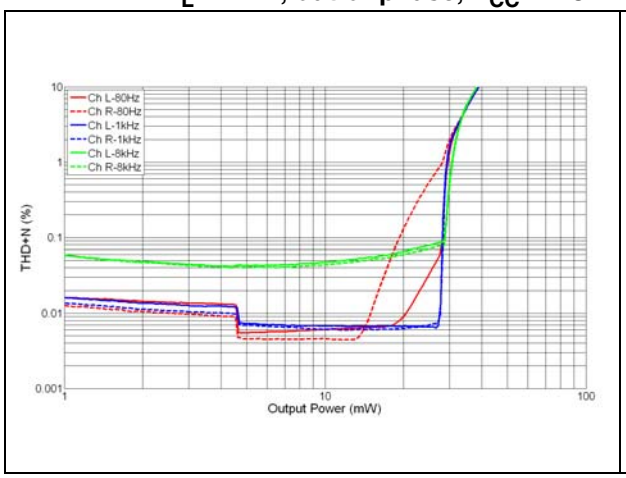


Figure 35. THD+N vs. frequency, R_L = 16 Ω, in-phase, V_{CC} = 2.5 V

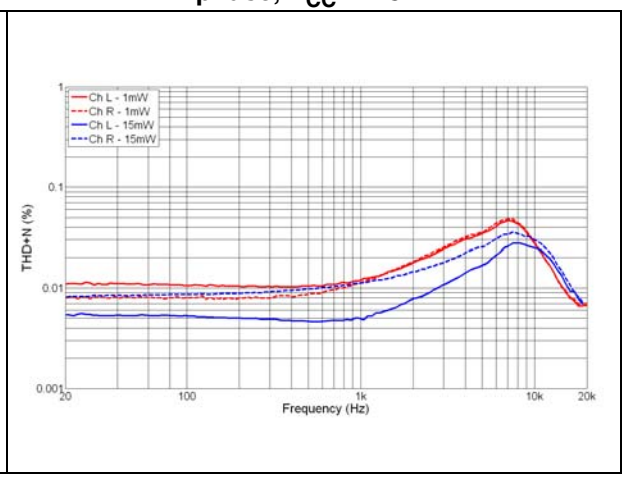


Figure 36. THD+N vs. frequency, R_L = 16 Ω, out-of-phase, V_{CC} = 2.5 V

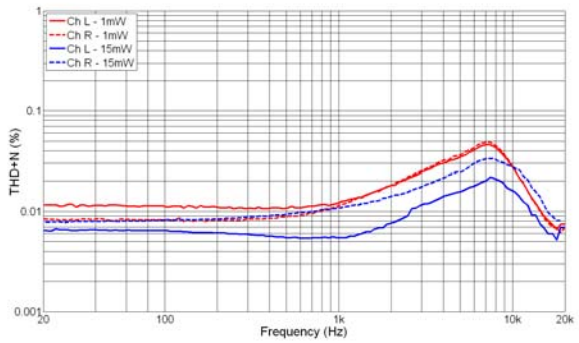


Figure 37. THD+N vs. frequency, R_L = 16 Ω, in-phase, V_{CC} = 3.6 V

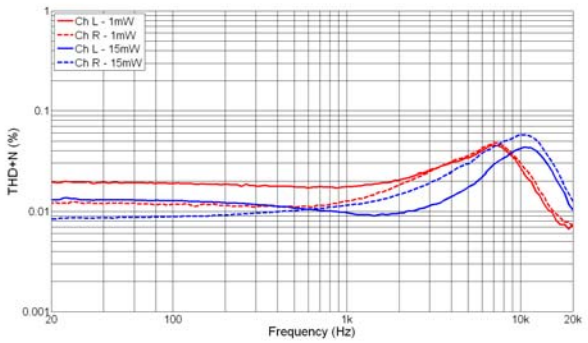


Figure 38. THD+N vs. frequency, R_L = 16 Ω, out-of-phase, V_{CC} = 3.6 V

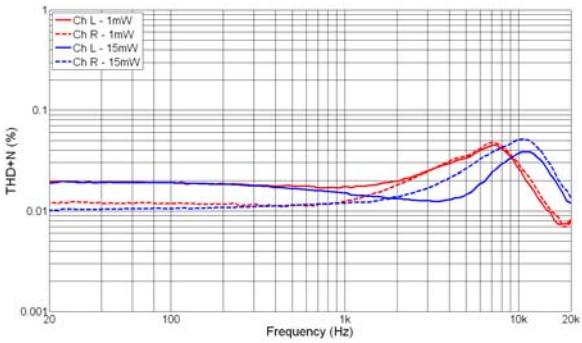


Figure 39. THD+N vs. frequency, R_L = 16 Ω, in-phase, V_{CC} = 4.8 V

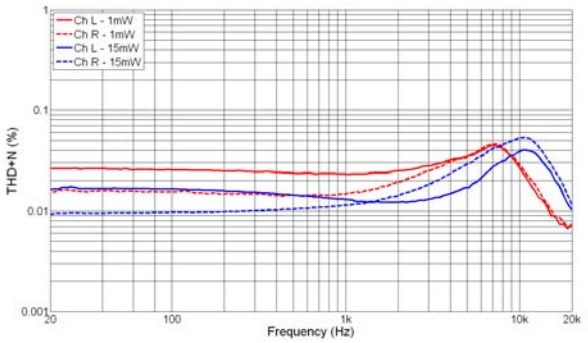


Figure 40. THD+N vs. frequency, R_L = 16 Ω, out-of-phase, V_{CC} = 4.8 V

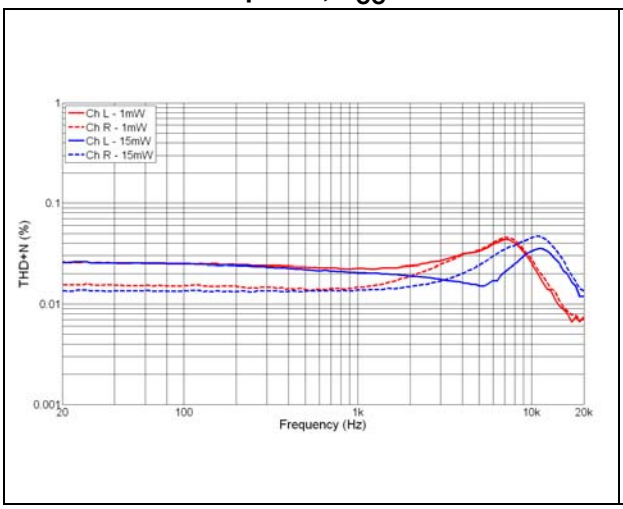


Figure 41. THD+N vs. frequency, R_L = 32 Ω, in-phase, V_{CC} = 2.5 V

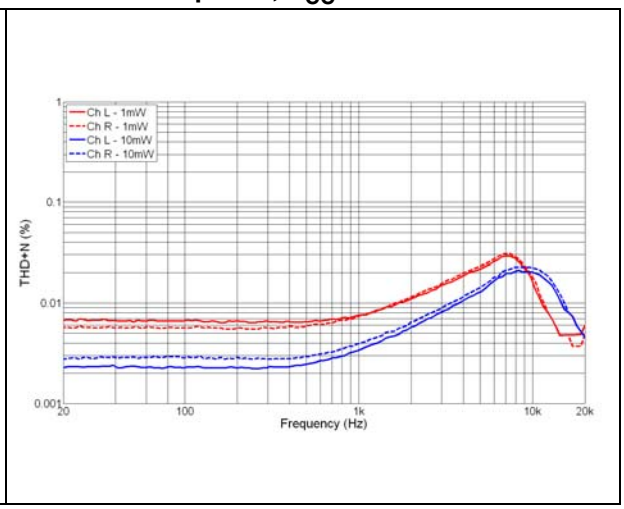


Figure 42. THD+N vs. frequency, R_L = 32 Ω, out-of-phase, V_{CC} = 2.5 V

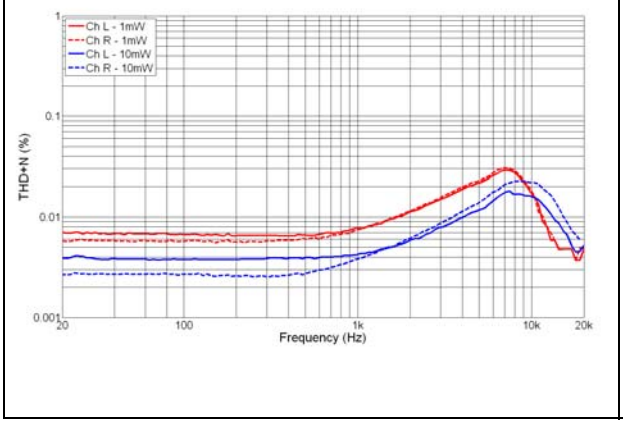


Figure 43. THD+N vs. frequency, R_L = 32 Ω, in-phase, V_{CC} = 3.6 V

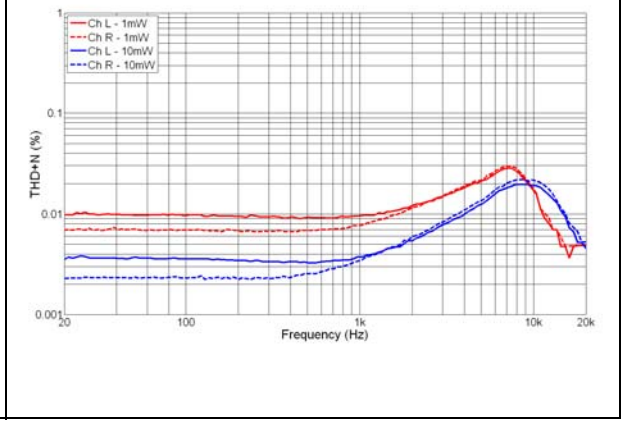


Figure 44. THD+N vs. frequency, R_L = 32 Ω, out-of-phase, V_{CC} = 3.6 V

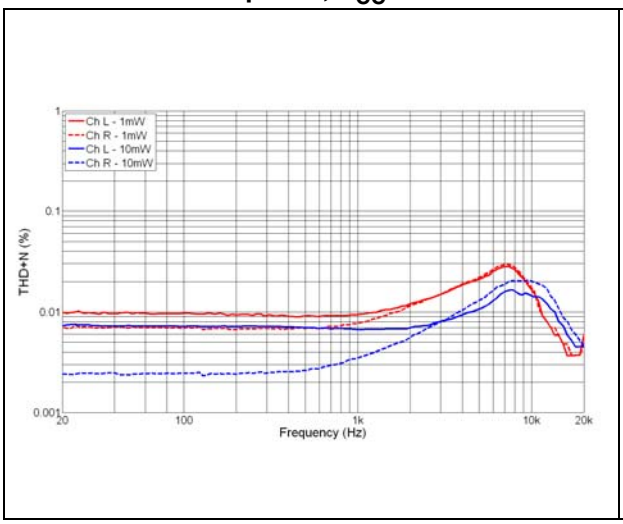


Figure 45. THD+N vs. frequency, R_L = 32 Ω, in-phase, V_{CC} = 4.8 V

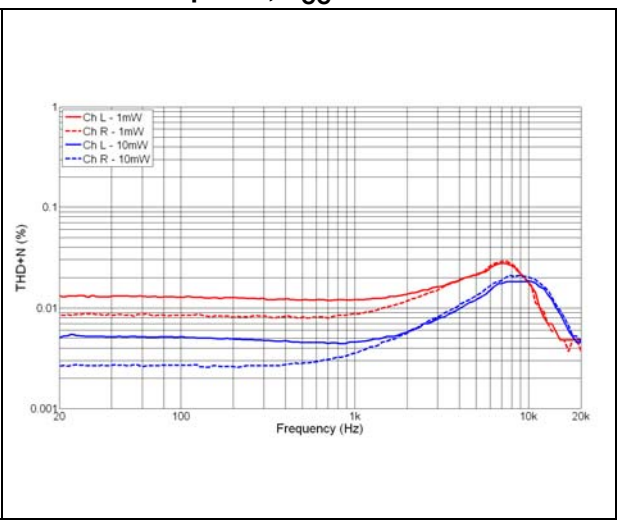


Figure 46. THD+N vs. frequency, R_L = 32 Ω, out-of-phase, V_{CC} = 4.8 V

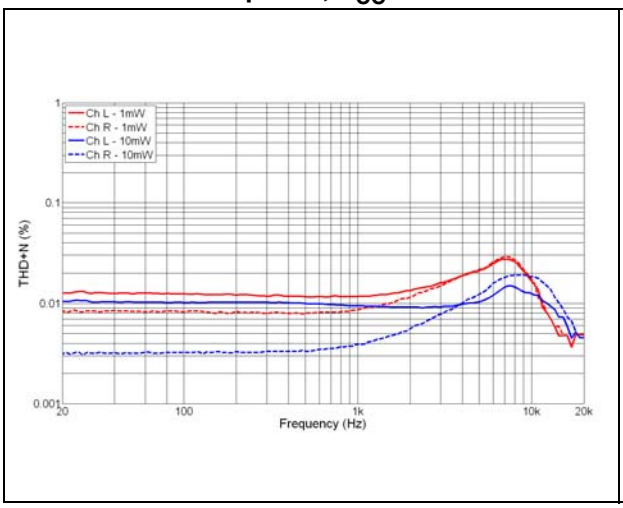


Figure 47. THD+N vs. frequency, R_L = 47 Ω, in-phase, V_{CC} = 2.5 V

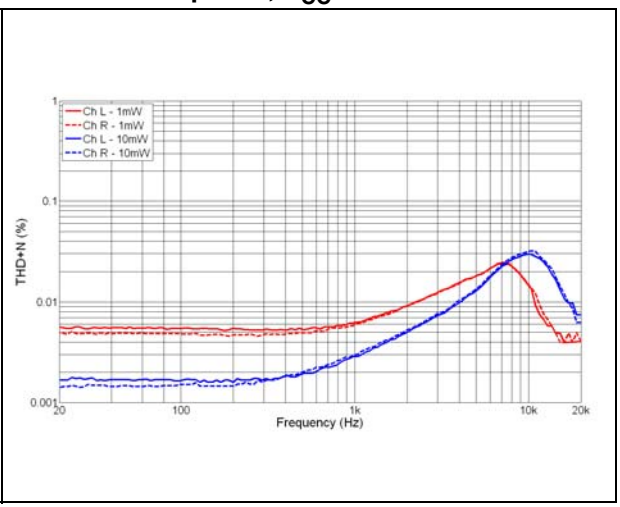


Figure 48. THD+N vs. frequency, R_L = 47 Ω, out-of-phase, V_{CC} = 2.5 V

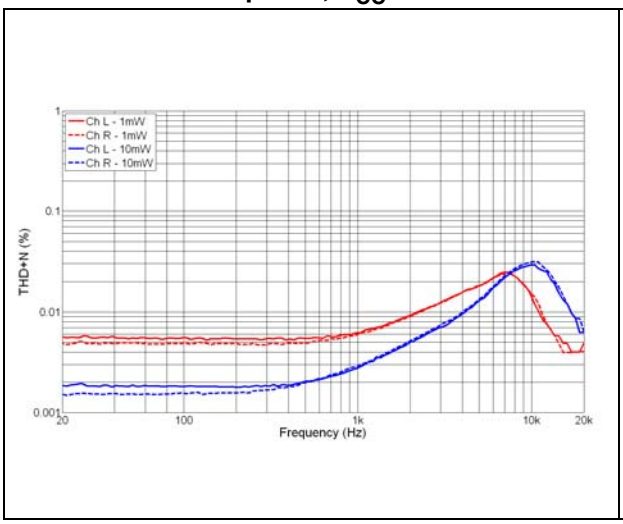


Figure 49. THD+N vs. frequency, R_L = 47 Ω, in-phase, V_{CC} = 3.6 V

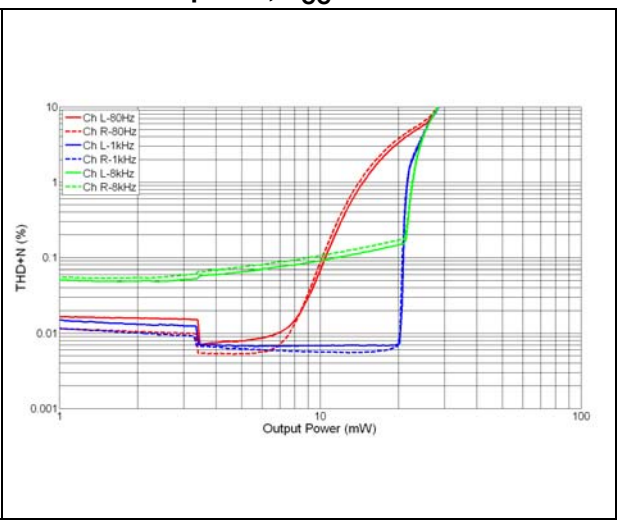


Figure 50. THD+N vs. frequency, R_L = 47 Ω, out-of-phase, V_{CC} = 3.6 V

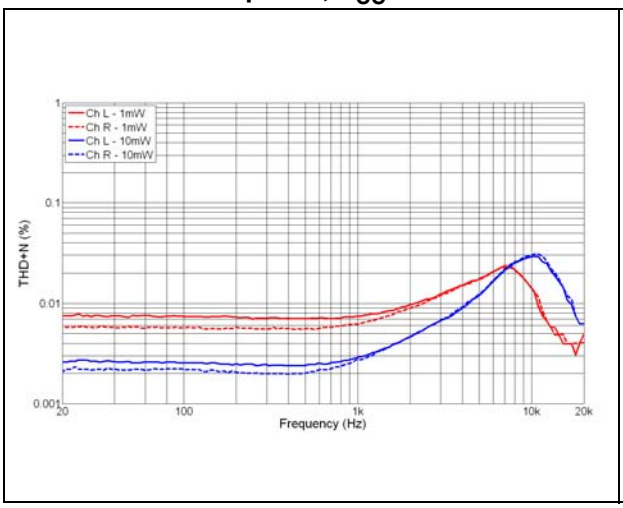


Figure 51. THD+N vs. frequency, R_L = 47 Ω, in-phase, V_{CC} = 4.8 V

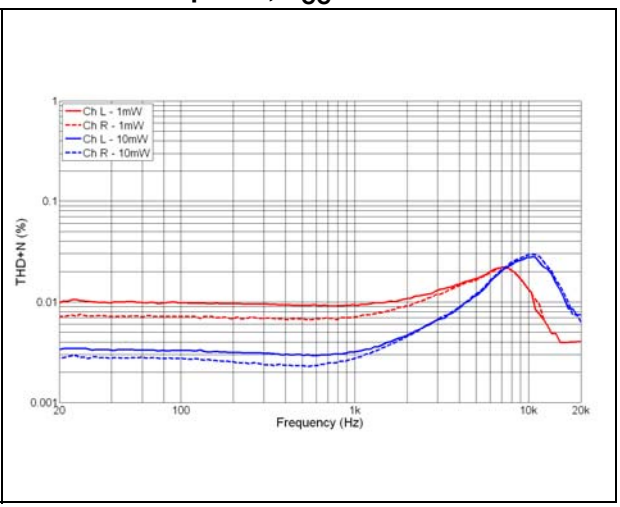


Figure 52. THD+N vs. frequency, R_L = 47 Ω, out-of-phase, V_{CC} = 4.8 V

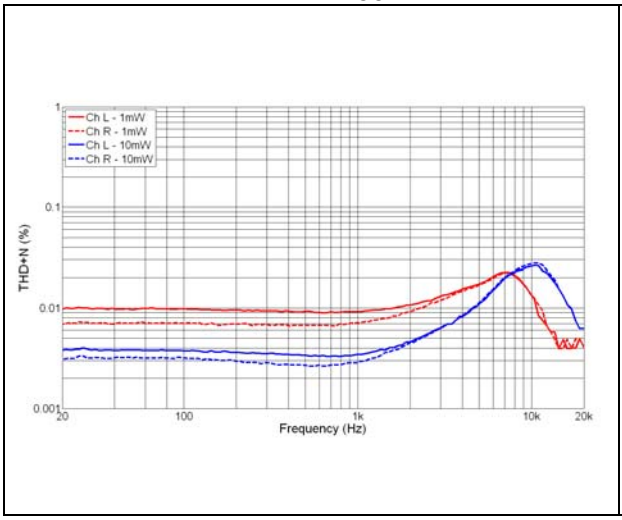


Figure 53. PSRR vs. frequency - V_{CC} = 3.6 V, gain = 0 dB

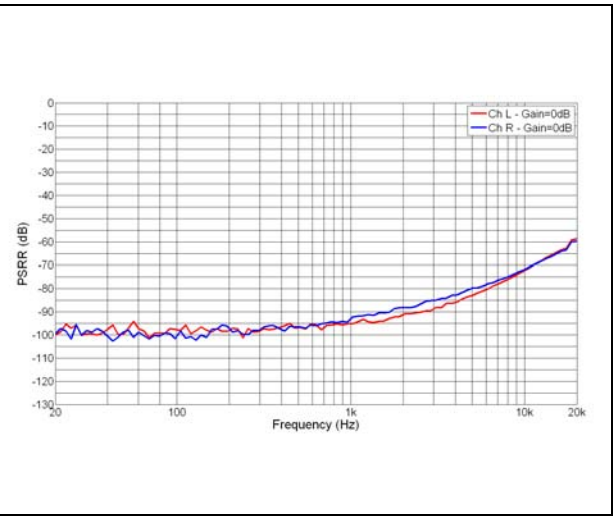


Figure 54. PSRR vs. frequency - V_{CC} = 3.6 V, gain = +6 dB

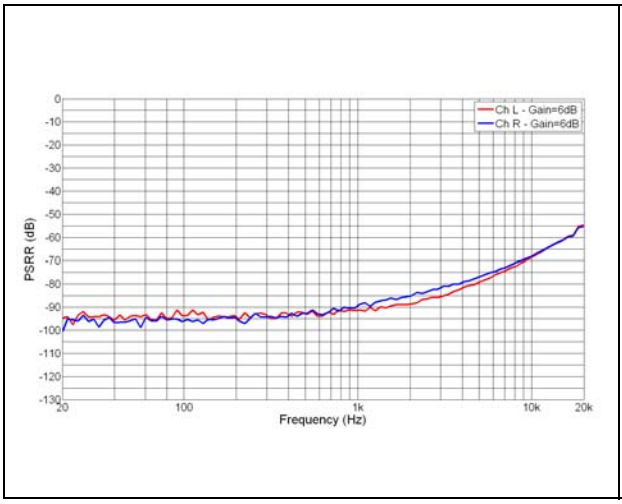


Figure 55. Output signal spectrum (V_{CC} = 3.6 V, load = 32 Ω)

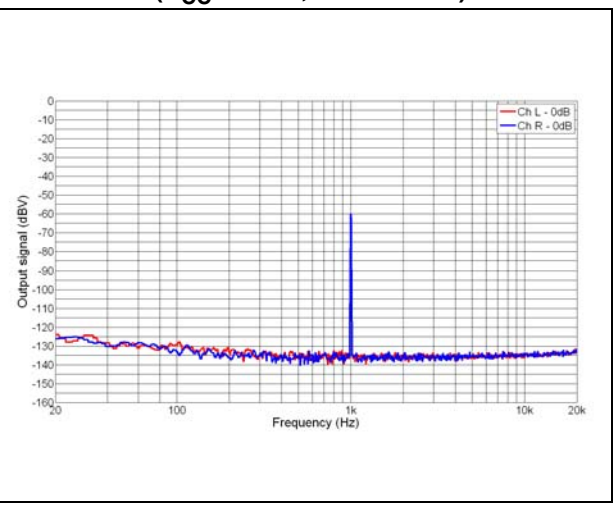


Figure 56. Crosstalk vs. frequency - R_L = 32 Ω, V_{CC} = 3.6 V, gain = 0 dB

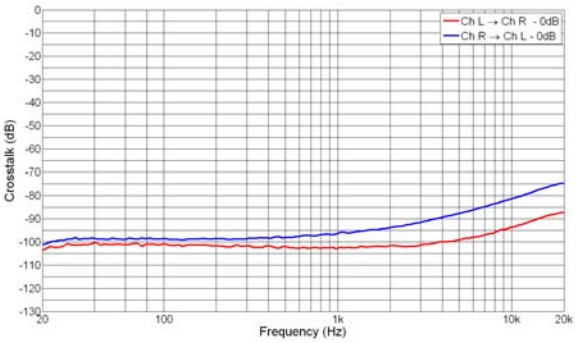


Figure 57. Crosstalk vs. frequency - R_L = 32 Ω, V_{CC} = 3.6 V, gain = +6 dB

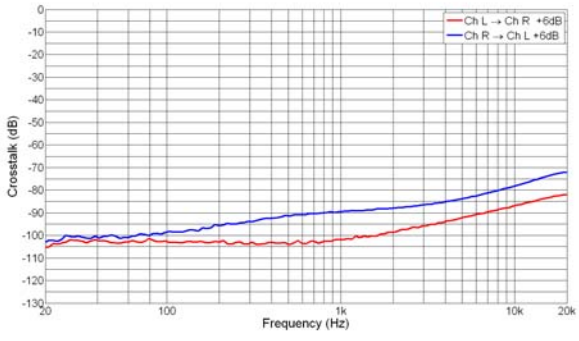


Figure 58. Crosstalk vs. frequency - R_L = 47 Ω, V_{CC} = 3.6 V, gain = 0 dB

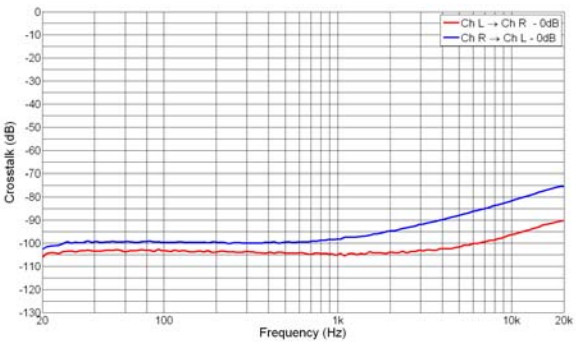


Figure 59. Crosstalk vs. frequency - R_L = 47 Ω, V_{CC} = 3.6 V, gain = +6 dB

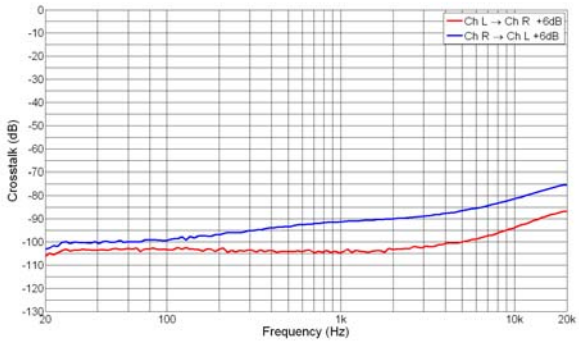


Figure 60. CMRR vs. frequency, 32 Ω, V_{CC} = 36 V, 0 dB

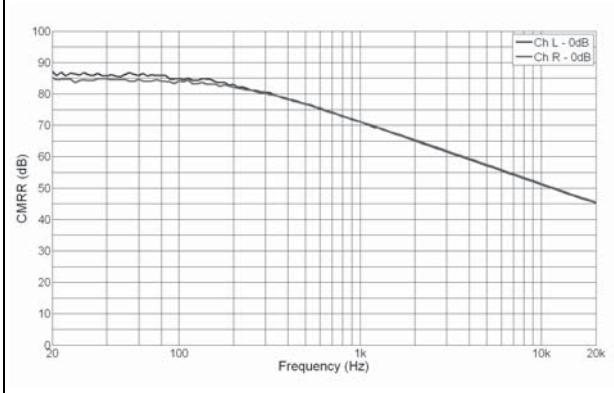


Figure 61. CMRR vs. frequency, 32 Ω, V_{CC} = 36 V, 6 dB

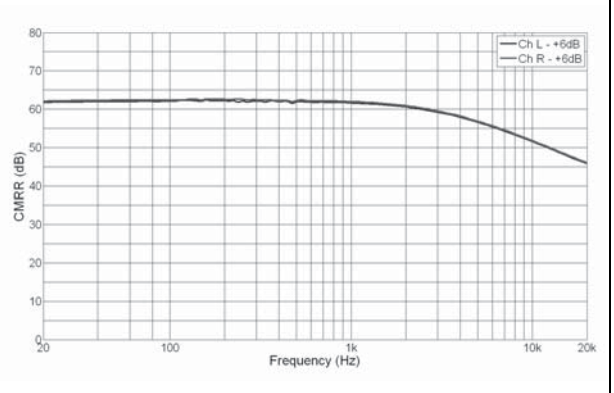


Figure 62. Wake-up time

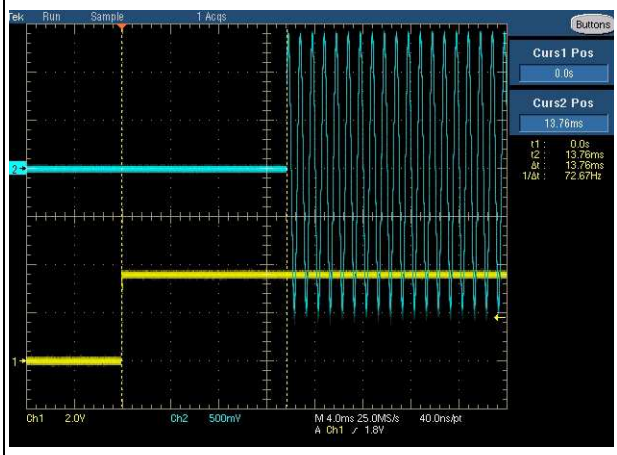
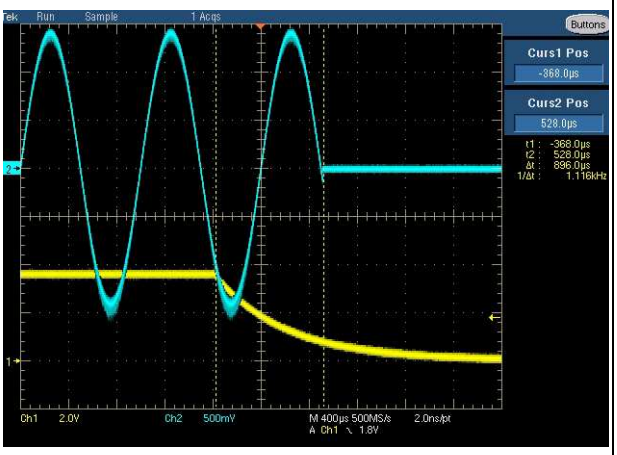


Figure 63. Shutdown



4 Application information

4.1 Gain control

The TS4621ML has two gain settings which are controlled via the GAIN pin:

GAIN voltage	Amplifier gain
≤ 0.6 V	0 dB
≥ 1.3 V	6 dB

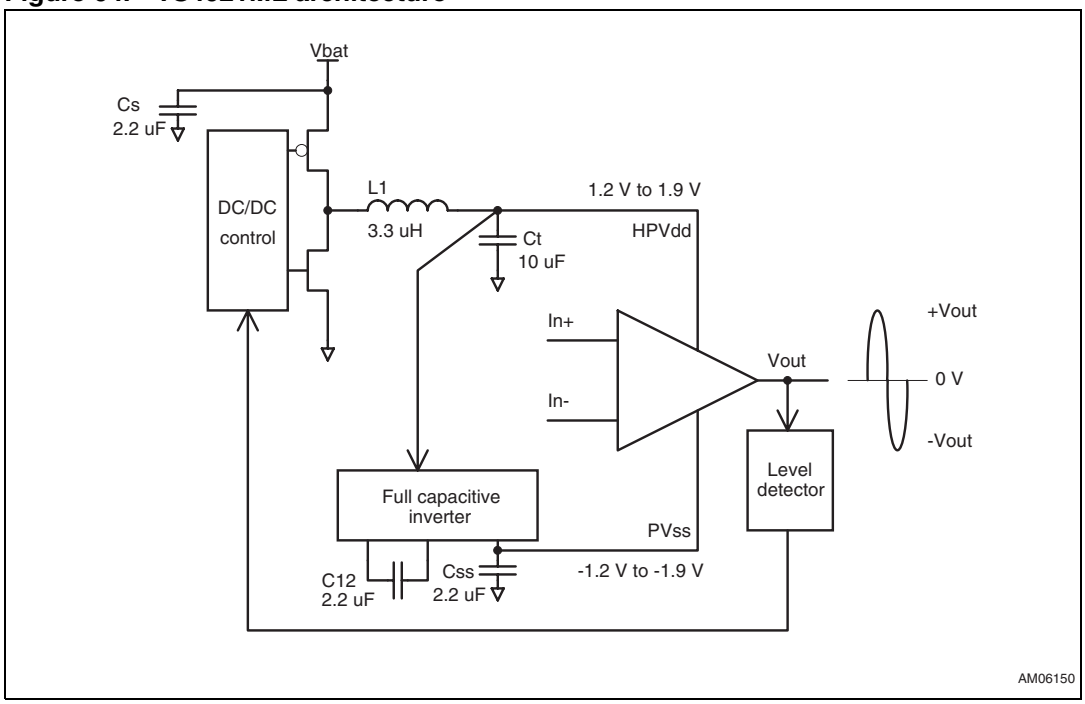
Note: See Table 5: Electrical characteristics of the amplifier for V_{IH} and V_{IL} levels.

4.2 Overview of the class-G, 2-level headphone amplifier

The TS4621ML uses what is referred to as *class-G operating mode*. This mode is a combination of the class AB biasing technique and an adaptive power supply. For this device, the power supply uses two levels: ±1.2 V and ±1.9 V.

To create the ±1.2 V and ±1.9 V levels, the device uses an internal high-efficiency step-down converter linked with a fully capacitive inverter from AVdd. Thanks to these internally-generated symmetrical power supply voltages, the output of the amplifier can be biased at 0 V, thus eliminating the classical bulky DC blocking output capacitors (typically more than 100 µF).

Figure 64. TS4621ML architecture



When an audio signal is playing with the TS4621ML, the class G feature adjusts in real time the internal power supply voltage in order to achieve the best efficiency possible. In addition, thanks to the fast transient response of the internal DC/DC converters, the switching between ±1.2 V and ±1.9 V can be achieved without audio clipping. Moreover, the out-of-