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TS4956

Stereo audio amplifier system with I²C bus interface

Features

- Operating from V_{CC} = 2.7 V to 5.5 V
- I²C bus control interface
- 38 mW output power at V_{CC} = 3.3 V, THD = 1%, F = 1 kHz, with 16 Ω load
- Ultra low consumption in standby mode: 0.5 µA
- Digital volume control range from +12 dB to -34 dB
- 32-step digital volume control
- Stereo loudspeaker option by I²C
- 8 different output mode selections
- Pop and click reduction circuitry
- Flip-chip package, 18 bumps with 300 µm diameter
- Lead-free flip chip package
- Output power limitation on headphone for eardrum damage consideration

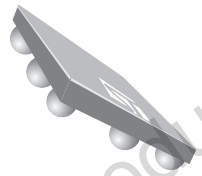
Applications

- Mobile phones (cellular/cordless)
- PDAs
- Laptop / notebook computers
- Portable audio devices

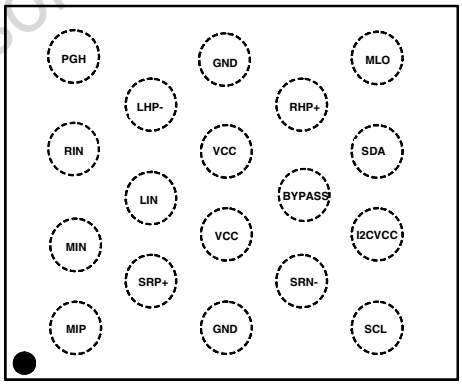
Description

The TS4956 is a complete audio system device with three dedicated outputs, one stereo headphone, one loudspeaker drive and one mono line for a hands-free set. The stereo headphone is capable of delivering more than 25 mW per channel of continuous average power into 16 Ω single-ended loads with 0.3% THD+N from a 5 V power supply. The device functions are controlled via an I²C bus, which minimizes the number of external components needed.

TS4956 - flip-chip 18



Pin connections (top view)



The overall gain and the different output modes of the TS4956 are controlled digitally by the control registers which are programmed via the I²C interface. It has also an internal thermal shutdown protection mechanism.

Contents

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_i	Input voltage (2)	G_{ND} to V_{CC}	V
T_{oper}	Operating free air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient (3)	200	°C/W
P_{diss}	Power dissipation	Internally limited(4)	
ESD	Susceptibility - human body model(5)	2	kV
	Susceptibility - machine model	150	V
Latch-up	Latch-up immunity	200	mA
	Lead temperature (soldering, 10sec)	260	°C

1. All voltage values are measured with respect to the ground pin.
2. The magnitude of input signal must never exceed V_{CC} + 0.3 V / GND - 0.3 V
3. Device is protected in case of over temperature by a thermal shutdown activated at 150°C.
4. Exceeding the power derating curves during a long period may involve abnormal operating conditions.
5. Human body model, 100 pF discharged through a 1.5 kΩ resistor, into pin to V_{CC} device

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}(1)	Supply voltage	2.7 to 5.5 V	V
R_L	Load resistor Speaker/BTL output (modes 1,2,7) Headphone, MLO output (modes 3,4,5,6,)	 ≥8 ≥16	Ω
C_L	Load capacitor R_L = 8 Ω to 100 Ω (speaker/BTL output - modes 1,2,7) R_L = 16 Ω to 100 Ω (headphone, MLO output - modes 3,4,5,6) R_L > 100 Ω	 500 400 100	pF
R_{thja}	Flip-chip thermal resistance junction to ambient	90(2)	°C/W

1. For proper functionality of I2C bus, V_{CC} pins must not be grounded. ESD protection diodes ground data and clock wires and cause dysfunction of I^2C bus in this condition.
2. With heat sink surface 120 mm^2.

Table 3. I^2C electrical characteristics

Symbol	Parameter	Value	Unit
I^2CV_{CC}	I2C supply voltage(1)	2.7 to 5.5 V	V
V_{ILI}	Maximum low level input voltage on pins SDA, SCL	0.3 I2CVCC	V
V_{IH}	Minimum high level input voltage	0.7 I2CVCC	V
I_{IN}	Maximum input current (pins SDA, SCL), 0.4 V < V_{in} < 4.5 V	10	µA
F_{SCL}	SCL maximum clock frequency	400	kHz
V_{ol}	Max low level output voltage, SDA pin, I_{sink} = 3 mA	0.4	V

1. Must be less than or equal to the power supply voltage V_{CC} of the device.

2 Typical application schematic

Table 4. Description of external components

Components	Functional description
C_{s1}, C_{s2}	Supply bypass capacitors which provide power supply filtering.
C_b	Bypass capacitor which provides half-supply filtering.
C_{in1} to C_{in4}	Input capacitors which form together with input impedance Z_{in} first-order high pass filter to block DC voltage on inputs
C_{out}	Output capacitor which forms with output load R_L first-order high pass filter to block half-supply voltage on single-ended output.
R_1	Resistor to keep C_{out} charged for better pop performance on single-ended output.

Figure 1. Typical application for the TS4956 (modes 1, 2, 3, 4, 5 and 6)

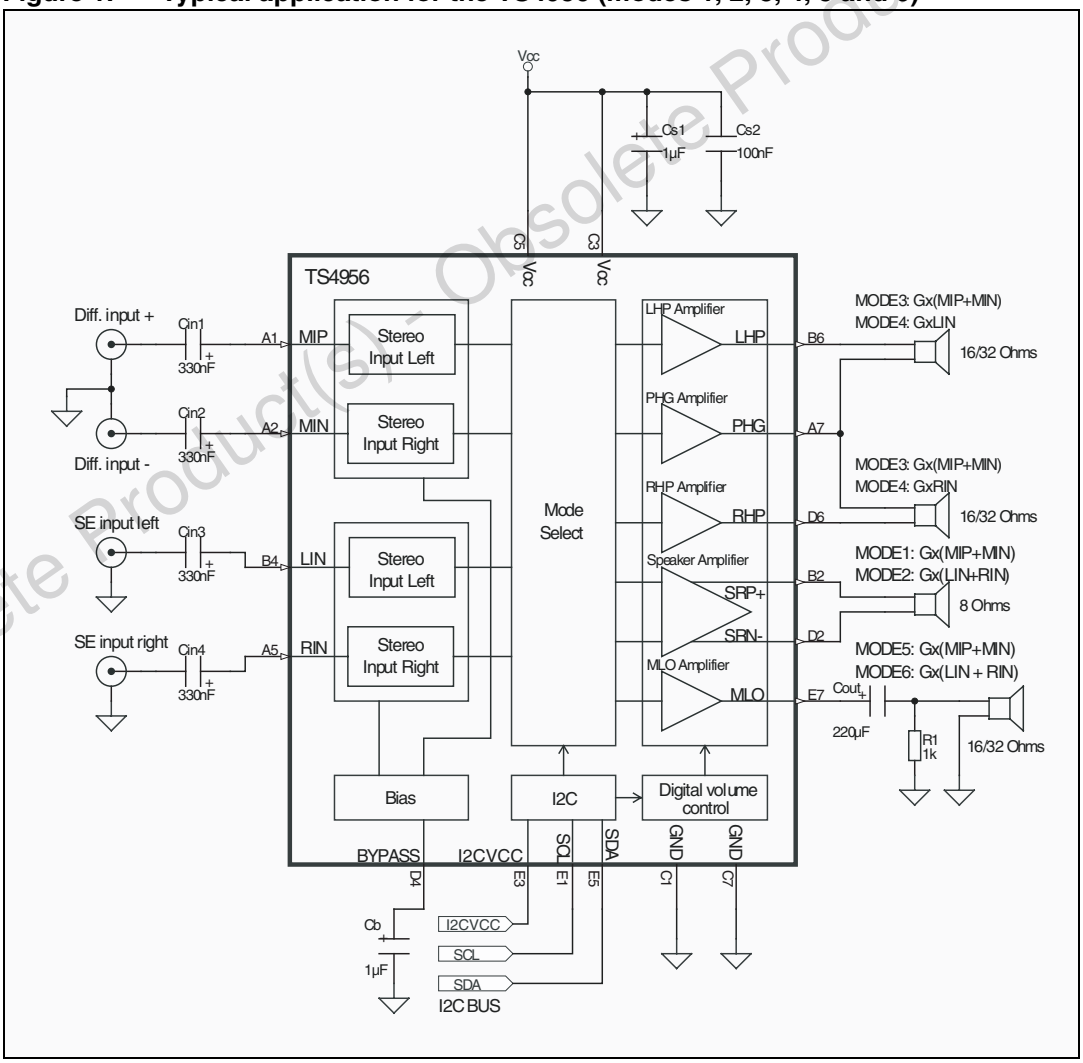
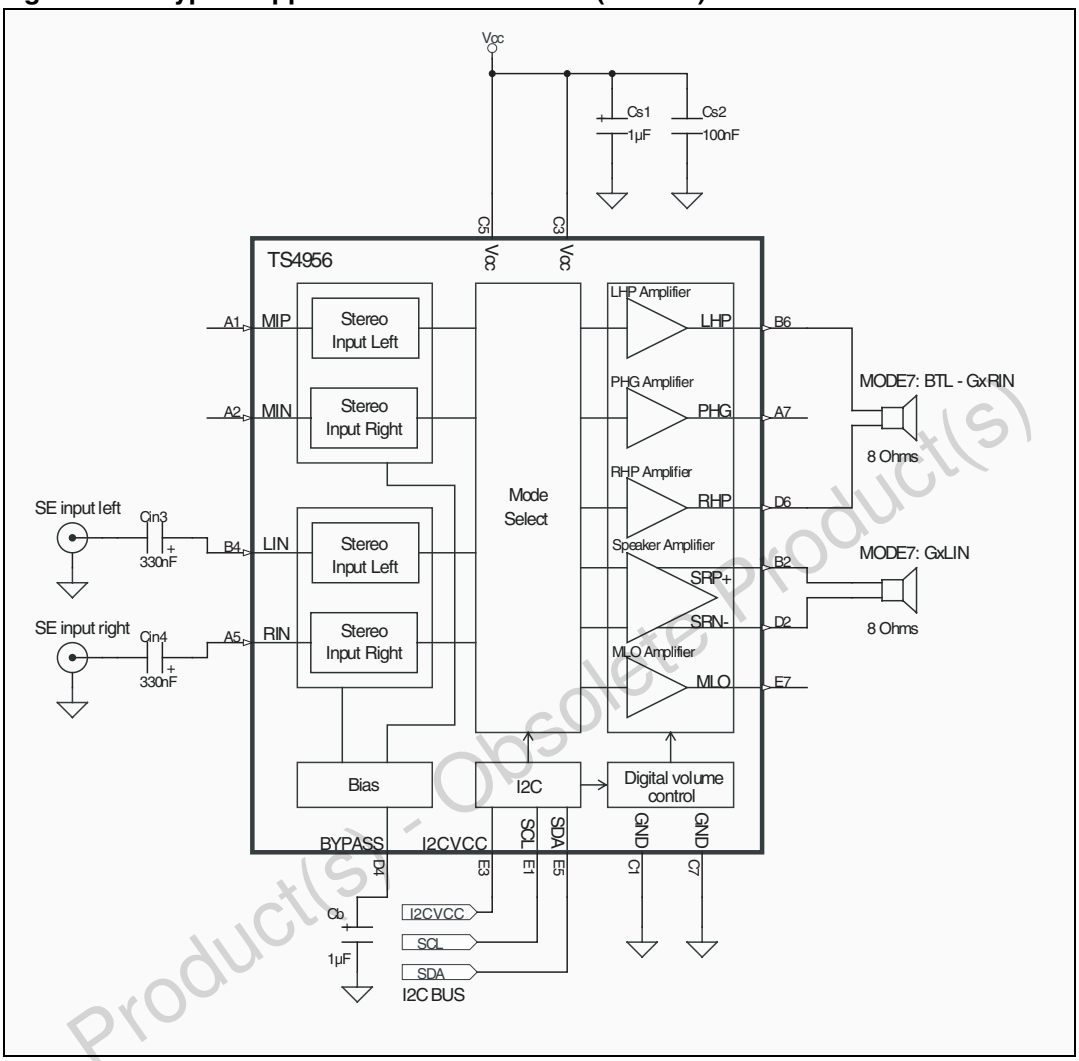


Figure 2. Typical application for the TS4956 (mode 7)



2.1 I²C interface

The TS4956 uses a serial bus, which conforms to the I²C protocol (the TS4956 must be powered when it is connected to the I²C bus), to control the chip's functions via two wires: clock and data.

The clock and data lines are bidirectional (open-collector) with an external chip pull-up resistor (typically 10 kΩ). The maximum clock frequency in fast-mode specified by the I²C standard is 400 kHz, and this frequency is supported by the TS4956. In this application, the TS4956 is always the slave device and the controlling MCU is the master device.

The I2CVCC pin determines the power supply of the TS4956's I²C interface. The voltage connected to this pin must be equal to or less than the TS4956 power supply voltage V_{CC}. The minimum value of the I2CVCC voltage is 2.7 V.

When the I2CVCC pin is connected to an I²C voltage, the TS4956 is ready to communicate via the I²C bus.

When the I2CVCC pin is connected to the ground, the TS4956 is in total standby mode, with an ultra-low standby current on the order of a few nanoamperes. In this condition the TS4956 cannot receive I²C commands from the I²C bus.

In both cases, pins SDA and SCL must respect logic HI or logic LOW thresholds (not floating) presented in *Table 3 on page 4*, in order for the circuit to function properly.

Table 5 summarizes the pin descriptions for the I²C bus interface.

Table 5. I²C bus interface: pin descriptions

Pin	Functional description
SDA	Serial data pin
SCL	Clock input pin
I2CVCC	I²C interface power supply

2.1.1 I²C operation description

The host MCU can write into the TS4946 control register to control the TS4956 and read from the control register to get the current configuration of the TS4956. The TS4956 is addressed by a single byte consisting of a 7-bit slave address and an R/W bit. The TS4956 control register address is $5Dh.

Table 6. First byte after the START message for addressing the device

A6	A5	A4	A3	A2	A1	A0	Rw
1	0	1	1	1	0	1	X

In order to write data into the TS4956 control register, after the "start" message the MCU must send the following data:

- send byte with the I²C 7-bit slave address and with the R/W bit set low.
- send the data (control register setting).

All bytes are sent with the MSB bit first. The transfer of written data ends with a "stop" message. When transmitting several bits of data, the data can be written without having to repeat the "start" message or address byte with the slave address.

In order to read data from the TS4956, after the "start" message, the MCU must send and receive the following data:

- send byte with the I²C 7-bit slave address and with the R/W bit set high.
- receive the data (control register value).

All bytes are read with the MSB bit first. The transfer of read data is ended with a "stop" message. When transmitting several bits of data, the data can be read with having to repeat the "start" message and the byte with slave address. In this case the value of the control register is read repeatedly.

Figure 3. I²C read/write operation

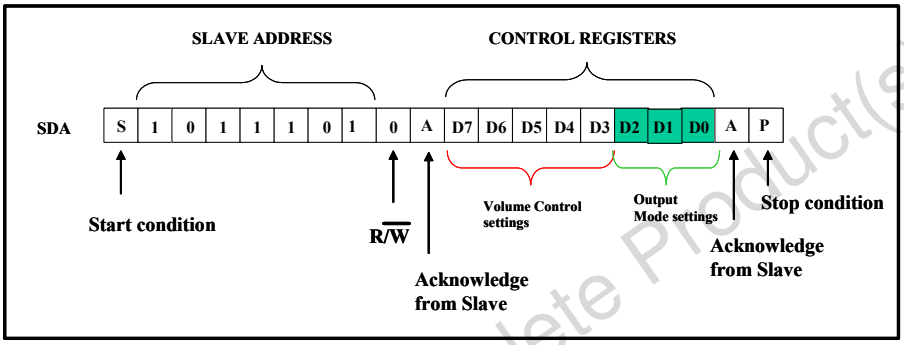


Table 7. Output mode selection: G from -34.5 dB to + 12 dB (by steps of 1.5 dB)(1)

Output mode #	RHP	LHP	Speaker P/N	Mono L/O
0	SD	SD	SD	SD
1	SD	SD	Gx (MIP + MIN)	SD
2	SD	SD	GX (RIN + LIN)	SD
3	GX (MIP + MIN)	GX (MIP + MIN)	SD	SD
4	G x RIN	G x LIN	SD	SD
5	SD	SD	SD	GX (MIP + MIN)
6	SD	SD	SD	GX (RIN + LIN)
7	BTL: G x RIN	BTL: G x RIN	G x LIN	SD

1. SD = shutdown mode
G = audio gain
MIP = mono input positive
MIN = mono input negative
RIN = stereo input right
LIN = stereo input left

2.1.2 Gain and mode setting operations

The gain of the TS4956 ranges from -34.5 dB to +12 dB. At power-up, the output channels are set to standby mode.

Table 8. Gain settings truth table

G: Gain (dB) #	D7 (MSB)	D6	D5	D4	D3
-34.5	0	0	0	0	0
-33	0	0	0	0	1
-31.5	0	0	0	1	0
-30	0	0	0	1	1
-28.5	0	0	1	0	0
-27	0	0	1	0	1
-25.5	0	0	1	1	0
-24	0	0	1	1	1
-22.5	0	1	0	0	0
-21	0	1	0	0	1
-19.5	0	1	0	1	0
-18	0	1	0	1	1
-16.5	0	1	1	0	0
-15	0	1	1	0	1
-13.5	0	1	1	1	0
-12	0	1	1	1	1
-10.5	1	0	0	0	0
-9	1	0	0	0	1
-7.5	1	0	0	1	0
-6	1	0	0	1	1
-4.5	1	0	1	0	0
-3	1	0	1	0	1
-1.5	1	0	1	1	0
0	1	0	1	1	1
+1.5	1	1	0	0	0
+3	1	1	0	0	1
+4.5	1	1	0	1	0
+6	1	1	0	1	1
+7.5	1	1	1	0	0
+9	1	1	1	0	1
+10.5	1	1	1	1	0
+12	1	1	1	1	1

Table 9. Output mode settings truth table

D2	D1	D0	Comments
0	0	0	OUTPUT MODE 0
0	0	1	OUTPUT MODE 1
0	1	0	OUTPUT MODE 2
0	1	1	OUTPUT MODE3
1	0	0	OUTPUT MODE 4
1	0	1	OUTPUT MODE 5
1	1	0	OUTPUT MODE 6
1	1	1	OUTPUT MODE 7

2.1.3 Acknowledge bit

The number of data bytes transferred between the start and the stop conditions from the CPU master to the TS4956 slave is unlimited. Each byte of eight bits is followed by one acknowledge bit.

The addressed TS4956 generates an acknowledge after receiving each byte that has been clocked out.

3 Electrical characteristics

Table 10. V_{CC} = +2.7 V, GND = 0 V, T_{amb} = 25° C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	Mode 1, 2, no input signal, no load		3.4	4.4	mA
		Mode 3, no input signal, no load		4.6	6	
		Mode 4, no input signal, no load		4.4	5.7	
		Mode 5, 6, no input signal, no load		1.75	2.3	
		Mode 7, no input signal, no load		5.7	7.4	
I_{STBY}	Standby current	No input signal		0.5	2	µA
V_{OO}	Output offset voltage	No input signal Modes 1, 2 speaker output, RL = 8 Ω Mode 3 headphone outputs, RL = 16 Ω Mode 4 headphone outputs, RL = 16 Ω Mode 7 BTL, speaker output, R_L = 8 Ω		 5 5 5 5	 50 50 20 20	mV
P_{out}	Headphone output power (phantom ground mode)	Modes 3, 4 THD+N = 1% max, F = 1 kHz, R_L = 16 Ω THD+N = 1% max, F = 1 kHz, R_L = 32 Ω	 30 20	 35 25		mW
	BTL, speaker output power	Modes 1, 2, 7 THD+N = 1% max, F = 1 kHz, R_L = 8 Ω	 270	 285		
	MLO output power	Modes 5, 6 THD+N = 1% max, F = 1 kHz, R_L = 16 Ω THD+N = 1% max, F = 1 kHz, R_L = 32 Ω	 35 20	 42 25		
THD+N	Total harmonic distortion + noise	G = +1.5 dB, 20 Hz < F < 20 kHz Modes 1, 2, 7, RL = 8 Ω, Pout = 200 mW Modes 3, 4, RL = 16 Ω, Pout = 15 mW Modes 5, 6, R_L = 16 Ω, P_{out} = 30 mW		 0.5 0.5 0.5		%
PSRR	Power supply rejection ratio(1)	F = 217Hz, G = +1.5 dB, V_{ripple} = 200 mVpp, Inputs grounded, C_b = 1 µF Mode 1, speaker output, RL = 8 Ω Mode 2, speaker output, RL = 8 Ω Mode 3, headphone outputs, RL = 16 Ω Mode 4, headphone outputs, RL = 16 Ω Mode 5, MLO output, RL = 16 Ω Mode 6, MLO output, RL = 16 Ω Mode 7, BTL, speaker outputs, RL = 8 Ω		 60 55 61 75 62 57 73		dB

Table 10. V_{CC} = +2.7 V, GND = 0 V, T_{amb} = 25° C (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crosstalk	Channel separation	Mode 4 F = 1 kHz, R_L = 16 Ω, P_{out} = 15 mW F = 20 Hz to 20 kHz, R_L = 16 Ω, P_{out} = 15 mW Mode 7 F = 1 kHz, R_L = 8 Ω, P_{out} = 200 mW F = 20 Hz to 20 kHz, R_L = 8 Ω, P_{out} = 200 mW		 50 50 80 60		dB
SNR	Signal-to-noise ratio	A-weighted, G = +1.5 dB, THD+N < 0.5%, 20 Hz < F < 20 kHz Mode 1 - speaker output, RL = 8 Ω Mode 2 - speaker output, RL = 8 Ω Mode 3 - headphone output, RL = 16 Ω Mode 4 - headphone output, RL = 16 Ω Mode 5 - MLO output, RL = 16 Ω Mode 6 - MLO output, R = 16 Ω Mode 7 - BTL, speaker output, R_L = 8 Ω, G = +10.5 dB		 91 90 84 90 85 85 92		dB
G	Digital gain range		-34.5		+12	dB
	Digital gain stepsize			1.5		dB
	Stepsize error		0.1		0.6	dB
Z_{in}	Input impedance, all gain setting	Differential input Differential input impedance (MIP to MIN) MIP input impedance referenced to ground MIN input impedance referenced to ground Stereo input RIN input impedance LIN input impedance	 48 24 36 24 24	 60 30 45 30 30	 72 36 54 36 36	kΩ
t_{WU}	Wake-up time			70	90	ms
t_{STBY}	Standby time			1		µs

1. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is an added sinus signal to V_{CC} at f = 217 Hz.

Table 11. V_{CC} = +3.3 V, GND = 0 V, T_{amb} = 25° C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	Mode 1, 2, no input signal, no load		3.6	4.7	mA
		Mode 3, no input signal, no load		4.8	6.2	
		Mode 4, no input signal, no load		4.6	6	
		Modes 5, 6, no input signal, no load		1.8	2.4	
		Mode 7, no input signal, no load		6	7.8	
I_{STBY}	Standby current	No input signal		0.5	2	µA
V_{OO}	Output offset voltage	No input signal Modes 1, 2 speaker output, RL = 8 Ω Mode 3 headphone outputs, RL = 16 Ω Mode 4 headphone outputs, RL = 16 Ω Mode 7 BTL, speaker output, R_L = 8 Ω		 5 5 5 5	 50 50 20 20	mV
P_{out}	Headphone output power (phantom ground mode)	Modes 3, 4 THD+N = 1% max, F = 1 kHz, RL = 16 Ω THD+N = 1% max, F = 1 kHz, RL = 32 Ω	 32 30	 38(1) 36(1)		mW
	BTL, speaker output power	Modes 1, 2, 7 THD+N = 1% max, F = 1 kHz, RL = 8 Ω	 430	 450		
	MLO output power	Modes 5, 6 THD+N = 1% max, F = 1 kHz, RL = 16 Ω THD+N = 1% max, F = 1 kHz, RL = 32 Ω	 58 32	 65 38		
THD+N	Total harmonic distortion + noise	G = +1.5 dB, 20 Hz < F < 20 kHz Modes 1, 2, 7, RL = 8 Ω, Pout = 300 mW Modes 3, 4, RL = 16 Ω, Pout = 15 mW Modes 5, 6, RL = 16 Ω, Pout = 50 mW		 0.5 0.5 0.5		%
PSRR	Power supply rejection ratio(2)	F = 217Hz, G = +1.5 dB, Vripple = 200 mVpp, inputs grounded, Cb = 1 µF Mode 1, speaker output, RL = 8 Ω Mode 2, speaker output, RL = 8 Ω Mode 3, headphone outputs, RL = 16 Ω Mode 4, headphone outputs, RL = 16 Ω Mode 5, MLO output, RL = 16 Ω Mode 6, MLO output, RL = 16 Ω Mode 7, BTL, speaker outputs, RL = 8 Ω		 63 57 63 77 64 58 74		dB

Table 11. V_{CC} = +3.3 V, GND = 0 V, T_{amb} = 25° C (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crosstalk	Channel separation	Mode 4 F = 1 kHz, RL = 16 Ω, Pout = 15 mW F = 20 Hz to 20 kHz, RL = 16 Ω, Pout = 15 mW Mode 7 F = 1 kHz, RL = 8 Ω, Pout = 300 mW F = 20 Hz to 20 kHz, RL = 8 Ω, Pout = 300 mW		 50 50 80 60		dB
SNR	Signal-to-noise ratio	A-weighted, G = +1.5 dB, THD+N < 0.5%, 20 Hz < F < 20 kHz Mode 1 - speaker output, RL = 8 Ω Mode 2 - speaker output, RL = 8 Ω Mode 3 - headphone output, RL = 16 Ω Mode 4 - headphone output, RL = 16 Ω Mode 5 - MLO output, RL = 16 Ω Mode 6 - MLO output, R = 16 Ω Mode 7 - BTL, speaker output, RL = 8 Ω, G = +10.5 dB		 93 92 85 91 87 87 95		dB
G	Digital gain range		-34.5		+12	dB
	Digital gain stepsize			1.5		dB
	Stepsize error		0.1		0.6	dB
Z_{in}	Input impedance, all gain setting	Differential input Differential input impedance (MIP to MIN) MIP input impedance referenced to ground MIN input impedance referenced to ground Stereo input RIN input impedance LIN input impedance	 48 24 36 24 24	 60 30 45 30 30	 72 36 54 36 36	kΩ
t_{WU}	Wake-up time			70	90	ms
t_{STBY}	Standby time			1		µs

1. Internal power limitation on headphone outputs (see application information).
2. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is an added sinus signal to V_{CC} at F = 217 Hz.

Table 12. V_{CC} = +5 V, GND = 0 V, T_{amb} = 25° C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	Mode 1, 2, no input signal, no load		4	5.2	mA
		Mode 3, no input signal, no load		5.3	6.9	
		Mode 4, no input signal, no load		5.2	6.8	
		Modes 5, 6, no input signal, no load		1.9	2.5	
		Mode 7, no input signal, no load		6.7	8.7	
I_{STBY}	Standby current	No input signal		0.5	2	µA
V_{OO}	Output offset voltage	No input signal Modes 1, 2 speaker output, RL = 8 Ω Mode 3 headphone outputs, RL = 16 Ω Mode 4 headphone outputs, RL = 16 Ω Mode 7 BTL, speaker output, RL = 8 Ω		 5 5 5 5	 50 50 20 20	mV
P_{out}	Headphone output power (phantom ground mode)	Modes 3, 4 THD+N = 1% max, F = 1 kHz, RL = 16 Ω THD+N = 1% max, F = 1 kHz, RL = 32 Ω	 32 35	 39(1) 43(1)		mW
	BTL, speaker output power	Modes 1, 2, 7 THD+N = 1% max, F = 1 kHz, RL = 8 Ω	 1000	 1055		
	MLO output power	Modes 5, 6 THD+N = 1% max, F = 1 kHz, RL = 16 Ω THD+N = 1% max, F = 1 kHz, RL = 32 Ω	 140 80	 150 88		
THD+N	Total harmonic distortion + noise	G = +1.5 dB, 20 Hz < F < 20 kHz Modes 1, 2, 7, RL = 8 Ω, Pout = 700 mW Modes 3, 4, RL = 16 Ω, Pout = 15 mW Modes 5, 6, RL = 16 Ω, Pout = 100 mW		 0.5 0.5 0.5		%
PSRR	Power supply rejection ratio(2)	F = 217Hz, G = +1.5 dB, Vripple = 200 mVpp, inputs grounded, Cb = 1 µF Mode 1, speaker output, RL = 8 Ω Mode 2, speaker output, RL = 8 Ω Mode 3, headphone outputs, RL = 16 Ω Mode 4, headphone outputs, RL = 16 Ω Mode 5, MLO output, RL = 16 Ω Mode 6, MLO output, RL = 16 Ω Mode 7, BTL, speaker outputs, RL = 8 Ω		 66 60 65 78 66 61 75		dB

Table 12. V_{CC} = +5 V, GND = 0 V, T_{amb} = 25° C (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crosstalk	Channel separation	Mode 4 F = 1 kHz, RL = 16 Ω, Pout = 15 mW F = 20 Hz to 20 kHz, RL = 16 Ω, Pout = 15 mW Mode 7 F = 1 kHz, RL = 8 Ω, Pout = 700 mW F = 20 Hz to 20 kHz, RL = 8 Ω, Pout = 700 mW		50 50 80 60		dB
SNR	Signal-to-noise ratio	A-weighted, G = +1.5 dB, THD+N < 0.5%, 20 Hz < F < 20 kHz Mode 1 - speaker output, RL = 8 Ω Mode 2 - speaker output, RL = 8 Ω Mode 3 - headphone output, RL = 16 Ω Mode 4 - headphone output, RL = 16 Ω Mode 5 - MLO output, RL = 16 Ω Mode 6 - MLO output, R = 16 Ω Mode 7 - BTL, Speaker output, RL = 8 Ω, G = +10.5 dB		96 96 85 91 90 90 98		dB
G	Digital gain range		-34.5		+12	dB
	Digital gain stepsize			1.5		dB
	Stepsize error		0.1		0.6	dB
Z_{in}	Input impedance, all gain setting	Differential input Differential input impedance (MIP to MIN) MIP input impedance referenced to ground MIN input impedance referenced to ground Stereo input RIN input impedance LIN input impedance	 48 24 36 24 24	 60 30 45 30 30	 72 36 54 36 36	kΩ
t_{WU}	Wake-up time			70	90	ms
t_{STBY}	Standby time			1		µs

1. Internal power limitation on headphone outputs (see application information).
2. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is an added sinus signal to V_{CC} at F = 217 Hz.

Table 13. Output noise V_{CC} = 2.7 V to 5.5 V (all inputs grounded)

	G = +12 dB		G = +10.5 dB		G = +1.5 dB	
	A-weighted filter	Unweighted filter (20Hz - 20kHz)	A-weighted filter	Unweighted filter (20Hz - 20kHz)	A-weighted filter	Unweighted filter (20Hz - 20kHz)
	V_{out} (µV)	V_{out} (µV)	V_{out} (µV)	V_{out} (µV)	V_{out} (µV)	V_{out} (µV)
Mode 1 - SPK out	54	80	67	100	45	66
Mode 2 - SPK out	67	99	75	111	45	69
Mode 3 - LHP, RHP	55	80	68	100	45	67
Mode 4 - LHP, RHP	29	43	35	52	23	34
Mode 5 - MLO	53	80	66	97	45	66
Mode 6 - MLO	65	96	73	106	45	67
Mode 7 - BTL, SPK out	29	42	35	52	23	34

Figure 4. THD+N vs. output power

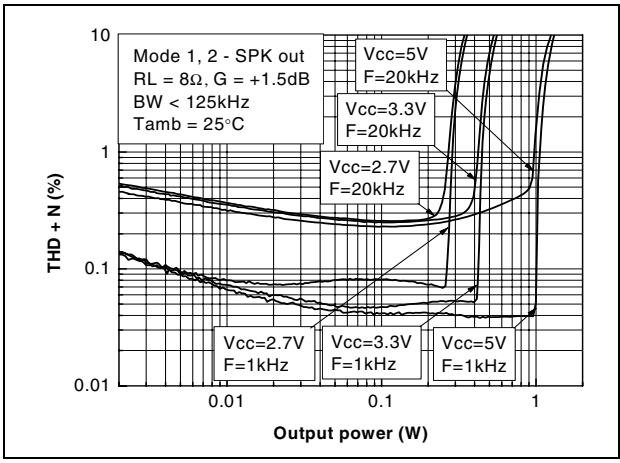


Figure 5. THD+N vs. output power

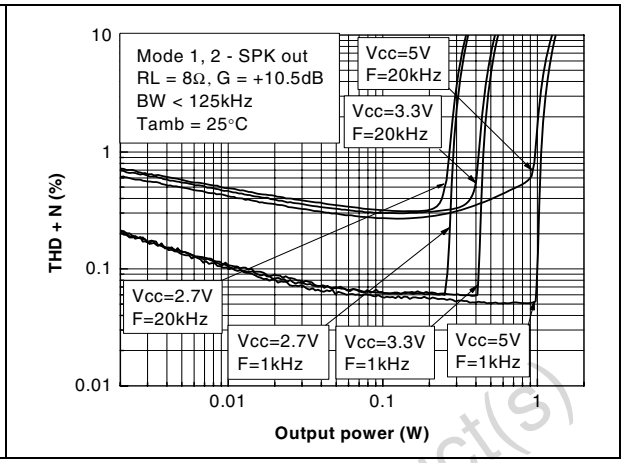


Figure 6. THD+N vs. output power

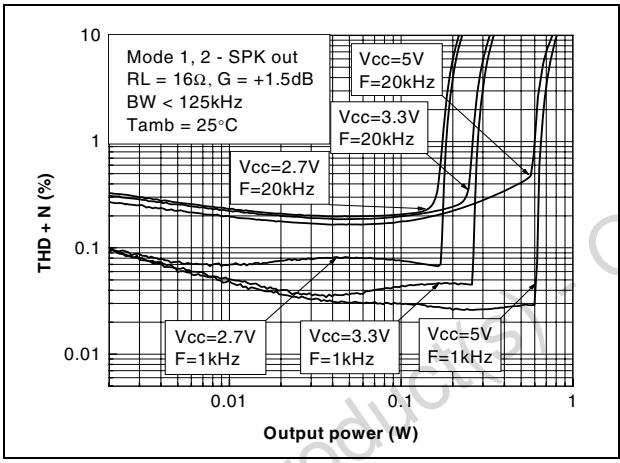


Figure 7. THD+N vs. output power

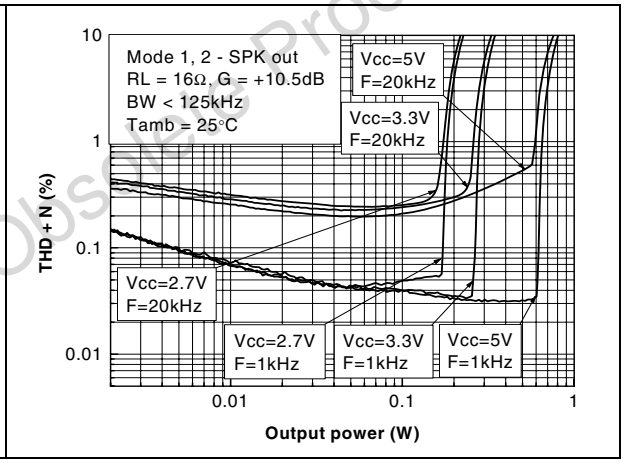


Figure 8. THD+N vs. output power

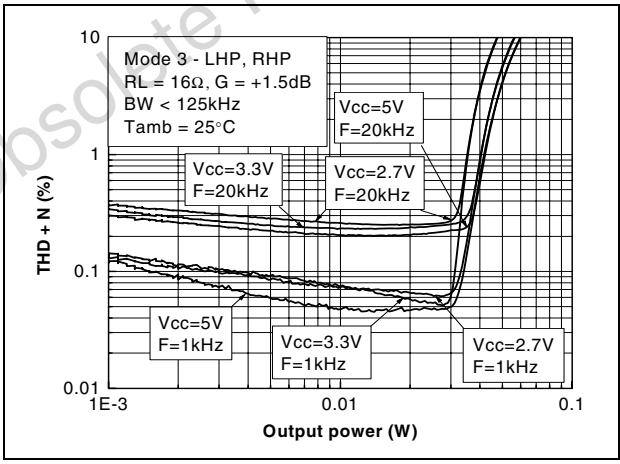


Figure 9. THD+N vs. output power

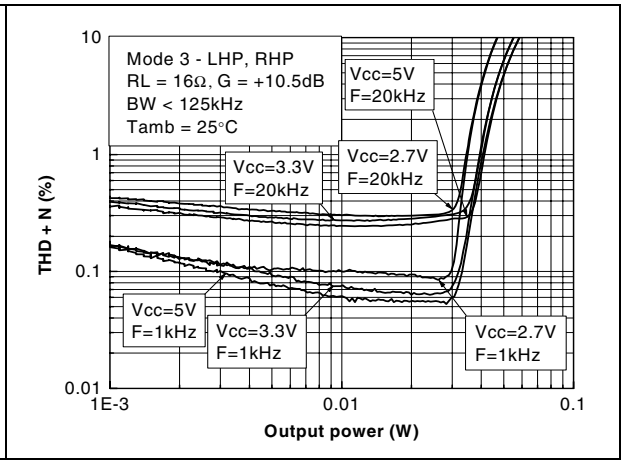


Figure 10. THD+N vs. output power

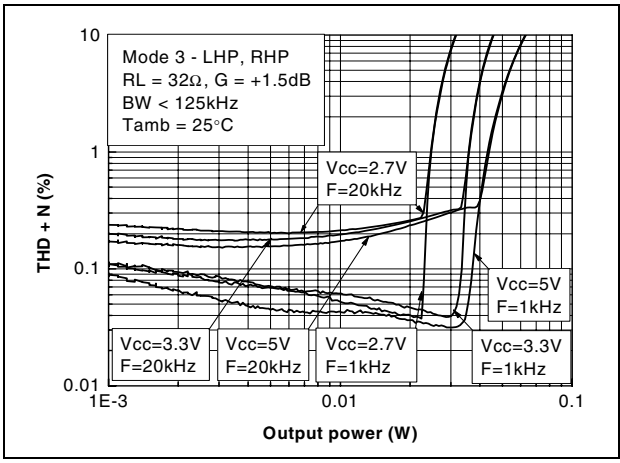


Figure 11. THD+N vs. output power

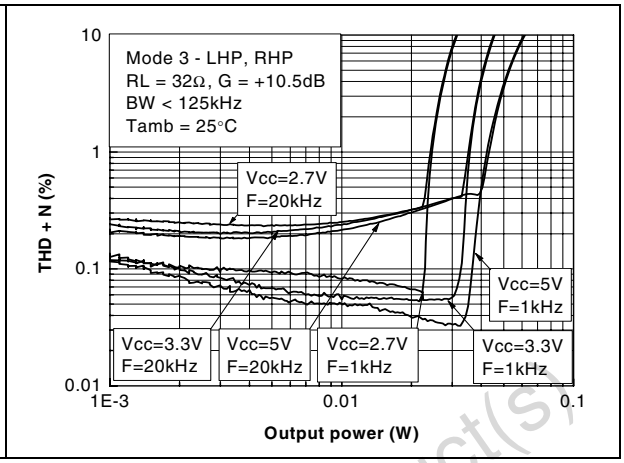


Figure 12. THD+N vs. output power

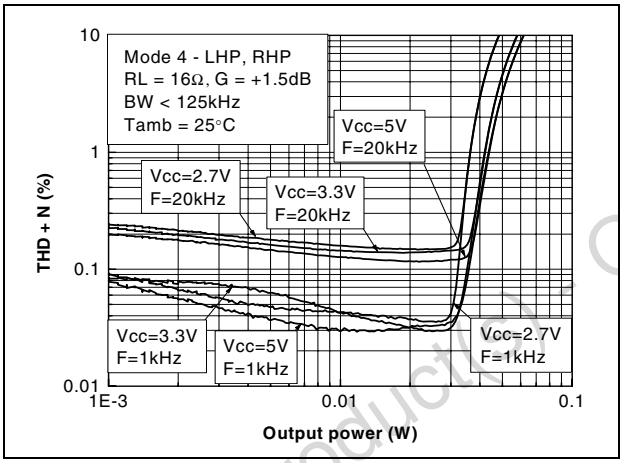


Figure 13. THD+N vs. output power

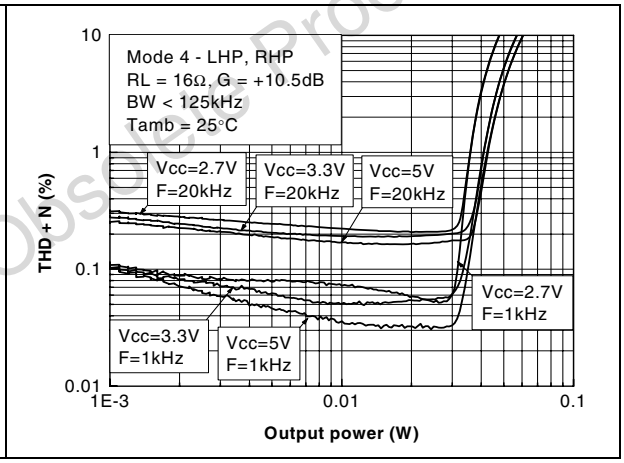


Figure 14. THD+N vs. output power

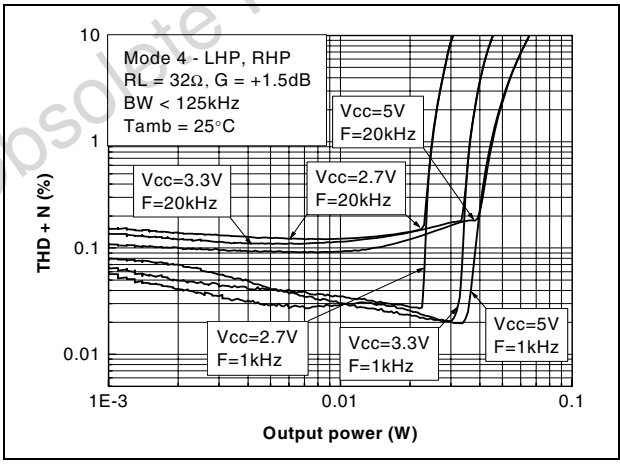


Figure 15. THD+N vs. output power

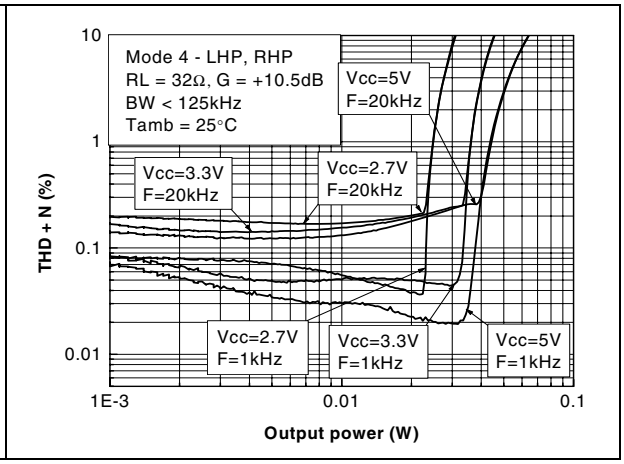


Figure 16. THD+N vs. output power

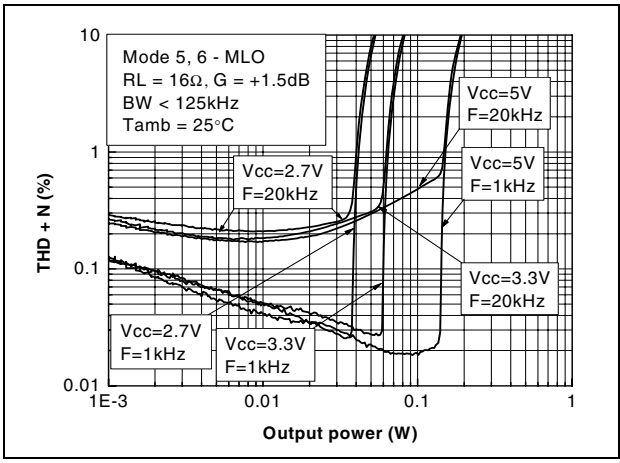


Figure 17. THD+N vs. output power

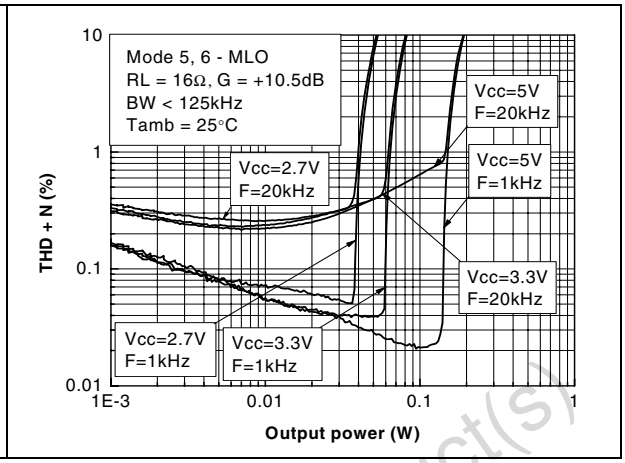


Figure 18. THD+N vs. output power

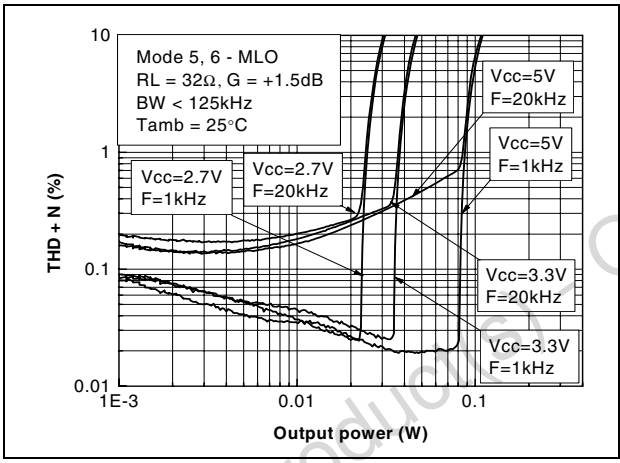


Figure 19. THD+N vs. output power

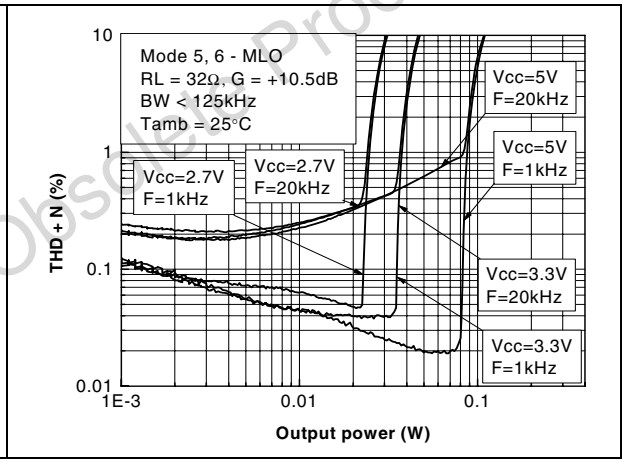


Figure 20. THD+N vs. output power

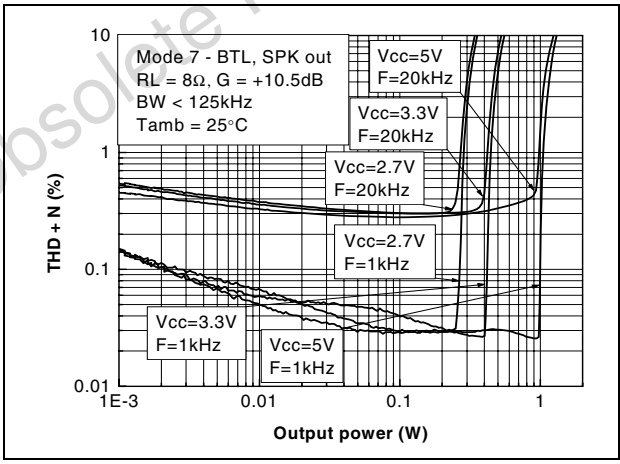


Figure 21. THD+N vs. output power

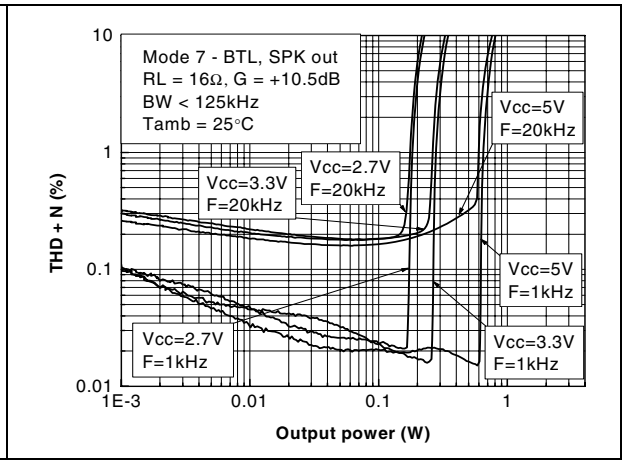


Figure 22. THD+N vs. frequency

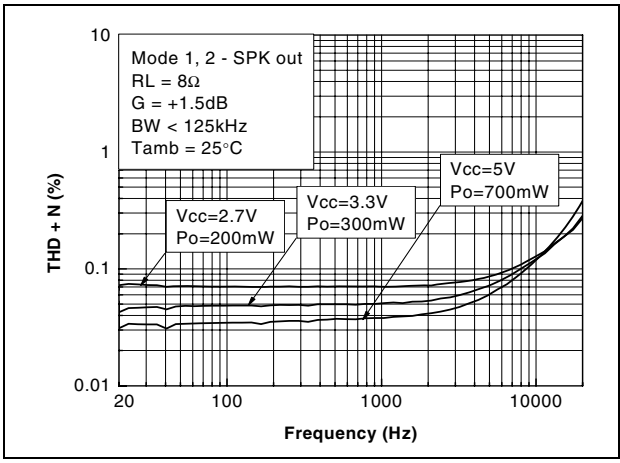


Figure 23. THD+N vs. frequency

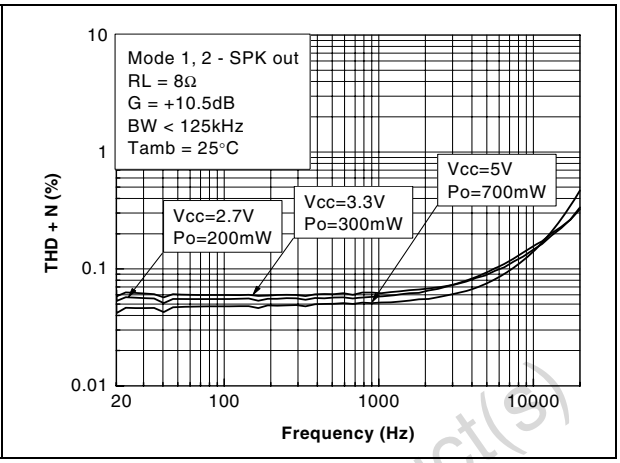


Figure 24. THD+N vs. frequency

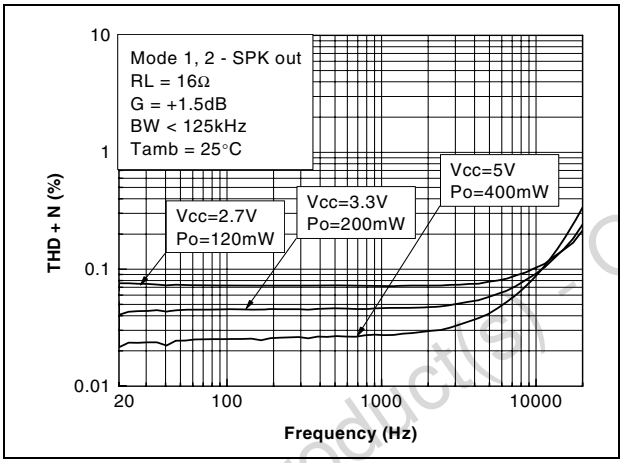


Figure 25. THD+N vs. frequency

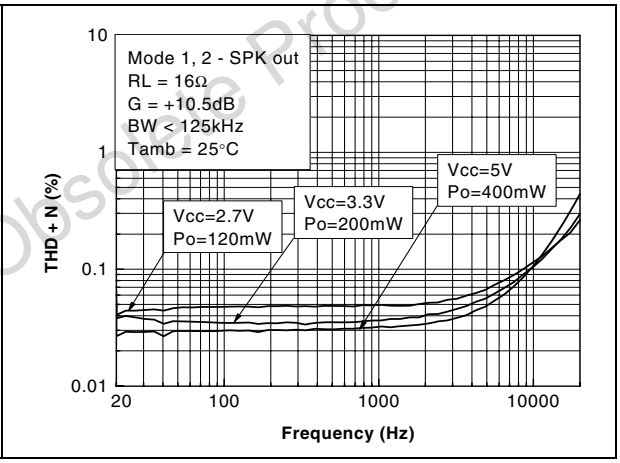


Figure 26. THD+N vs. frequency

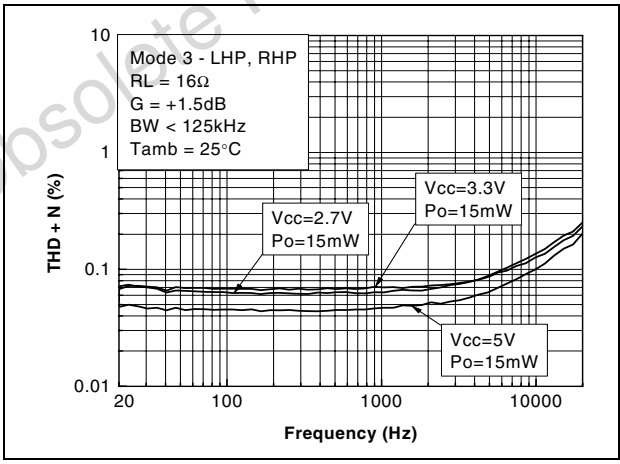


Figure 27. THD+N vs. frequency

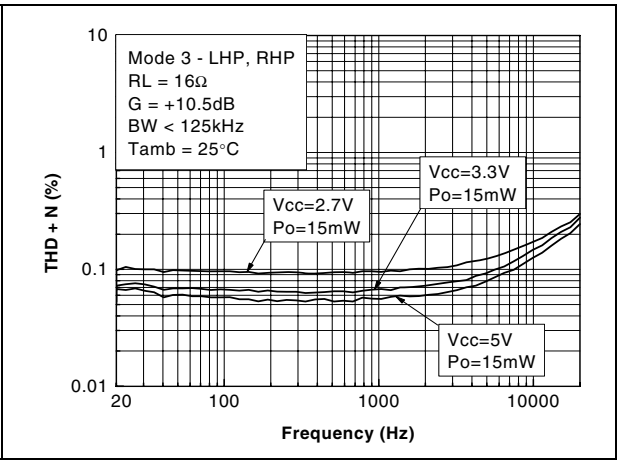


Figure 28. THD+N vs. frequency

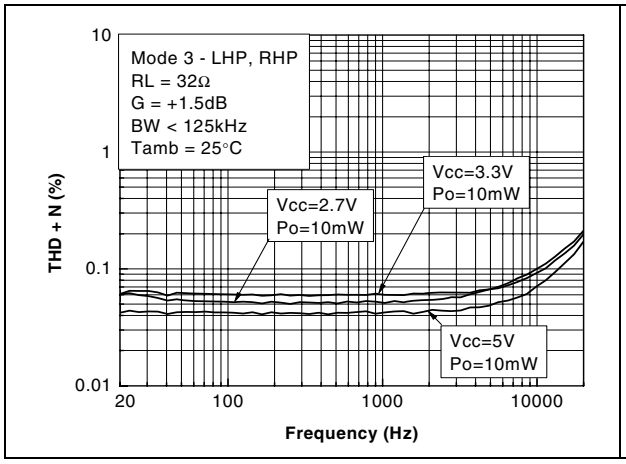


Figure 29. THD+N vs. frequency

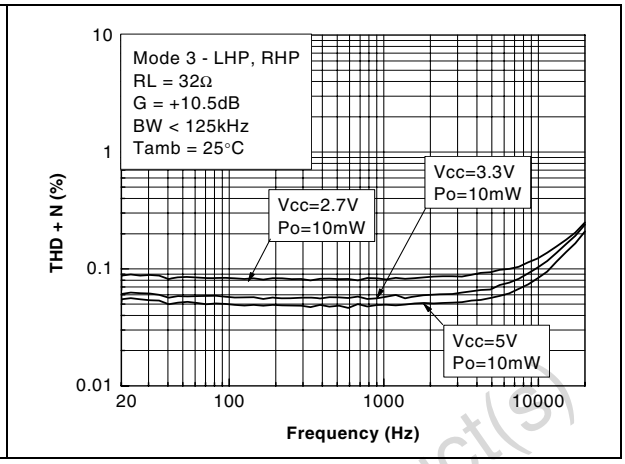


Figure 30. THD+N vs. frequency

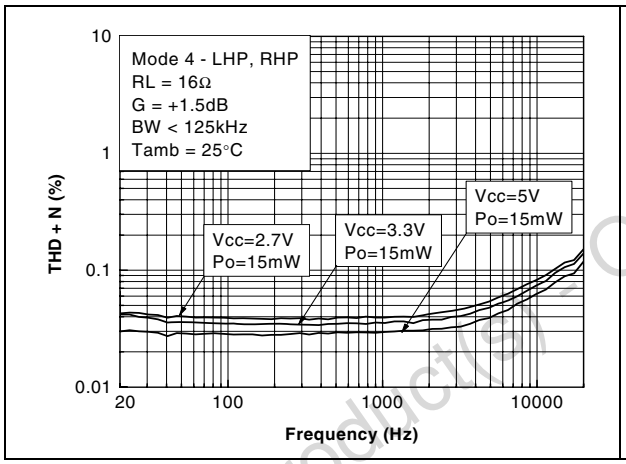


Figure 31. THD+N vs. frequency

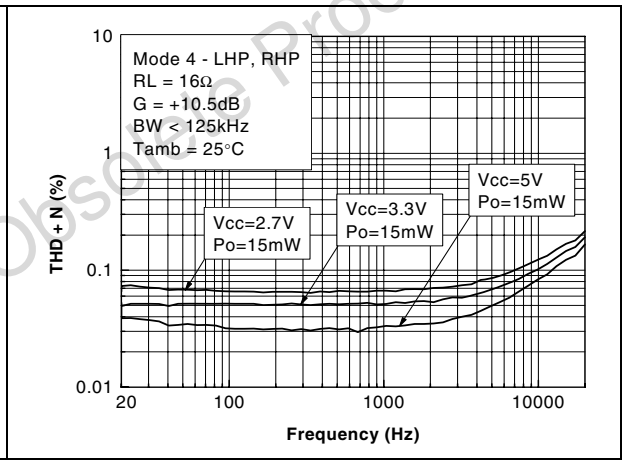


Figure 32. THD+N vs. frequency

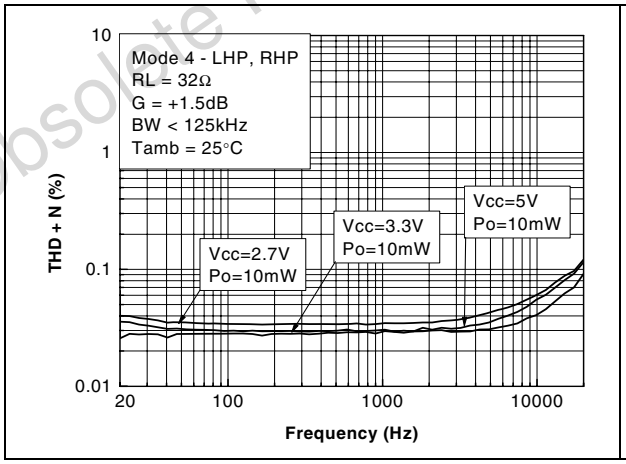


Figure 33. THD+N vs. frequency

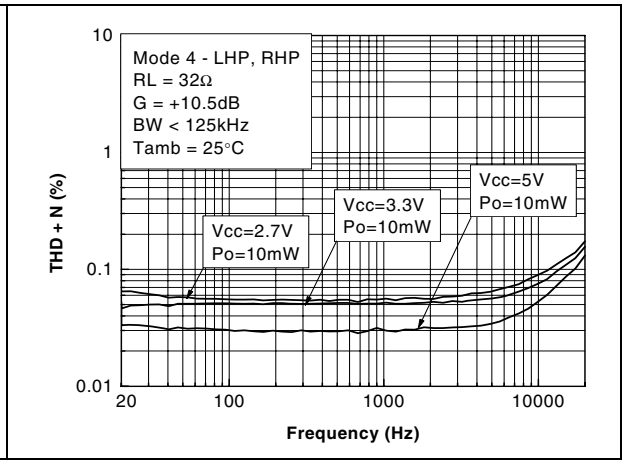


Figure 34. THD+N vs. frequency

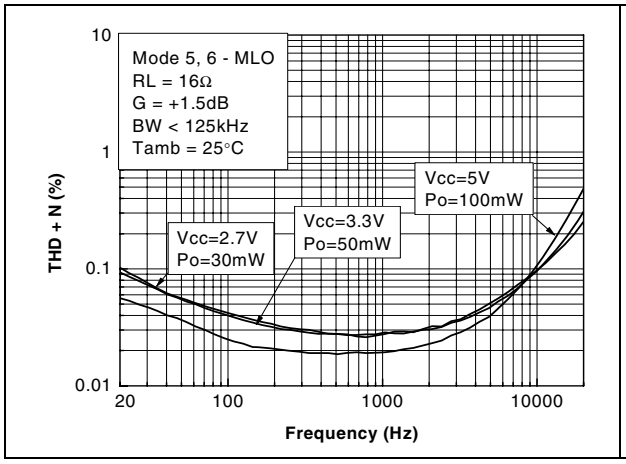


Figure 35. THD+N vs. frequency

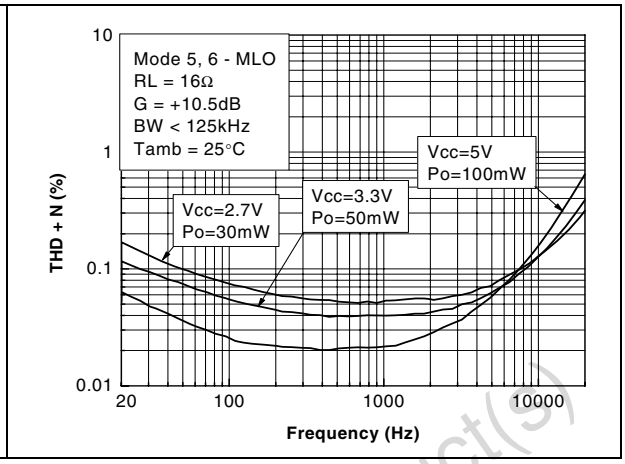


Figure 36. THD+N vs. frequency

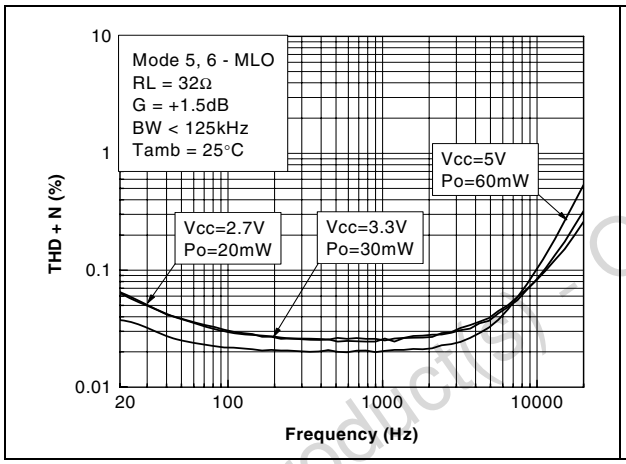


Figure 37. THD+N vs. frequency

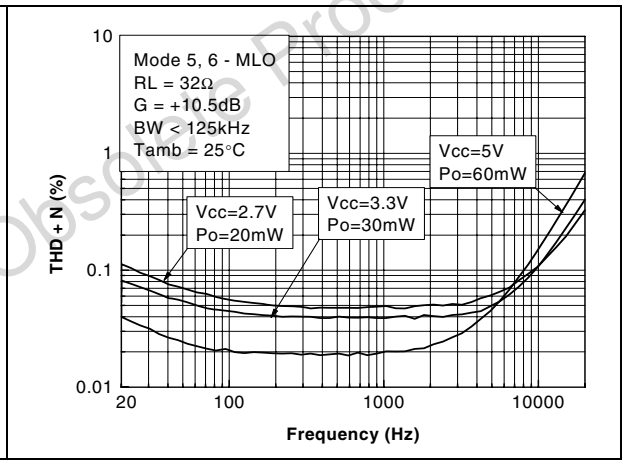


Figure 38. THD+N vs. frequency

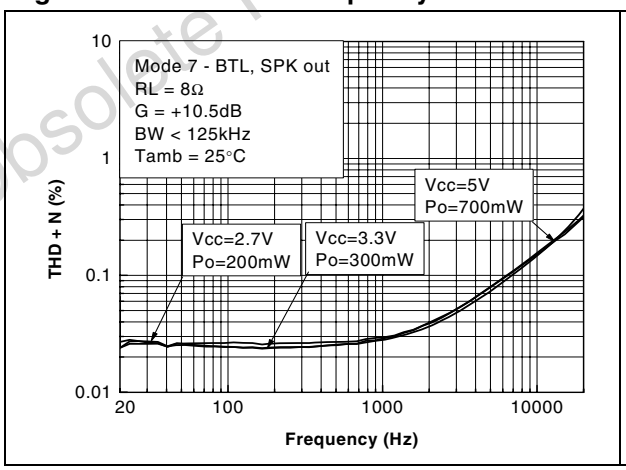


Figure 39. THD+N vs. frequency

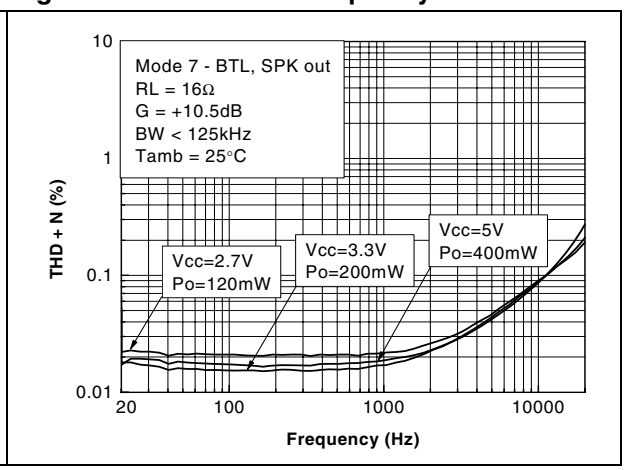


Figure 40. Output power vs. power supply voltage

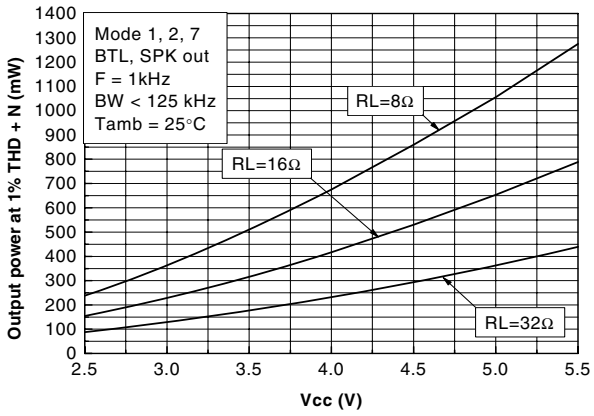


Figure 41. Output power vs. power supply voltage

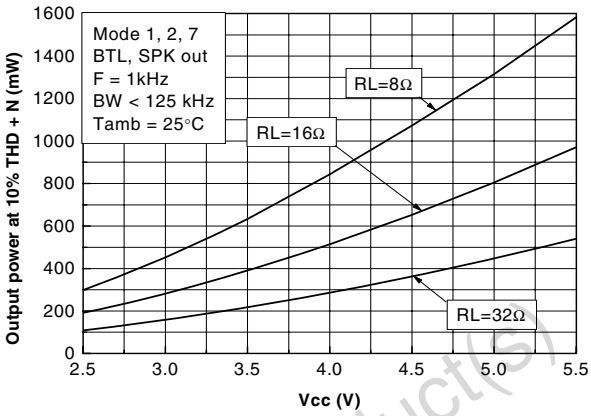


Figure 42. Output power vs. power supply voltage

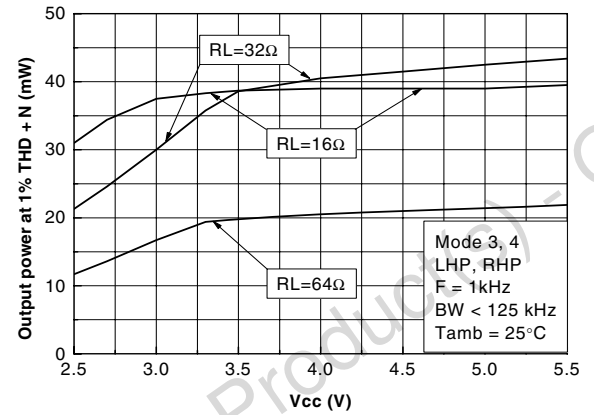


Figure 43. Output power vs. power supply voltage

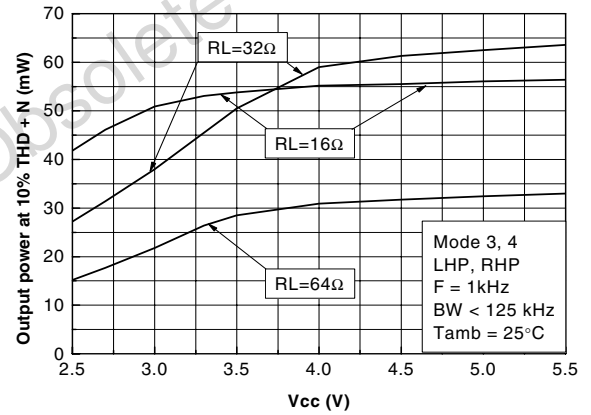


Figure 44. Output power vs. power supply voltage

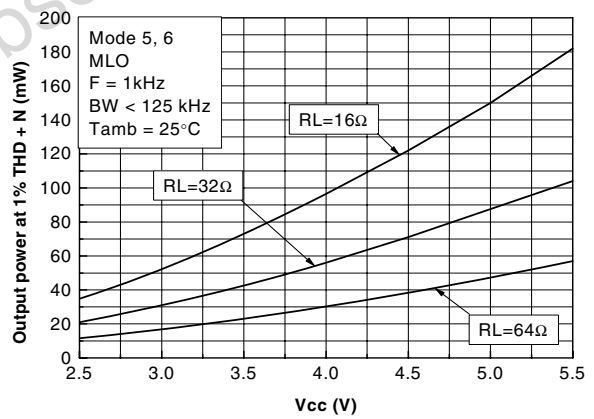


Figure 45. Output power vs. power supply voltage

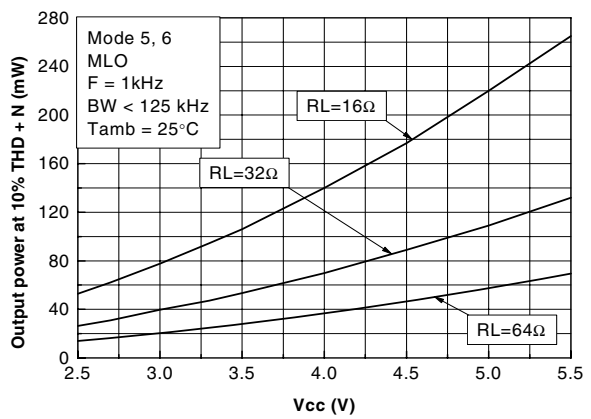


Figure 46. Output power vs. load resistance

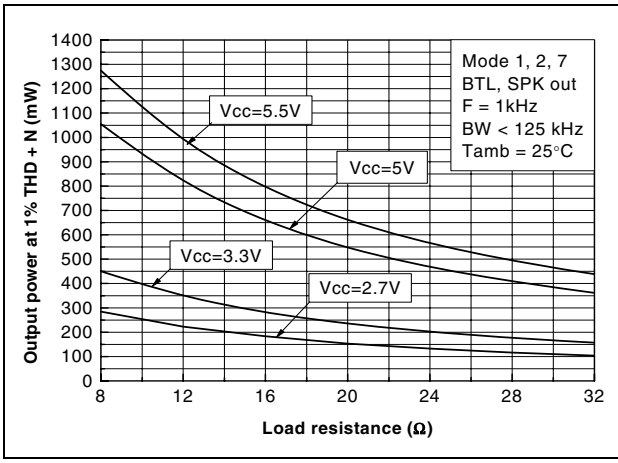


Figure 47. Output power vs. load resistance

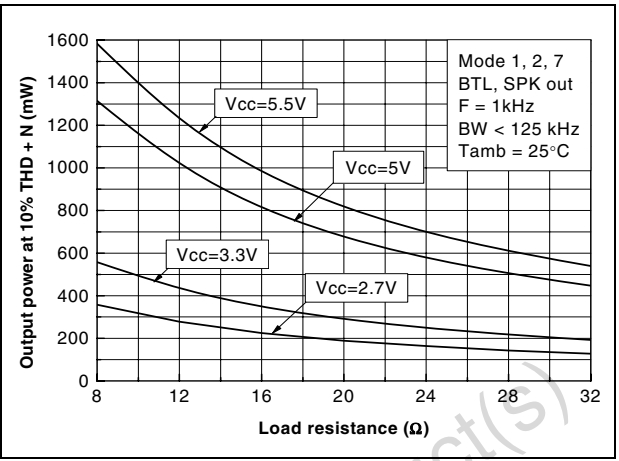


Figure 48. Output power vs. load resistance

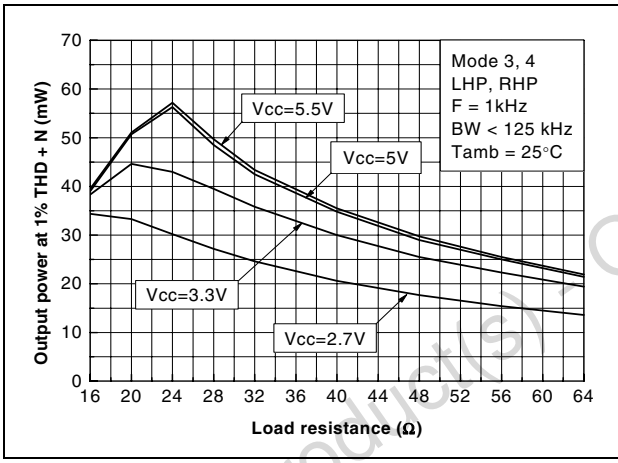


Figure 49. Output power vs. load resistance

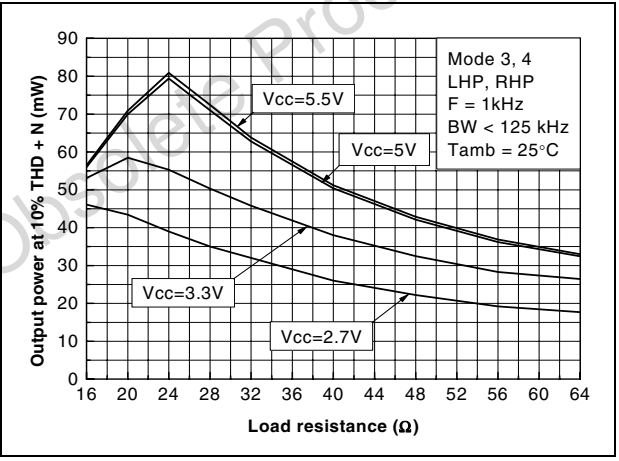


Figure 50. Output power vs. load resistance

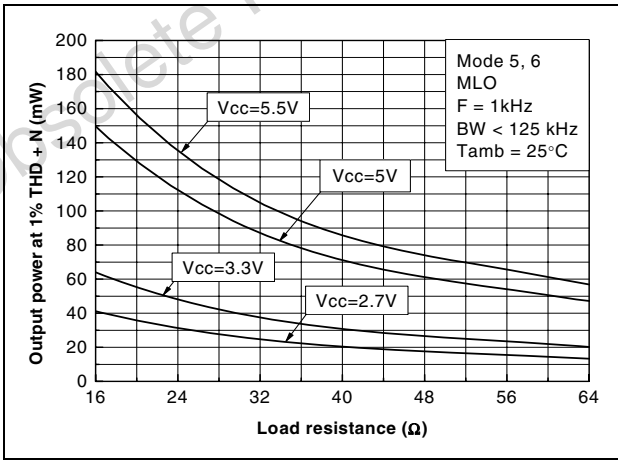


Figure 51. Output power vs. load resistance