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TS4973

1.2W Two Audio Inputs With Gain Control Power Amplifier with Standby Mode Active Low

- Operating from V_{CC} = 2.8V to 5.5V
- RAIL TO RAIL Input/Output
- 1.2W output power @ Vcc=5V, THD=1%, F=1kHz, with 8Ω load
- Ultra low consumption in standby mode (10nA)
- 53dB PSRR @ 217Hz from 2.8 to 5V
- Low distortion (0.5%)
- Gain settings pin: GS
- Unity gain stable
- Available in lead free flip-chip 9 x 300µm bumps

Description

At 3.3v, the TS4973 is an Audio Power Amplifier capable of delivering 500mW of continuous RMS output power into a 8Ω bridged-tied loads with 1% THD+N, and 150mWof continuous average power into 32Ω. An external standby mode control reduces the supply current to less than 10nA. An internal over-temperature shutdown protection is provided.

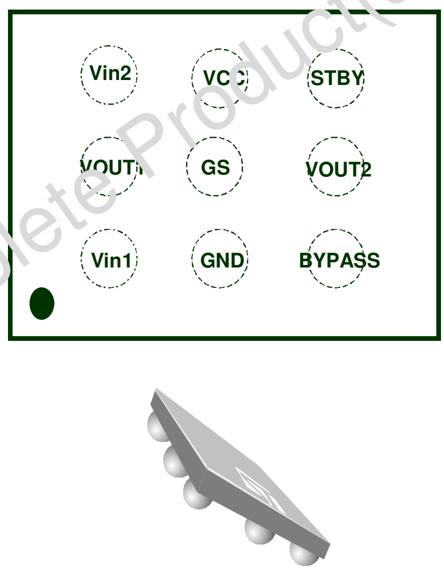
The TS4973 has been designed for high quality audio applications such as mobile phones and to minimize the number of external components. It has two inputs which can be used to switch the gain between 6dB (internal) or a user's adjustable gain setting with one external resistance.

Applications

- Mobile phones (cellular / cordless)
- PDAs
- Laptop/Notebook computers
- Portable audio devices

Pin Connections (top view)

TS4973IJT / TS4973EIJT - FLIP CHIP



Order Codes

Part Number	Temperature Range	Package	Packaging	Marking
TS4973IJT	-40, +85°C	Flip-Chip9	Tape & Reel	A73
TS4973EIJT		Lead Free Flip-Chip		
TS4973EKIJT	-40, +85°C	FC + Back Coating	Tape & Reel	

1 Application Schematic

Figure 1: Typical application schematic

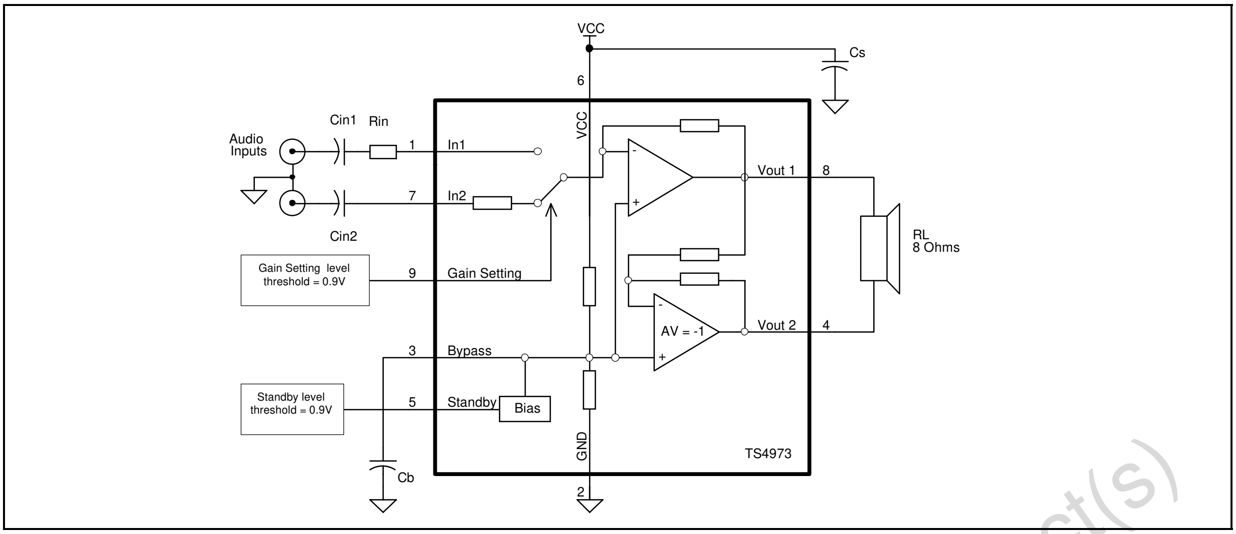


Table 1: Absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC	Supply voltage [1]	6	V
V_i	Input Voltage [2]	G_{ND} to V_{CC}	V
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Thermal Resistance Junction to Ambient [3]	200	°C/W
Pd	Power Dissipation	Internally Limited [4]	
ESD	Human Body Model [5]	1	kV
ESD	Machine Model (min. Value)	200	V
Latch-up	Latch-up Immunity	200	mA
	Lead Temperature (soldering, 10sec)	250	°C

1) All voltages values are measured with respect to the ground pin.
2) The magnitude of input signal must never exceed V_{CC} + 0.3V / G_{ND} - 0.3V
3) Device is protected in case of over temperature by a thermal shutdown active @ 150°C.
4) Exceeding the power derating curves during a long period, may involve abnormal operating condition.
5) Minimum value. Human body model, 100pF discharged through a 1.5kOhm resistor, into pin to Vcc device.

Table 2: Operating conditions

Symbol	Parameter	Value	Unit
VCC	Supply Voltage	2.8 to 5.5	V
VSTB	Standby Voltage Input: Device ON Device OFF	$1.5 \leq V_{STB} \leq V_{CC}$ $GND \leq V_{STB} \leq 0.4$	V
VGS	Gain Setting Voltage Input: External Gain (In1 Input) Internal Gain (In2 Input)	$1.5 \leq V_{STB} \leq V_{CC}$ $GND \leq V_{STB} \leq 0.4$	V
RL	Load Resistor	≥ 4	Ω
R_{thja}	Thermal Resistance Junction to Ambient [1]	90	°C/W

1) With Heat Sink Surface = 125mm^2

2 Electrical Characteristics

Table 3: Electrical Characteristics - V_{CC} = +5V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		6	8	mA
$I_{STANDBY}$	Standby Current No input signal, VGS = Gnd, Vstdby = Gnd, RL = 8Ω		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 8Ω		5	50	mV
Po	Output Power THD = 1% Max, f = 1kHz, RL = 8Ω	0.85	1.2		W
BTL GAIN	GS = Low (Av = 2) input signal Vin = 100mV rms, No load	5.6	6	6.4	dB
THD + N	Total Harmonic Distortion + Noise Po = 900mW rms, GS = Low (Av = 2) 20Hz < F < 20kHz, RL = 8Ω		0.5		%
PSRR	Power Supply Rejection Ratio[1] F = 217Hz, RL = 8Ω, GS = Low (Av = 2) Vripple = 200mVpp, Input Grounded, Cin = 220nF, Cb = 1µF		53		dB
PSRR	Power Supply Rejection Ratio[2] F = 217Hz, RL = 8Ω, GS = Low (Av = 2) Vripple = 200mVpp, Input Floating, Cb = 1µF		70		dB
Zin	Input Impedance GS = Low (Av = 2)	37.5	50	62.5	KΩ
Rfeed	Internal Feedback Resistor	37.5	50	62.5	KΩ
V_N	Output Voltage Noise F = 20Hz to 20kHz, RL = 8Ω Unweighted, Vstdby = Gnd A weighted, Vstdby = Gnd Unweighted, GS = Low (Av = 2) A weighted, GS = Low (Av = 2) Unweighted, GS = High (Av = 10) A weighted, GS = High (Av = 10)		 6 2.5 23 15 56 40		μV_{RMS}

1) Dynamic measurements - 20*log(rms(Vout)/rms (Vripple)). Vripple is an added sinus signal to Vcc @ F = 217Hz
2) Dynamic measurements - 20*log(rms(Vout)/rms (Vripple)). Vripple is an added sinus signal to Vcc @ F = 217Hz

Table 4: Electrical Characteristics - V_{CC} = +3.3V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.5	8	mA
$I_{STANDBY}$	Standby Current No input signal, VGS = Gnd, Vstdby = Gnd, RL = 8Ω		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 8Ω		5	50	mV
Po	Output Power THD = 1% Max, f = 1kHz, RL = 8Ω	350	500		mW
BTL GAIN	GS = Low (Av = 2) input signal Vin = 100mV rms, No load	5.6	6	6.4	dB
THD + N	Total Harmonic Distortion + Noise Po = 380mW rms, GS = Low (Av = 2) 20Hz < F < 20kHz, RL = 8Ω		0.5		%
PSRR	Power Supply Rejection Ratio[1] F = 217Hz, RL = 8Ω, GS = Low (Av = 2) Vripple = 200mVpp, Input Grounded, Cin = 220nF, Cb = 1μF		53		dB
PSRR	Power Supply Rejection Ratio[2] F = 217Hz, RL = 8Ω, GS = Low (Av = 2) Vripple = 200mVpp, Input Floating, Cb = 1μF		68		dB
Zin	Input Impedance GS = Low (Av = 2)	37.5	50	62.5	KΩ
Rfeed	Internal Feedback Resistor	37.5	50	62.5	KΩ
V_N	Output Voltage Noise F = 20Hz to 20kHz, RL = 8Ω Unweighted, Vstdby = Gnd A weighted, Vstdby = Gnd Unweighted, GS = Low (Av = 2) A weighted, GS = Low (Av = 2) Unweighted, GS = High (Av = 10) A weighted, GS = High (Av = 10)		 6 2.5 23 15 56 40		μV_{RMS}

1) Dynamic measurements - 20*log(rms(Vout)/rms (Vripple)). Vripple is an added sinus signal to Vcc @ F = 217Hz
2) Dynamic measurements - 20*log(rms(Vout)/rms (Vripple)). Vripple is an added sinus signal to Vcc @ F = 217Hz

Table 5: Electrical characteristics - V_{CC} = 2.8V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.5	8	mA
$I_{STANDBY}$	Standby Current No input signal, VGS = Gnd, Vstdby = Gnd, RL = 8Ω		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 8Ω		5	50	mV
BTL GAIN	GS = Low (Av = 2) input signal Vin = 100mV rms, No load	5.6	6	6.4	dB
Po	Output Power THD = 1% Max, f = 1kHz, RL = 8Ω	250	350		mW

Table 5: Electrical characteristics - V_{CC} = 2.8V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
THD + N	Total Harmonic Distortion + Noise Po = 250mW rms, GS = Low (Av = 2) 20Hz < F < 20kHz, RL = 8Ω		0.5		%
PSRR	Power Supply Rejection Ratio[1] F = 217Hz, RL = 8Ω, GS = Low (Av = 2) Vripple = 200mVpp, Input Grounded, Cin = 220nF, Cb = 1µF		53		dB
PSRR	Power Supply Rejection Ratio[2] F = 217Hz, RL = 8Ω, GS = Low (Av = 2) Vripple = 200mVpp, Input Floating, Cb = 1µF		68		dB
Zin	Input Impedance GS = Low (Av = 2)	37.5	50	62.5	KΩ
Rfeed	Internal Feedback Resistor	37.5	50	62.5	KΩ
V_N	Output Voltage Noise F = 20Hz to 20kHz, RL = 8Ω Unweighted, Vstdby = Gnd A weighted, Vstdby = Gnd Unweighted, GS = Low (Av = 2) A weighted, GS = Low (Av = 2) Unweighted, GS = High (Av = 10) A weighted, GS = High (Av = 10)		 6 2.5 23 15 56 40		μV_{RMS}

1) Dynamic measurements - 20*log(rms(Vout)/rms (Vripple)). Vripple is an added sinus signal to Vcc @ F = 217Hz
2) Dynamic measurements - 20*log(rms(Vout)/rms (Vripple)). Vripple is an added sinus signal to Vcc @ F = 217Hz

Table 6: Application Components Information

Components	Functional Description
Rin	Inverting input resistor which sets the closed loop gain (when GS = high) in conjunction with the internal feedback resistor Rfeed. This resistor also forms a high pass filter with Cin1 Fc = 1 / (2 x Pi x Rin x Cin1)
Cin1	Input coupling capacitor which blocks the DC voltage at the amplifier input terminal In1
Cin2	Input coupling capacitor which blocks the DC voltage at the amplifier input terminal In2. This capacitor also forms a high pass filter with Zin (internal input impedance when Gs = Low Fc = 1 / (2 x Pi x Zin x Cin2)
Cs	Supply Bypass capacitor which provides power supply filtering (Recommended value = 1µF)
Cb	Bypass pin capacitor which provides half supply filtering (Recommended value = 1µF)
Av	Closed loop gain in BTL configuration When Gs = Low, Av = 2 or 6dB When GS = high, Av = 2 x (Rfeed / Rin). Rfeed value see Electrical Characteristics.

Remarks:

1. All measurements, except PSRR measurements, are made with a supply bypass capacitor Cs = 1µF.
2. The standby response time is about 1µs.

Figure 2: Power supply rejection ratio (psrr) vs power supply

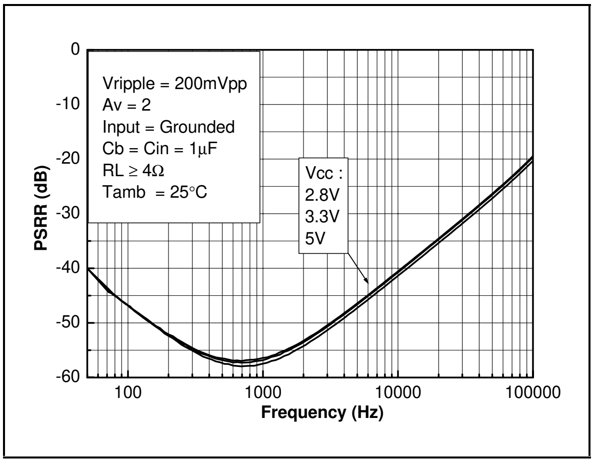


Figure 3: Power supply rejection ratio (PSRR) vs power supply

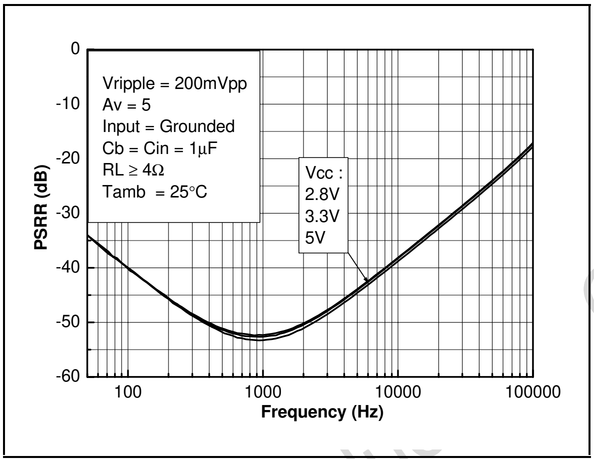


Figure 4: Power supply rejection ratio (PSRR) vs power supply

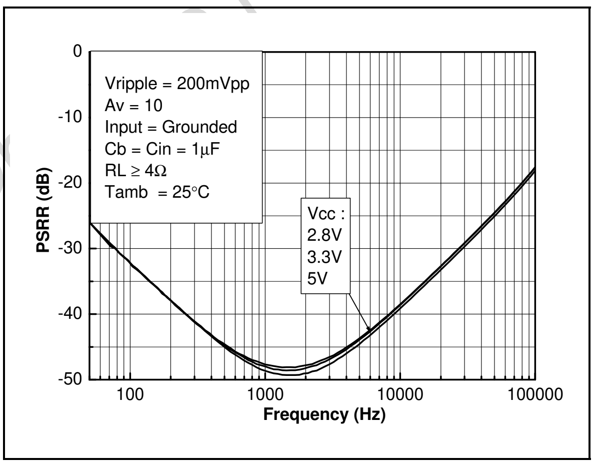


Figure 5: Power supply rejection ratio (PSRR) vs bypass capacitor

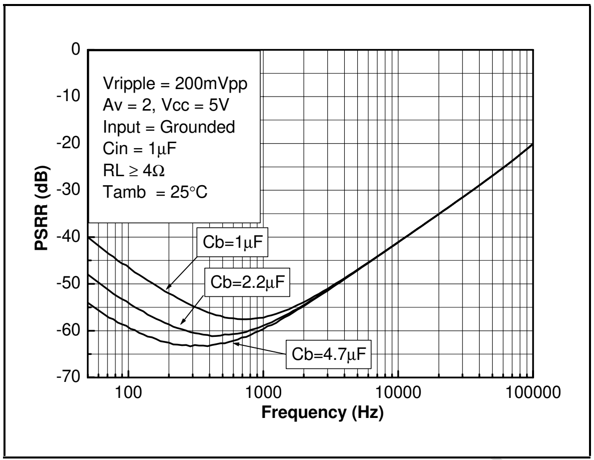


Figure 6: Power supply rejection ratio (PSRR) vs bypass capacitor

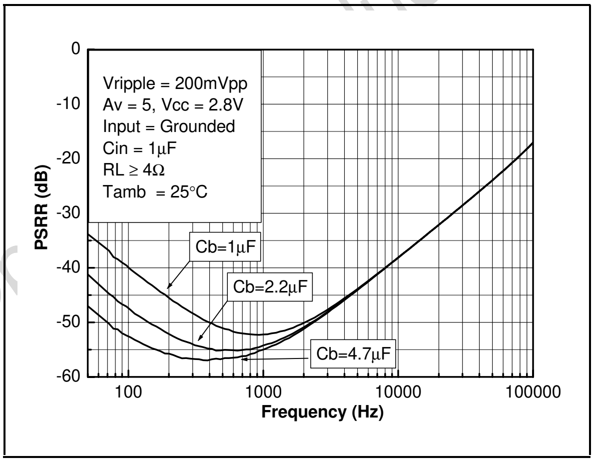


Figure 7: Power supply rejection ratio (PSRR) vs bypass capacitor

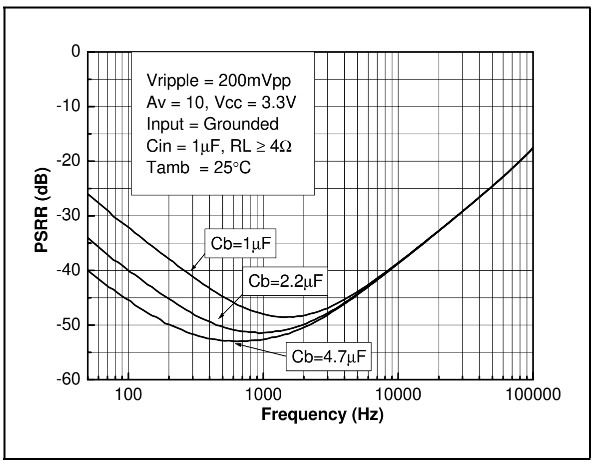


Figure 8: Power supply rejection ratio (PSRR)

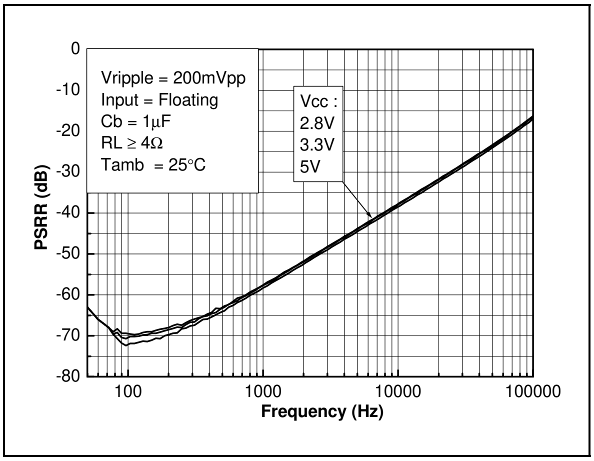


Figure 11: Signal to noise ratio vs power supply with a weighted filter

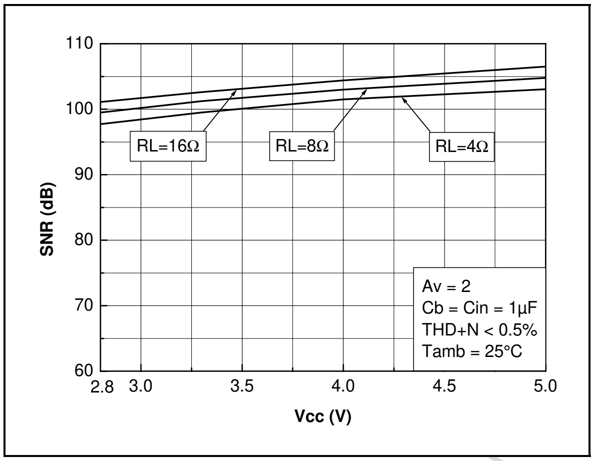


Figure 9: Crosstalk between inputs vs frequency

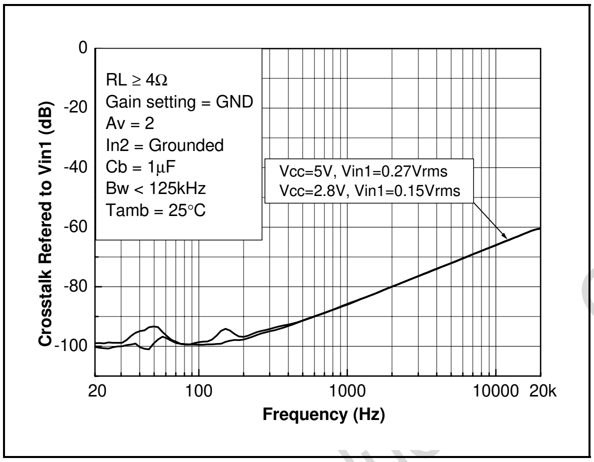


Figure 12: Signal to noise ratio vs power supply with a weighted filter

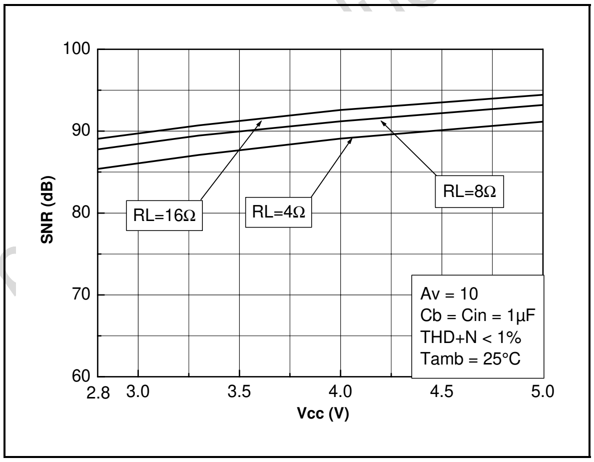


Figure 10: Crosstalk between inputs vs frequency

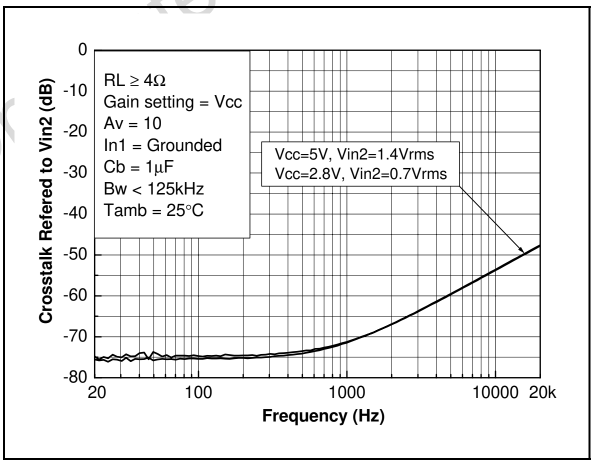


Figure 13: Signal to noise ratio vs power supply with unweighted filter (20Hz to 20kHz)

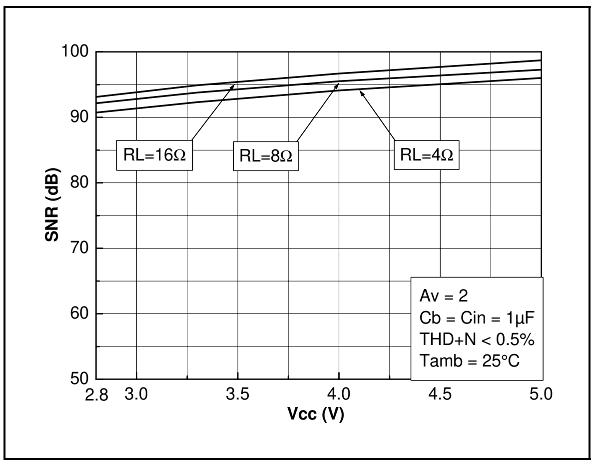


Figure 14: Signal to noise ratio vs power supply with unweighted filter (20Hz to 20kHz)

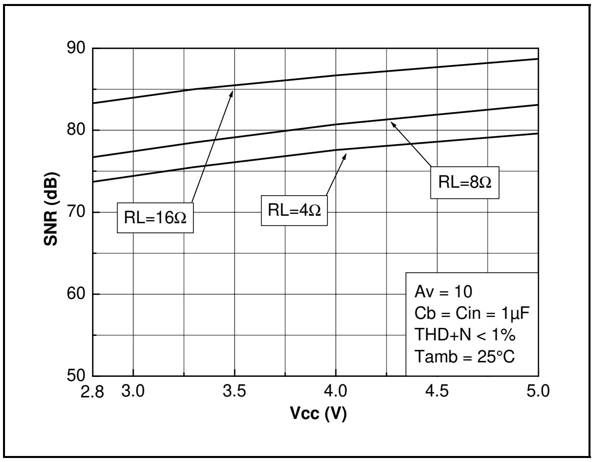


Figure 15: Output power vs power supply voltage

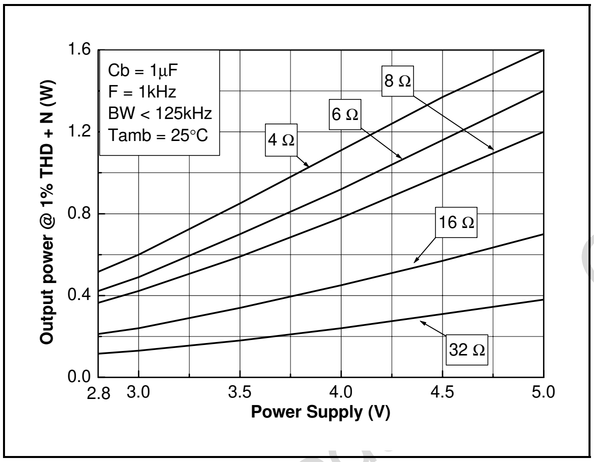


Figure 16: Output power vs power supply voltage

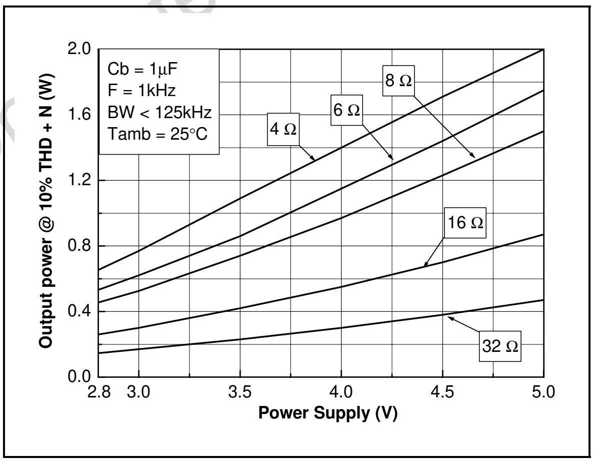


Figure 17: Power dissipation vs output power

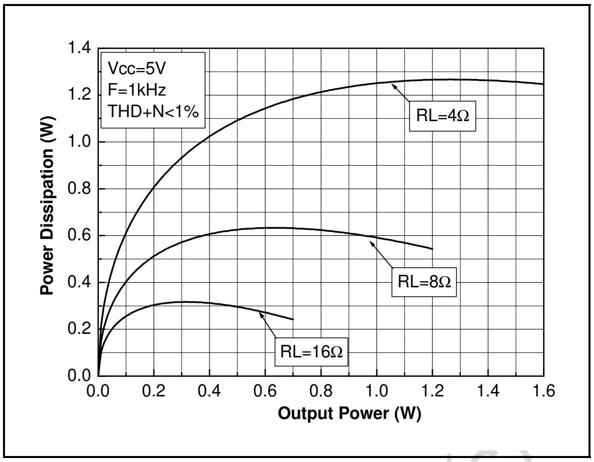


Figure 18: Power dissipation vs output power

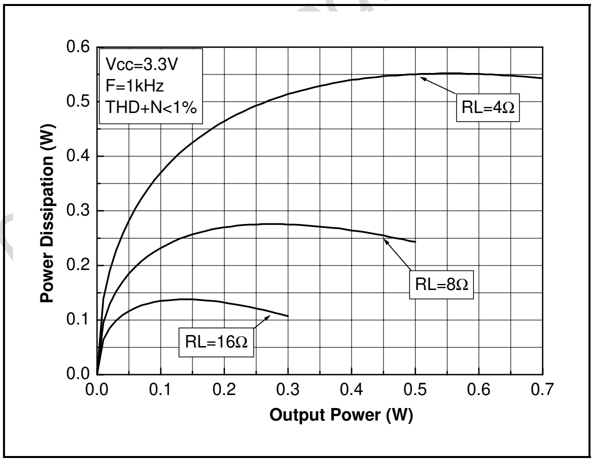


Figure 19: Power dissipation vs output power

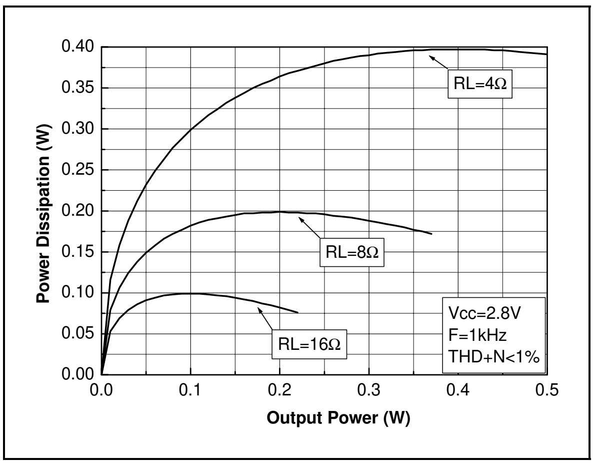


Figure 20: Power derating curves

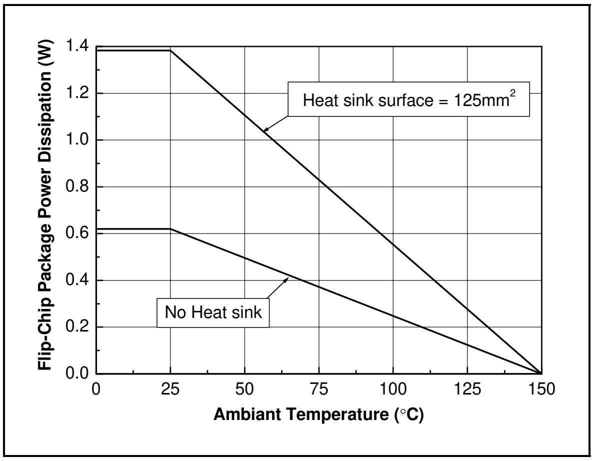


Figure 23: Current consumption vs power supply voltage

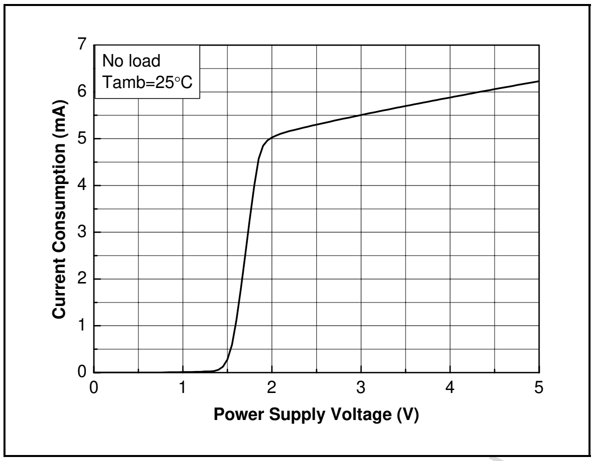


Figure 21: Clipping voltage vs power supply voltage and load resistor

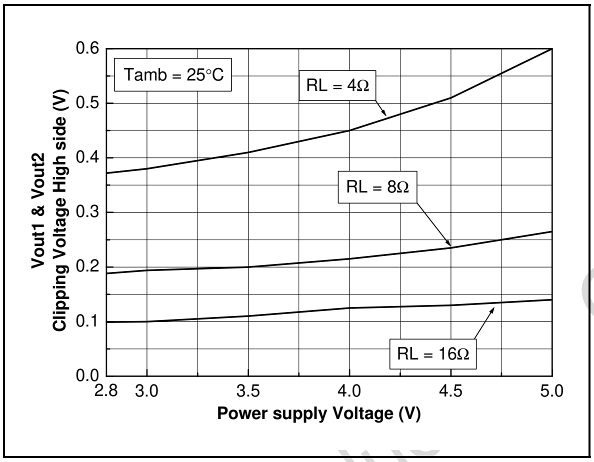


Figure 24: Current consumption vs standby voltage @ Vcc = 5V

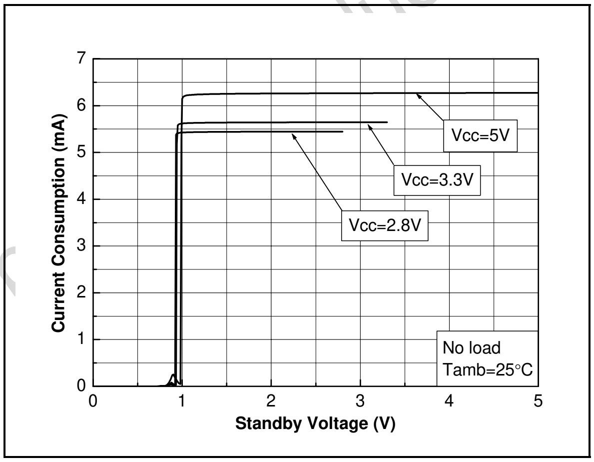


Figure 22: Clipping voltage vs power supply voltage and load resistor

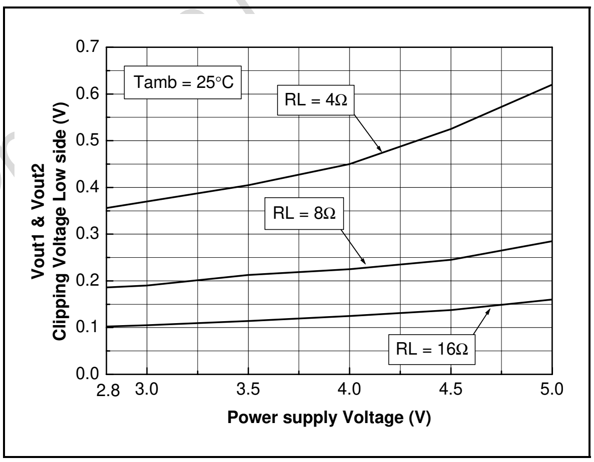


Figure 25: THD + N vs output power

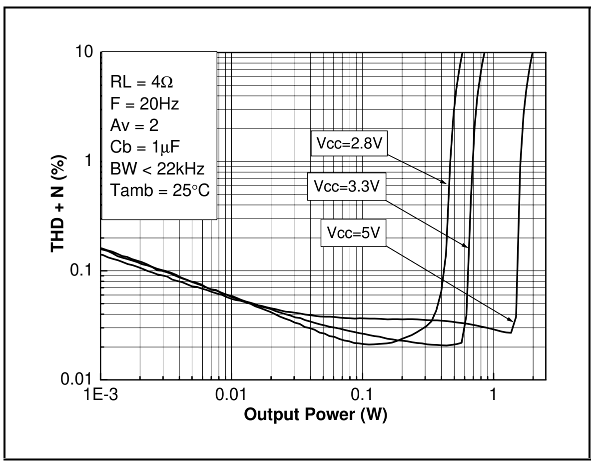


Figure 26: THD + N vs output power

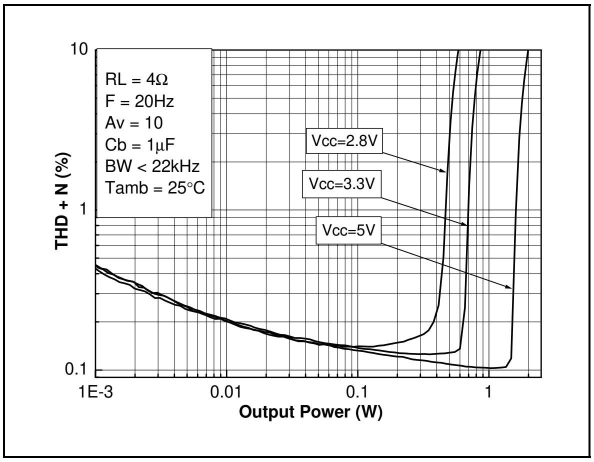


Figure 29: THD + N vs Output power

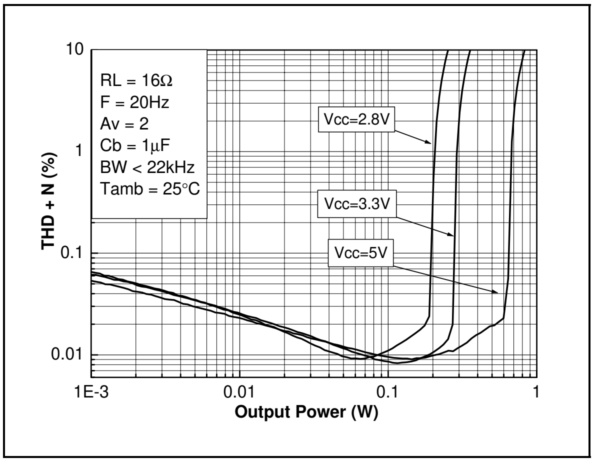


Figure 27: THD + N vs output power

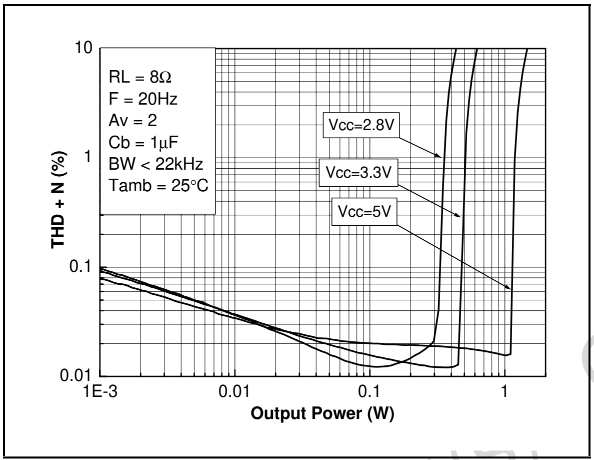


Figure 30: THD + N vs output power

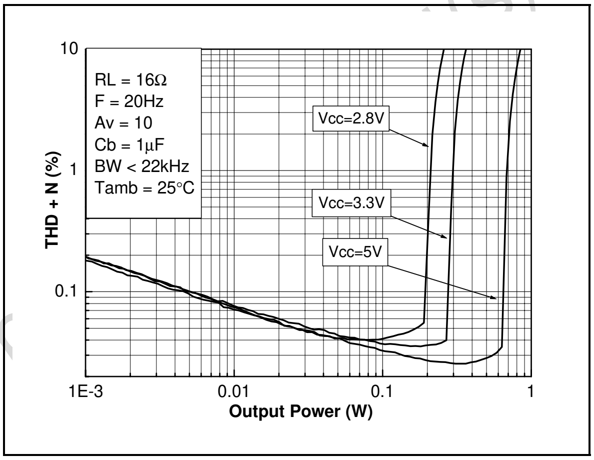


Figure 28: THD + N vs output power

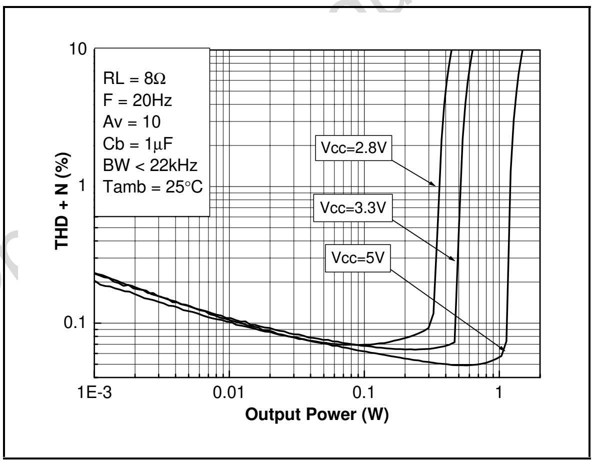


Figure 31: THD + N vs output power

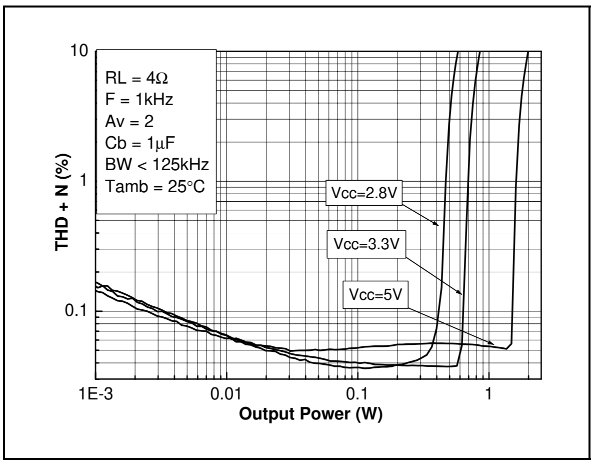


Figure 32: THD + N vs output power

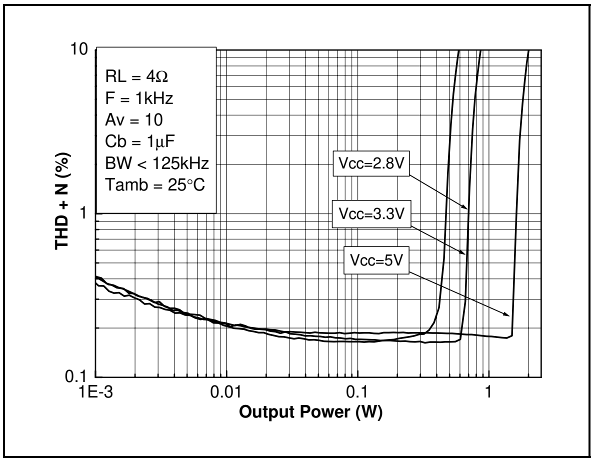


Figure 33: THD + N vs output power

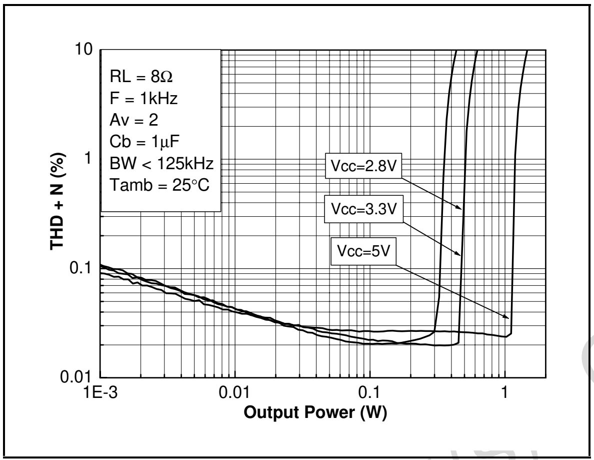


Figure 34: THD + N vs output power

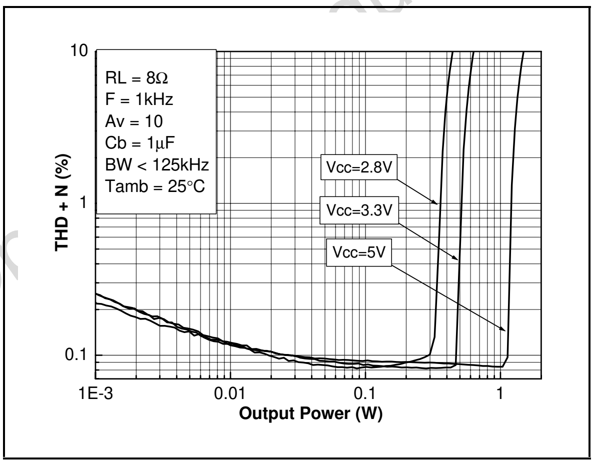


Figure 35: THD + N vs output power

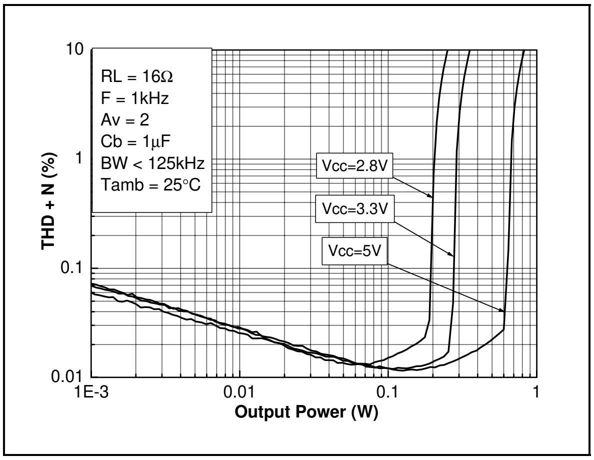


Figure 36: THD + N vs output power

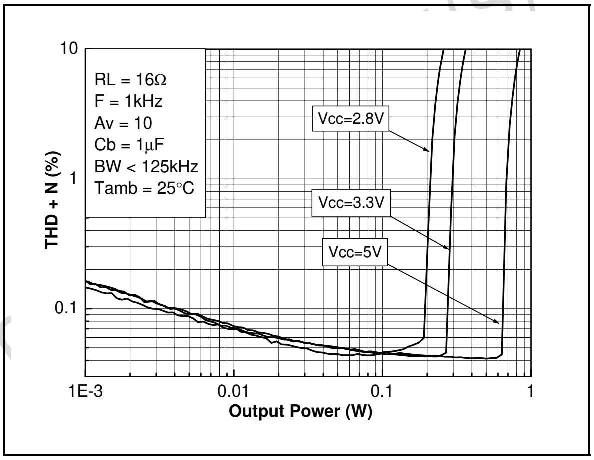


Figure 37: THD + N vs output power

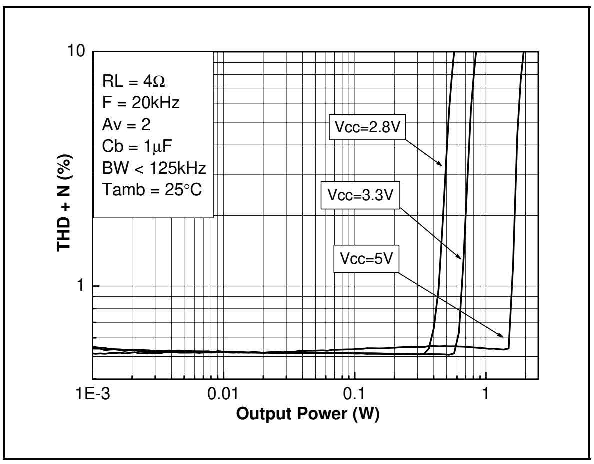


Figure 38: THD + N vs output power

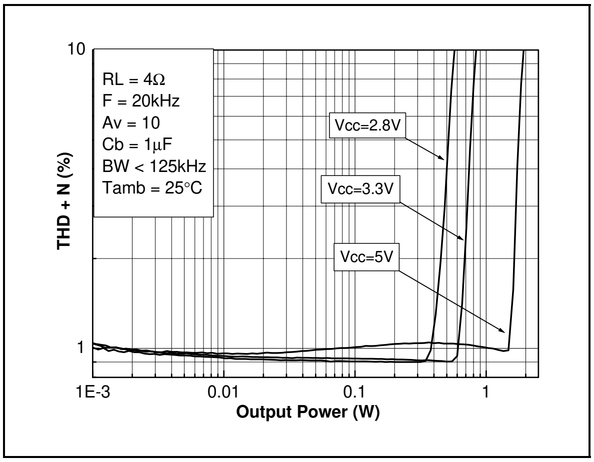


Figure 41: THD + N vs output power

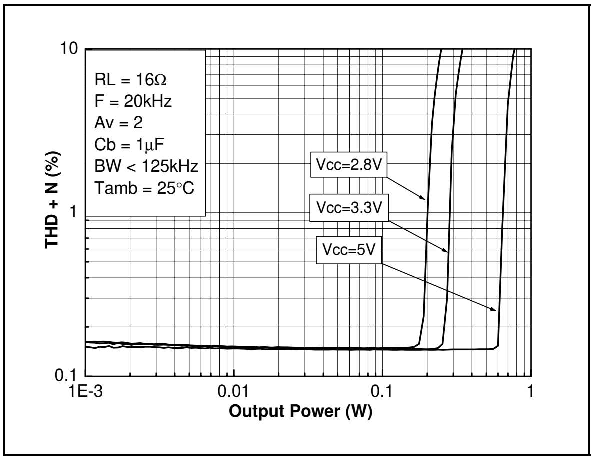


Figure 39: THD + N vs output power

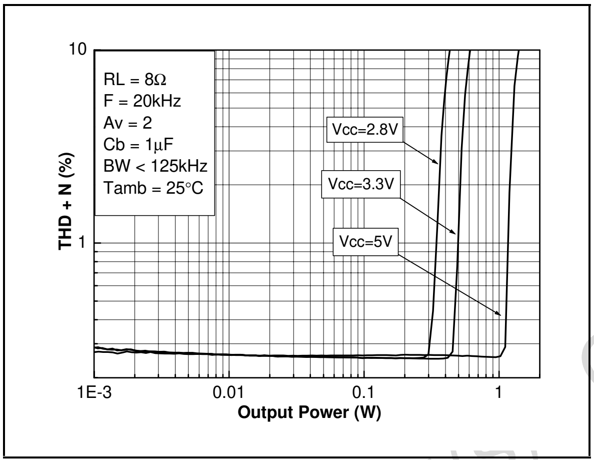


Figure 42: THD + N vs output power

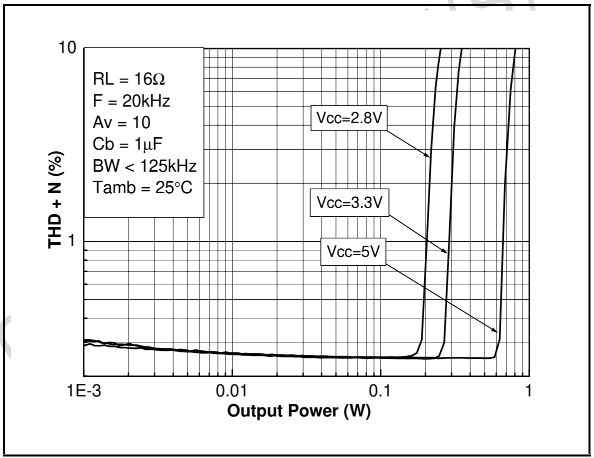


Figure 40: THD + N vs output power

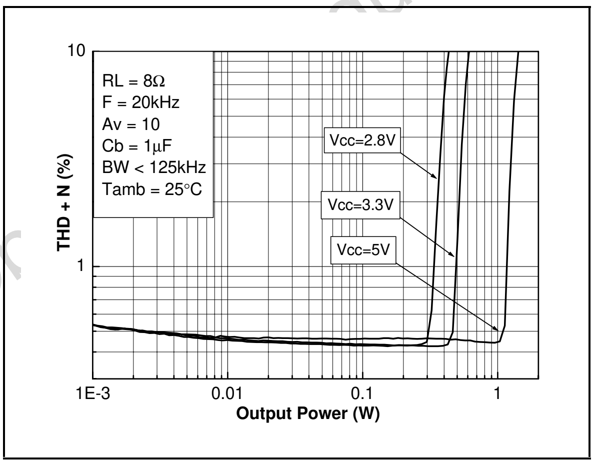


Figure 43: THD + N vs frequency

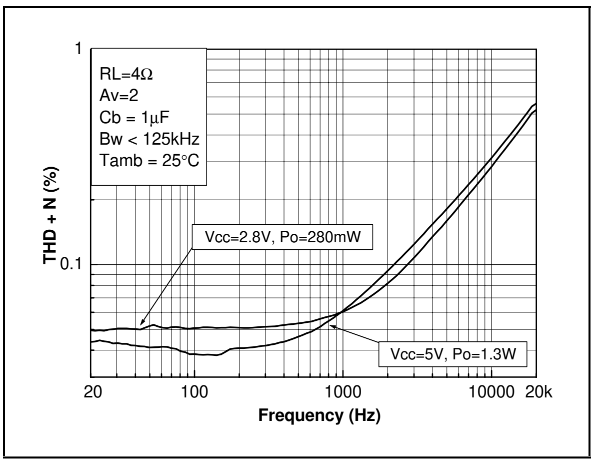


Figure 44: THD + N vs frequency

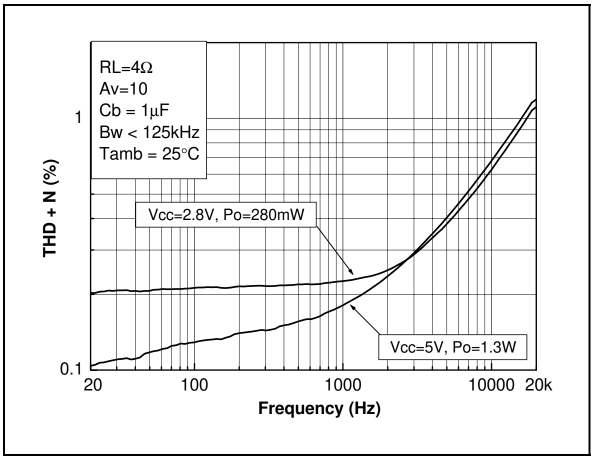


Figure 45: THD + N vs frequency

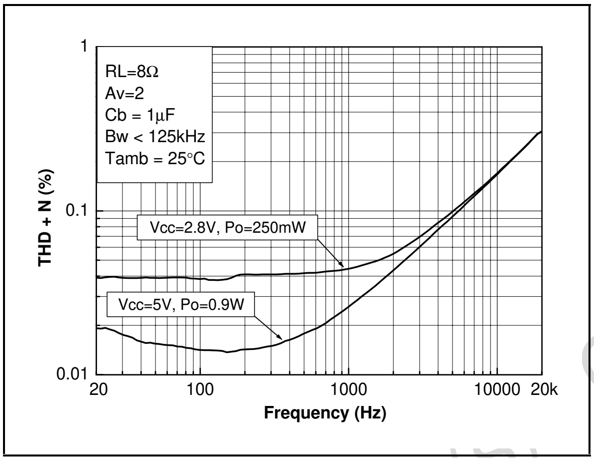


Figure 46: THD + N vs frequency

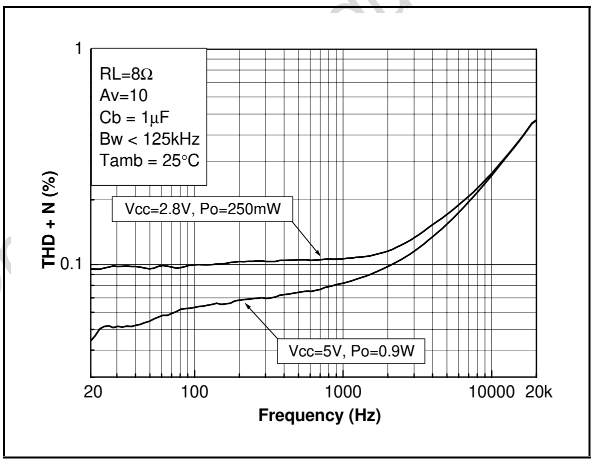


Figure 47: THD + N vs frequency

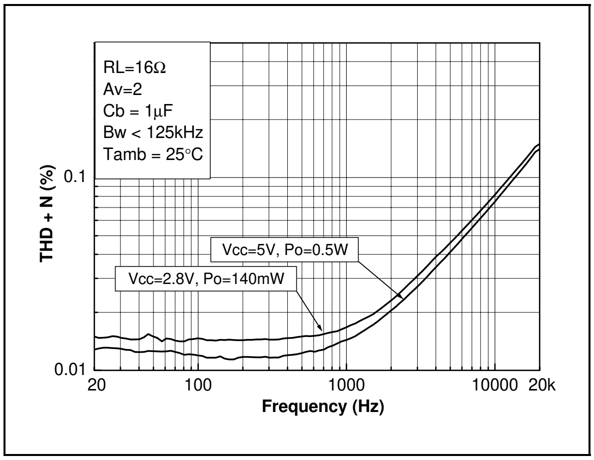
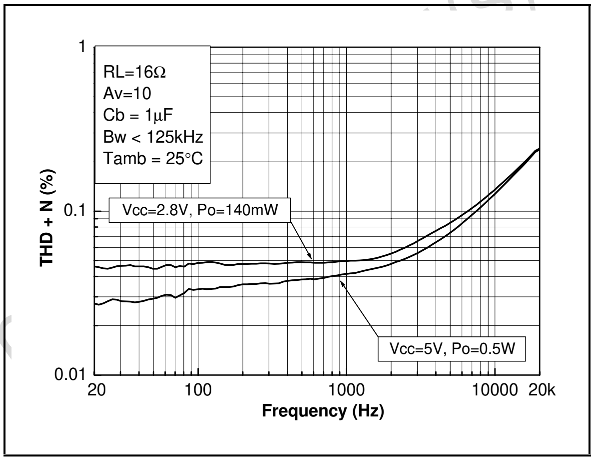


Figure 48: THD + N vs frequency



3 Application Information

3.1 BTL Configuration Principle

The TS4973 are monolithic power amplifiers with a BTL output type. BTL (Bridge Tied Load) means that each end of the load is connected to two single-ended output amplifiers. Thus, we have:

Single ended output 1 = Vout1 = Vout (V)
Single ended output 2 = Vout2 = -Vout (V)

And Vout1 - Vout2 = 2Vout (V)

The output power is:

$$Pout = \frac{(2\,Vout_{RMS})^2}{R_L}\ (W)$$

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single ended configuration.

3.2 Gain In Typical Application Schematic (cf. page1 of TS4973 datasheet)

Depending on gain select (Gs) voltage, the output is driven by In1 when Gs≥1.5V and by In2 when Gs≤0.4V. In the flat region (no C_{IN} effect), the gain is expressed by this general equation:

$$Av = \frac{Vout_1 - Vout_2}{Vin_{(1,2)}}$$

If Gs ≤ 0.4V: The typical value is

$$Av = \frac{Vout_1 - Vout_2}{Vin_2} = 2$$

with a range of:

$$1.9 \le Av = \frac{Vout_1 - Vout_2}{Vin_2} \le 2.1$$

If Gs ≥ 1.5V: The typical value is (Rin in kΩ)

$$Av = \frac{Vout_1 - Vout_2}{Vin_1} = \frac{100}{Rin}$$

with a range of :

$$\frac{75}{Rin} \le Av = \frac{Vout_1 - Vout_2}{Vin_1} \le \frac{125}{Rin}$$

Remark: Vout2 is in phase with Vin and Vout1 is phased 180° with Vin. This means that the positive terminal of the loudspeaker should be connected to Vout2 and the negative to Vout1.

3.3 Low frequency response

In the low frequency region, C_{IN} starts to have an effect. C_{IN} forms with R_{IN} (or the input impedance Zin when Gs ≤ 0.4V) a high-pass filter with a -3dB cut off frequency.

If Gs ≤ 0.4V: The typical value is (Cin_2 in nF)

$$F_{CL} = \frac{4823}{C_{in2}}\ (Hz)$$

with a range of

$$\frac{6366}{C_{in2}} \le F_{CL}\ (Hz) \le \frac{3789}{C_{in2}}$$

If Gs ≥ 1.5V: The value is (Rin in kΩ, Cin_1 in nF):

$$F_{CL} \le \frac{159000}{Rin\ C_{in1}}\ (Hz)$$

3.4 Power dissipation and efficiency

Hypothesis:

- Load voltage and current are sinusoidal (Vout and Iout)
- Supply voltage is a pure DC source (Vcc)

Regarding the load we have:

$$V_{OUT} = V_{PEAK} \sin \omega t\ (V)$$

and

$$I_{OUT} = \frac{V_{OUT}}{R_L}\ (A)$$

and

$$P_{OUT} = \frac{{V_{PEAK}}^2}{2R_L}\ (W)$$

Then, the average current delivered by the supply voltage is:

$$Icc_{AVG} = 2\frac{V_{PEAK}}{\pi R_L}\ (A)$$

The power delivered by the supply voltage is:
Psupply = Vcc Icc_{AVG} (W)

Then, the **power dissipated by the amplifier** is:
Pdiss = Psupply - Pout (W)

$$Pdiss = \frac{2\sqrt{2}\,Vcc}{\pi\sqrt{R_L}}\sqrt{P_{OUT}} - P_{OUT}\ (W)$$

and the maximum value is obtained when:

$$\frac{\partial Pdiss}{\partial P_{OUT}} = 0$$

and its value is:

$$Pdiss\,max = \frac{2\,Vcc^2}{\pi^2 R_L}\ (W)$$

Remark: This maximum value is only dependent upon power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply

$$\eta = \frac{P_{OUT}}{P_{supply}} = \frac{\pi V_{PEAK}}{4 Vcc}$$

The maximum theoretical value is reached when Vpeak = Vcc, so

$$\frac{\pi}{4} = 78.5\%$$

3.5 Decoupling of the circuit

Two capacitors are needed to bypass properly the TS4973. A power supply bypass capacitor C_S and a bias voltage bypass capacitor C_B.

C_S has particular influence on the THD+N in the high frequency region (above 7kHz) and an indirect influence on power supply disturbances. With 1µF, you can expect similar THD+N performances to those shown in the datasheet.

In the high frequency region, if C_S is lower than 1µF, it increases THD+N and disturbances on the power supply rail are less filtered.
On the other hand, if C_S is higher than 1µF, those disturbances on the power supply rail are more filtered.

$\mathbf{C_B}$ has an influence on THD+N at lower frequencies, but its function is critical to the final result of PSRR (with input grounded and in the lower frequency region).

If C_B is lower than 1µF, THD+N increases at lower frequencies and PSRR worsens.
If C_B is higher than 1µF, the benefit on THD+N at lower frequencies is small, but the benefit to PSRR is substantial.

Note that C_{IN} has a non-negligible effect on PSRR at lower frequencies. The lower the value of C_{IN}, the higher the PSRR.

3.6 Wake-up Time: T_{WU}

T_{WU} is directly linked to the size of the bypass capacitor Cb. The slower the speed is, the higher Cb is. When power supply is apply or standby command is released, output amplifier are immediately un function. At this moment, the charge of Cb begins and the internal bias voltage, raise at the speed controlled by Cb. So, we define the T_{WU} when the internal bias voltage reaches 80% of the final value. With this condition, we can write with Cb in µF:

$$T_{WU} \approx 0.42\ Cb\ (s)$$

3.7 Shutdown time

When the standby command is set, the time to put the two output stage in high impedance and the internal circuitry in shutdown mode is a few microseconds.

3.8 Pop and Click performance

Pop and Click performance is intimately linked with the size of the input capacitor Cin and the bias voltage bypass capacitor Cb.

Size of Cin is due to the lower cut-off frequency and PSRR value requested. Size of Cb is due to THD+N and PSRR requested always in lower frequency.

Moreover, Cb determines the speed that the amplifier turns ON. The slower the speed is, the softer the turn ON noise is.

The charge time of Cb is directly proportional to the internal generator resistance 350kΩ.
Then, the charge time constant for Cb is
$\boldsymbol{\tau b = 350k\Omega x Cb}$ (s)

As Cb is directly connected to the non-inverting input and if we want to minimize, in amplitude and duration, the output spike on Vout1, Cin must be charged faster than Cb. The charge time constant of Cin is:

If Gs ≤ 0.4V: $\boldsymbol{\tau in = 40000 x Cin_2}$ (s)

If Gs ≥ 1.5V: $\boldsymbol{\tau in = Rin x Cin_1}$ (s)

Thus we have the relation
$\boldsymbol{\tau in << \tau b}$ (s)

The respect of this relation permits to minimize the pop and click noise.

Remark: Minimize Cin and Cb has a benefit on pop and click phenomena but also on cost and size of the application.

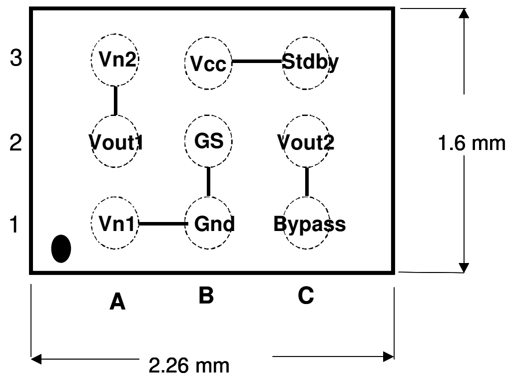
3.9 Biasing of Cin_1 and Cin_2

An internal bias circuitry allow to keep Cin_1 and Cin_2 always bias with the right DC value.

This circuitry eliminates all "possible clicks" when gain select pin is used to switch for a gain to another.

4 Mechanical Data

Figure 49: Daisy chain mechanical data (top view: all drawings dimensions are in millimeters)



Remarks:

Daisy chain sample is featuring pins connection two by two. The schematic above is illustrating the way connecting pins each other. This sample is used for testing continuity on board. PCB needs to be designed on the opposite way, where pin connections are not done on daisy chain samples. By that way, just connecting an Ohmmeter between pin 8 and pin 1, the soldering process continuity can be tested.

Table 7: Order Codes

Part Number	Temperature Range	Package	Marking
		J	
TSDC05IJT	-40, +85°C	•	DC5

Figure 50: TS4973 footprint recommendation

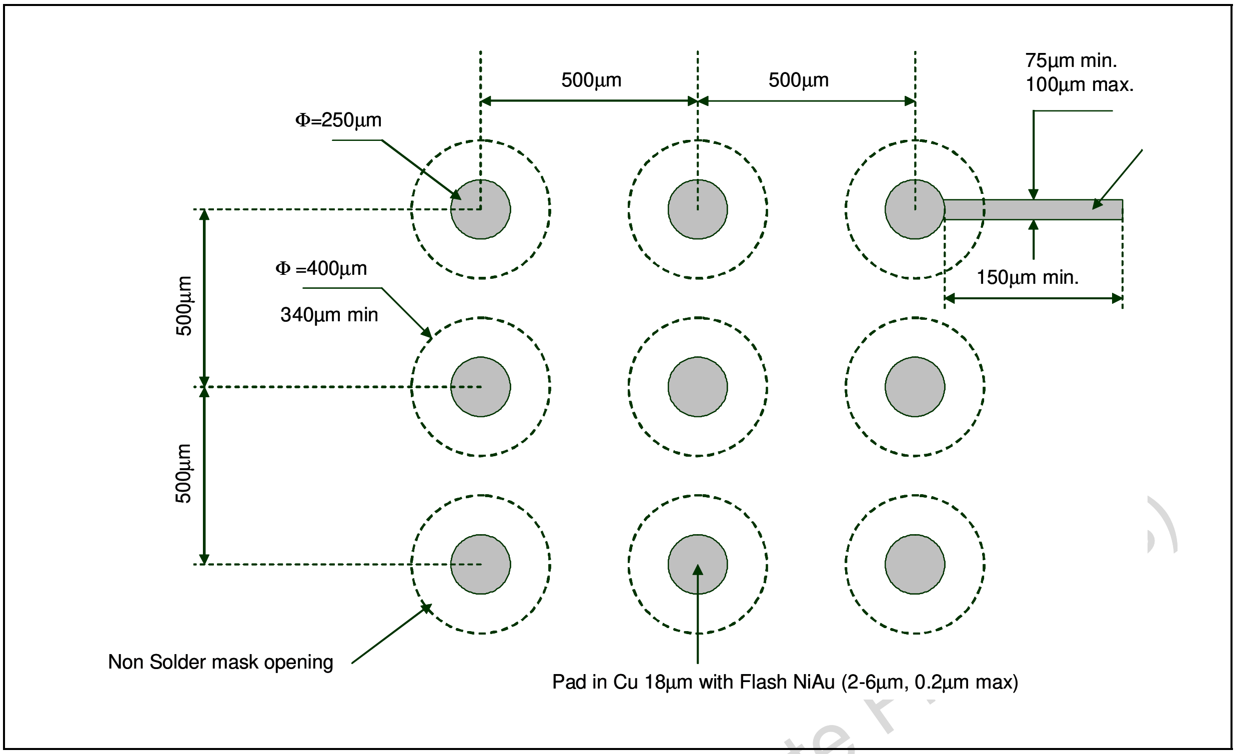


Figure 51: Pin out (top view)

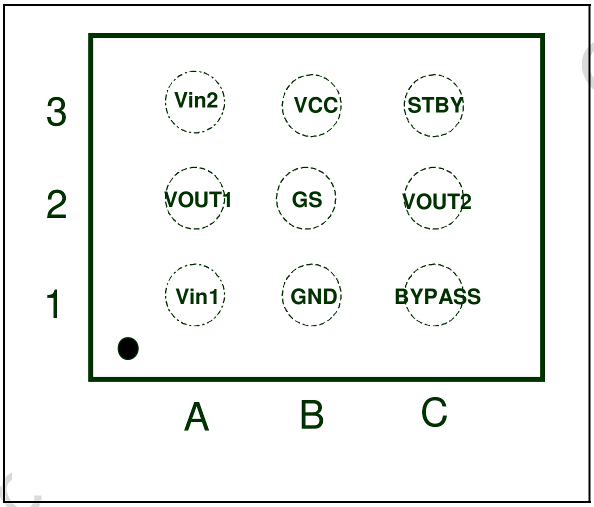
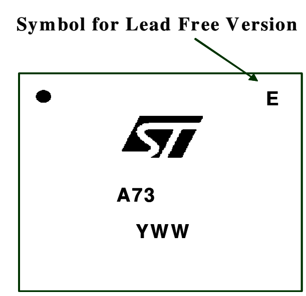


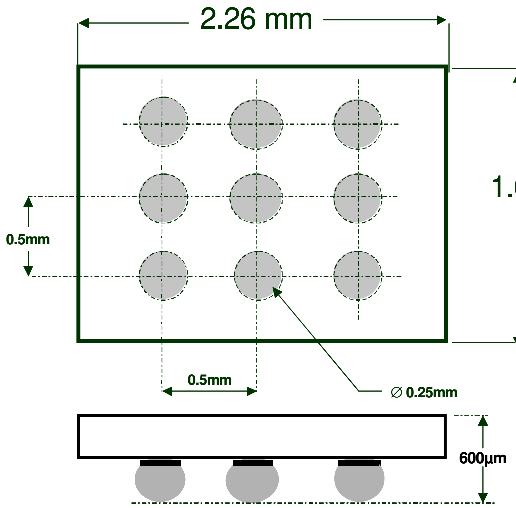
Figure 52: Marking (top view)



- Logo: **ST**
- Part Number: **A73**
- Three digit Date Code: **YWW**
- The Dot is for marking pin **A1**
- **E** symbol for Lead Free only

5 Package Mechanical Data

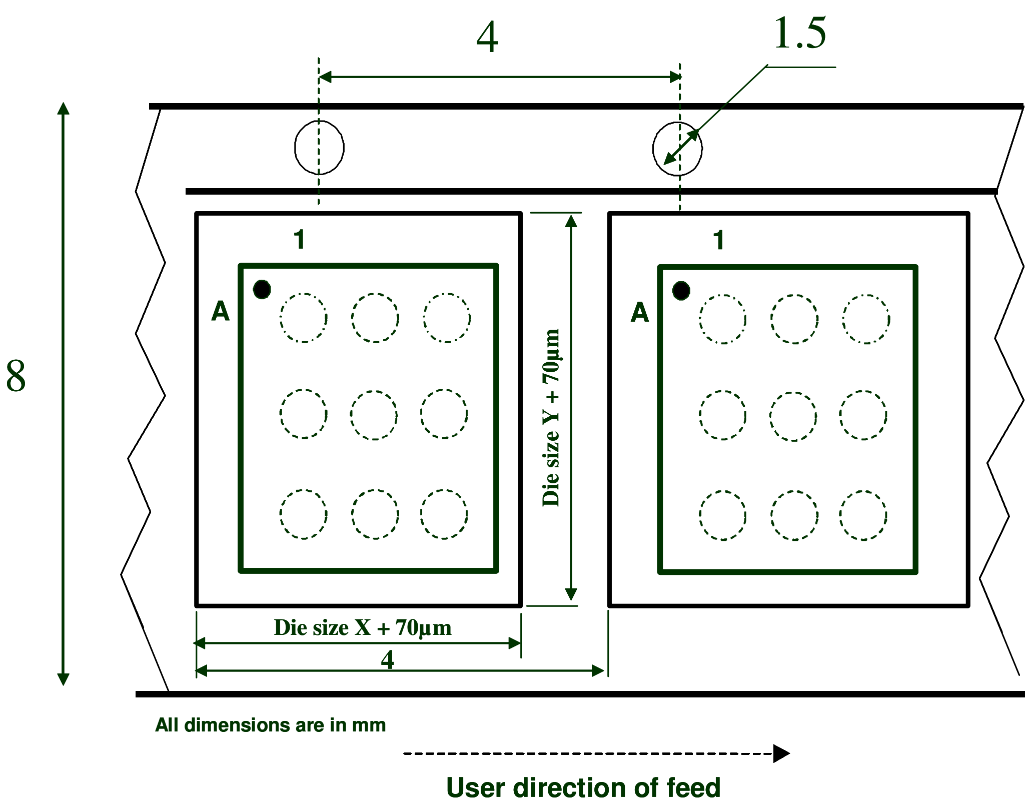
Figure 53: Flip-Chip - 9 bumps



- Die size: **2.26mm x 1.6mm** ± 30µm
- Die height (including bumps): **600µm**
- Bumps diameter: **315µm** ±50µm
- Bump Diameter Before Reflow: **300µm** ±10µm
- Bumps Height: **250µm** ±40µm
- Die Height: **350µm** ±20µm
- Pitch: **500µm** ±50µm
- Coplanarity: **60µm max**
- * Back Coating height : **100µm** ±10µm

* Optional

Figure 54: Tape & reel specification (top view)



6 Revision History

Date	Revision	Description of Changes
01 Aug 2004	1	First Release
01 Oct 2004	2	Flip Chip with Back Coating Order Code

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