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Features

- **Object Code Compatible with Earlier TS68000 Microprocessors**
- **Addressing Mode Extensions for Enhanced Support of High Level Languages**
- **New Bit Field Data Type Accelerates Bit-oriented Application, i.e. Video Graphics**
- **Fast on-chip Instruction Cache Speed Instructions and Improves Bus Bandwidth**
- **Co-processor Interface to Companion 32-bit Peripherals: TS68881 and TS68882 Floating Point Co-processors**
- **Pipelined Architecture with High Degree of Internal Parallelism Allowing Multiple Instructions to be Executed Concurrently**
- **High Performance Asynchronous Bus in Non-multiplexed and Full 32 Bits**
- **Dynamic Bus Sizing Efficiently Supports 8-, 16-, 32-bit Memories and Peripherals**
- **Full Support of Virtual Memory and Virtual Machine**
- **Sixteen 32-bit General-purpose Data and Address Registers**
- **Two 32-bit Supervisor Stack Pointers and 5 Special Purpose Control Registers**
- **18 Addressing Modes and 7 Data Types**
- **4-Gbyte Direct Addressing Range**
- **Processor Speed: 16.67 MHz - 20 MHz - 25 MHz**
- **Power Supply: 5.0 V_{DC} ± 10%**

Description

The TS68020 is the first full 32-bit implementation of the TS68000 family of microprocessors. Using HCMOS technology, the TS68020 is implemented with 32-bit registers and data paths, 32-bit addresses, a rich instruction set, and versatile addressing modes.

Screening/Quality

This product is manufactured in full compliance with either:
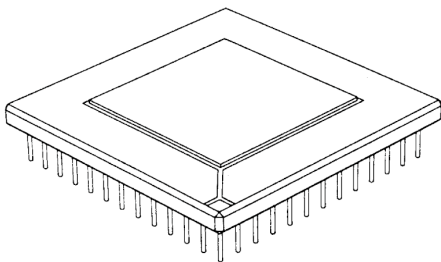
- MIL-STD-883 (class B)
- DESC 5962 - 860320
- or according to Atmel standards

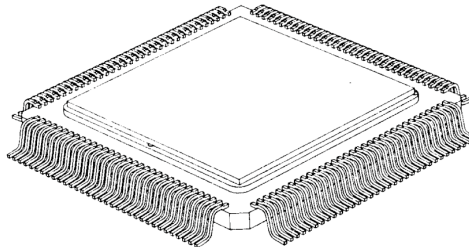See "Ordering Information" on page 43.

Pin connection: see page 3.

HCMOS 32-bit Virtual Memory Microprocessor

TS68020

R suffix
PGA 114
Ceramic Pin Grid Array

F suffix
**CQFP 132**
Ceramic Quad Flat Pack

Introduction

The TS68020 is a high-performance 32-bit microprocessor. It is the first microprocessor to have evolved from a 16-bit machine to a full 32-bit machine that provides 32-bit address and data buses as well as 32-bit internal structures. Many techniques were utilized to improve performance and at the same time maintain compatibility with other processors of the TS68000 Family. Among the improvements are new addressing modes which better support high-level language structures, an expanded instruction set which provides 32-bit operations for the limited cases not supported by the TS68000 and several new instructions which support new data types. For special-purpose applications when a general-purpose processor alone is not adequate, a co-processor interface is provided.

The TS68020 is a high-performance microprocessor implemented in HCMOS, low power, small geometry process. This process allows CMOS and HMOS (high density NMOS) gates to be combined on the same device. CMOS structures are used where speed and low power is required, and HMOS structures are used where minimum silicon area is desired. This technology enables the TS68020 to be very fast while consuming less power (less than 1.5 watts) and still have a reasonably small die size. It utilizes about 190.000 transistors, 103.000 of which are actually implemented. The package is a pin-grid array (PGA) with 114 pins, arranged 13 pins on a side with a depopulated center and 132 pins ceramic quad flat pack.
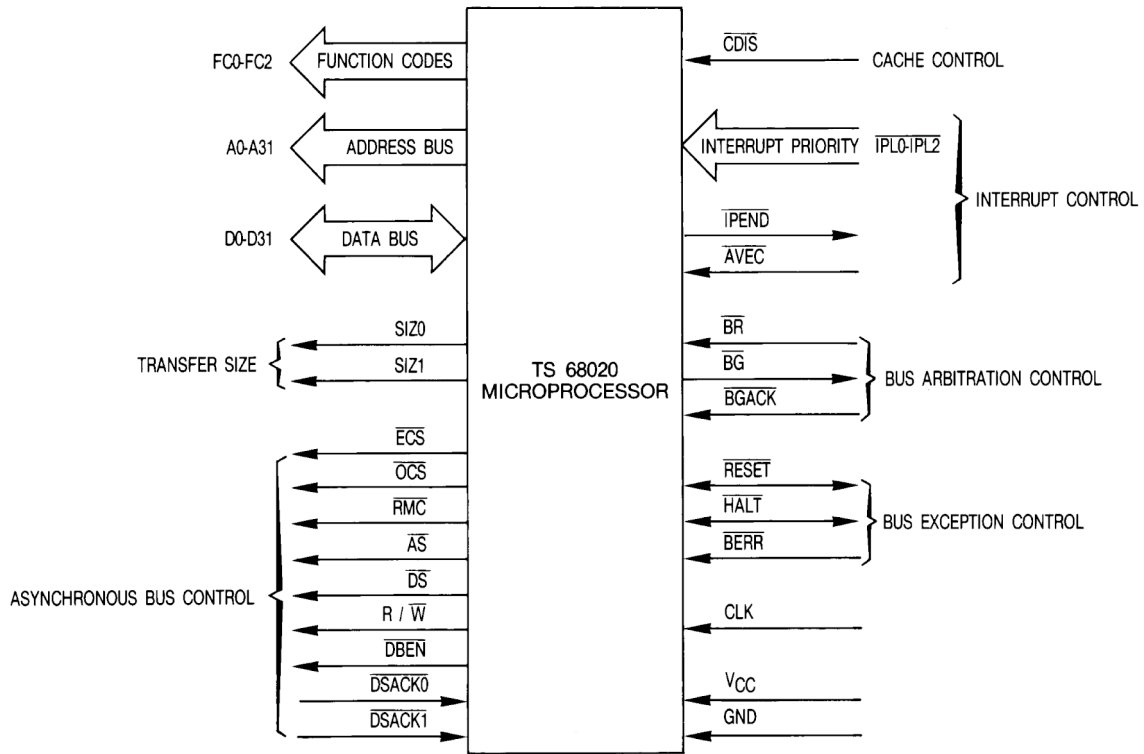
Figure 1 is a block diagram of the TS68020. The processor can be divided into two main sections: the bus controller and the micromachine. This division reflects the autonomy with which the sections operate.

Figure 1. TS68020 Block Diagram
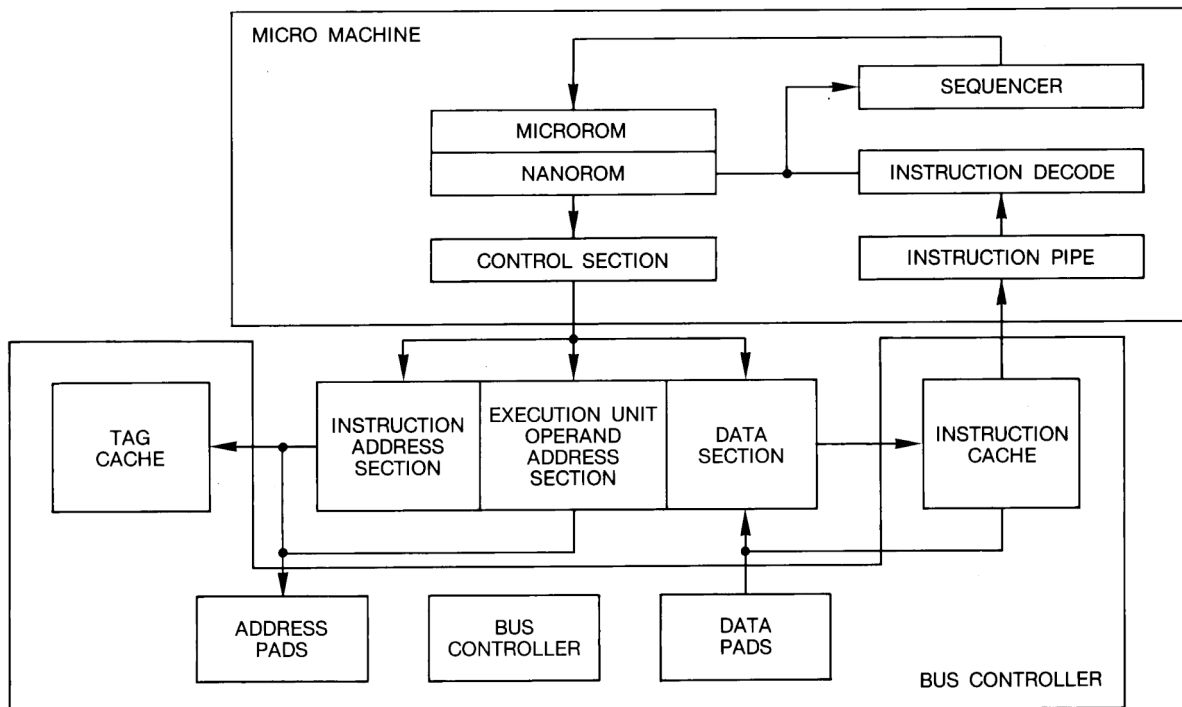
The bus controller consists of the address and data pads and multiplexers required to support dynamic bus sizing, a macro bus controller which schedules the bus cycles on the basis of priority with two state machines (one to control the bus cycles for operated accesses and the other to control the bus cycles for instruction accesses), and the instruction cache with its associated control.

The micromachine consists of an execution unit, nanorom and microrom storage, an instruction decoder, an instruction pipe, and associated control sections. The execution unit consists of an address section, an operand address section, and a data section. Microcode control is provided by a modified two-level store of microrom and nanorom. Programmed logical arrays (PLAs) are used to provide instruction decode and sequencing information. The instruction pipe and other individual control sections provide the secondary decode of instructions and generated the actual control signals that result in the decoding and interpretation of nanorom and micorom information.

Figure 2. PGA Terminal Designation

Figure 3. CQFP Terminal Designation

Figure 4. Functional Signal Groups

Signal Description

Figure 4 illustrates the functional signal groups and Table 1 lists the signals and their function.

The V_{CC} and GND pins are separated into four groups to provide individual power supply connections for the address bus buffers, data bus buffers, and all other output buffers and internal logic.

Group	V_{CC}	GND
Address Bus	A9, D3	A10, B9,C3, F12
Data Bus	M8, N8, N13	L7, L11, N7, K3
Logic	D1, D2, E3, G11, G13	G12, H13, J3, K1
Clock	—	B1

Table 1. Signal Index

Signal Name	Mnemonic	Function
Address Bus	A0-A31	32-bit Address Bus Used to address any of 4, 294, 967, 296 bytes.
Data Bus	D0-D31	32-bit Data Bus Used to Transfer 8, 16, 24 or 32 bits of Data Per Bus Cycle.
Function Codes	FC0-FC2	3-bit Function Case Used to Identify the Address Space of Each Bus Cycle.
Size	SIZ0/SIZ1	Indicates the Number of Bytes Remaining to be Transferred for this Cycle. These Signals, Together with A0 And A1, Define the Active Sections of the Data Bus.
Read-Modify-Write Cycle	$\overline{RMC}$	Provides an Indicator that the Current Bus Cycle is Part of an Indivisibleread-modify-write Operation.
External Cycle Start	$\overline{ECS}$	Provides an Indication that a Bus Cycle is Beginning.
Operand Cycle Start	$\overline{OCS}$	Identical Operation to that of ECS Except that OCS Is Asserted Only During the First Bus Cycle of an Operand Transfer.
Address Strobe	$\overline{AS}$	Indicates that a Valid Address is on The Bus.
Data Strobe	$\overline{DS}$	Indicates that Valid Data is to be Placed on the Data Bus by an External Device or has been Laced on the Data Bus by the TS68020.
Read/Write	R/$\overline{W}$	Defines the Bus Transfer as an MPU Read or Write.
Data Buffer Enable	$\overline{DBEN}$	Provides an Enable Signal for External Data Buffers.
Data Transfer and Size Acknowledge	$\overline{DSACK0}/\overline{DSACK1}$	Bus Response Signals that Indicate the Requested Data Transfer Operation is Completed. In Addition, these Two Lines Indicate the Size of the External Bus Port on a Cycle-by-cycle Basis.
Cache Disable	$\overline{CDIS}$	Dynamically Disables the On-chip Cache to Assist Emulator Support.
Interrupt Priority Level	$\overline{IPL0}$-$\overline{IPL2}$	Provides an Encoded Interrupt Level to the Processor.
Autovector	$\overline{AVEC}$	Requests an Autovector During an Interrupt Acknowledge Cycle.
Interrupt Pending	$\overline{IPEND}$	Indicates that an Interrupt is Pending.
Bus Request	$\overline{BR}$	Indicates that an External Device Requires Bus Mastership.
Bus Grant	$\overline{BG}$	Indicates that an External Device may Assume Bus Mastership.
Bus Grant Acknowledge	$\overline{BGACK}$	Indicates that an External Device has Assumed Bus Mastership.
Reset	$\overline{RESET}$	System Reset.
Halt	$\overline{HALT}$	Indicates that the Processor Should Suspend Bus Activity.
Bus Error	$\overline{BERR}$	Indicates an Invalid or Illegal Bus Operation is Being Attempted.
Clock	CLK	Clock Input to the Processor.
Power Supply	V_{CC}	+5-volt ± 10% Power Supply.
Ground	GND	Ground Connection.

Detailed Specifications

Scope

This drawing describes the specific requirements for the microprocessor 68020, 16.67 MHz, 20 MHz and 25 MHz, in compliance with the MIL-STD-883 class B.

Applicable Documents

MIL-STD-883

- MIL-STD-883: Test Methods and Procedures for Electronics
- MIL-PRF-38535 appendix A: General Specifications for Microcircuits
- Desc Drawing 5962 - 860320xxx

Requirements

General

The microcircuits are in accordance with the applicable document and as specified herein.

Design and Construction

Terminal Connections

Depending on the package, the terminal connections shall be as shown in Figure 2 and Figure 3.

Lead Material and Finish

Lead material and finish shall be any option of MIL-STD-1835.

Package

The macrocircuits are packages in hermetically sealed ceramic packages which are conform to case outlines of MIL-STD-1835 (when defined):

- 114-pin SQ.PGA UP PAE Outline
- 132-pin Ceramic Quad Flat Pack CQFP

The precise case outlines are described on Figure 23 and Figure 24.

Electrical Characteristics

Table 2. Absolute Maximum Ratings

| Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{CC}	Supply Voltage		-0.3	+7.0	V
V_I	Input Voltage		-0.5	+7.0	V
P_{dmax}	Max Power Dissipation	T_{case} = -55°C		2.0	W
		T_{case} = +125°C		1.9	W
T_{case}	Operating Temperature	M Suffix	-55	+125	°C
		V Suffix	-40	+85	°C
T_{stg}	Storage Temperature		-55	+150	°C
T_{leads}	Lead Temperature	Max 5 Sec. Soldering		+270	°C

Table 3. Recommended Condition of Use

Unless otherwise stated, all voltages are referenced to the reference terminal (see Table 1).

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		4.5	5.5	V
V_{IL}	Low Level Input Voltage		-0.3	0.5	V
V_{IH}	High Level Input Voltage		2.4	5.25	V
T_{case}	Operating Temperature		-55	+125	°C
R_L	Value of Output Load Resistance		(1)		Ω
C_L	Output Loading Capacitance			(1)	pF
$t_r(c)$–$t_f(c)$	Clock Rise Time (See Figure 5)	68020-16		5	ns
		68020-20		5	
		68020-25		4	
f_c	Clock Frequency (See Figure 5)	68020-16	8	16.67	MHz
		68020-20	12.5	20	
		68020-25	12.5	25	
t_{cyc}	Cycle Time (see Figure 5)	68020-16	60	125	ns
		68020-20	50	80	
		68020-25	40	80	
$t_W(CL)$	Clock Pulse Width Low (See Figure 5)	68020-16	24	95	ns
		68020-20	20	54	
		68020-25	19	61	
$t_W(CH)$	Clock Pulse Width High (See Figure 5)	68020-16	24	95	ns
		68020-20	20	50	
		68020-25	19	61	

Note: 1. Load network number 1 to 4 as specified (Table 7) gives the maximum loading of the relevant output.

This device contains protective circuitry against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Figure 5. Clock Input Timing Diagram
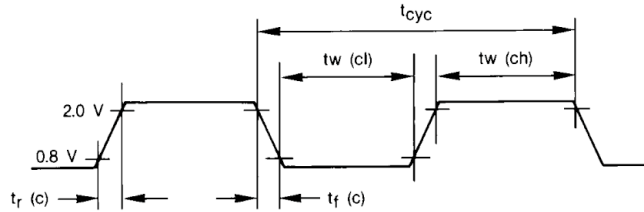
Note: Timing measurements are referenced to and from a low voltage of 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8V and 2.0V.

Table 4. Thermal Characteristics at 25°C

Package	Symbol	Parameter	Value	Unit
PGA 114	θ_{JA}	Thermal Resistance - Ceramic Junction to Ambient	26	°C/W
	θ_{JC}	Thermal Resistance - Ceramic Junction to Case	5	°C/W
CQFP 132	θ_{JA}	Thermal Resistance - Ceramic Junction to Ambient	34	°C/W
	θ_{JC}	Thermal Resistance - Ceramic Junction to Case	2	°C/W

Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \qquad (1)$$

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \cdot V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K + (T_J + 273) \qquad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273) + \theta_{JA} \cdot P_D^2 \qquad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation **(3)** by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations **(1)** and **(2)** iterativley for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation:

$$\theta_{JA} = \theta_{JC} = \theta_{CA} \qquad\qquad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (**1**) will result in a lower semiconductor junction temperature.

Mechanical and Environment

The microcircuits shall meet all mechanical environmental requirements of MIL-STD-883 for class B devices.

Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum:

- ATMEL Logo
- Manufacturer's Part Number
- Class B Identification
- Date-code of Inspection Lot
- ESD Identifier if Available
- Country of Manufacturing

Quality Conformance Inspection

DESC/MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspections are performed on a periodical basis.

Electrical Characteristics

General Requirements

All static and dynamic electrical characteristics specified and the relevant measurement conditions are given below.

(last issue on request to our marketing services).

Table 5: Static electrical characteristics for all electrical variants.

Table 6: Dynamic electrical characteristics for 68020-16 (16.67 MHz), 68020-20 (20 MHz) and 68020-25 (25 MHz).

For static characteristics, test methods refer to "Test Conditions Specific to the Device" on page 14 hereafter of this specification (Table 7).

For dynamic characteristics (Table 6), test methods refer to IEC 748-2 method, where existing.

Indication of "min." or "max." in the column "test temperature" means minimum or maximum operating temperature.

Table 5. Static Characteristics. $V_{CC} = 5.0V_{DC} \pm 10\%$; GND = $0V_{DC}$; T_c = -55/+125°C or -40/+85°C (Figure 4 to Figure 8)

Symbol	Parameter	Condition	Min	Max	Units
I_{CC}	Maximum Supply Current	V_{CC} = 5.5V T_{case} -55°C to +25°C		333	mA
I_{CC}	Maximum Supply Current	V_{CC} = 5.5V T_{case} = 125°C		207	mA
V_{IH}	High Level Input Voltage	V_O = 0.5V or 2.5 V_{CC} = 4.5V to 5.5V	2.0	V_{CC}	V
V_{IL}	Low Level Input Voltage	V_O = 0.5V or 2.4V V_{CC} = 4.5V to 5.5V	-0.5	0.8	V
V_{OH}	High Level Output Voltage All Outputs	I_{OH} = 400 µA	2.4		V
V_{OL}	Low Level Output Voltage Outputs A0-A31, FC0-FC2, D0-D31, SIZ0-SIZ1, $\overline{BG}$	I_{OL} = 3.2 mA Load Circuit as Figure 8 R = 1.22 kΩ		0.5	V
V_{OL}	Low Level Output Voltage Outputs $\overline{AS}$, $\overline{DS}$, $\overline{RMC}$, R/$\overline{W}$, $\overline{DBEN}$, $\overline{IPEND}$	I_{OL} = 5.3 mA Load Circuit as Figure 8 R = 740Ω		0.5	V
V_{OL}	Low Level Output Voltage Outputs $\overline{ECS}$, $\overline{OCS}$	I_{OL} = 2.0 mA Load Circuit as Figure 8 R = 2 kΩ		0.5	V
V_{OL}	Low Level Output Voltage Outputs $\overline{HALT}$, $\overline{RESET}$	I_{OL} = 10.7 mA Load Circuit as Figure 6 and Figure 7		0.5	V
| I_{IN} |	Input Leakage Current (High and Low State)	-0.5V ≤ V_{IN} ≤ V_{CC} (Max)		2.5	µA
| I_{OHZ} |	High level leakage current at three-state outputs Outputs A0-A31, $\overline{AS}$, $\overline{DBEN}$, $\overline{DS}$, D0-D31, R/$\overline{W}$, FC0-FC2, $\overline{RMC}$, SIZ0-SIZ1	V_{OH} = 2.4V		2.5	µA
| I_{OLZ} |	Low Level Leakage Current at Three-state Outputs Outputs A0-A31, $\overline{AS}$, $\overline{DBEN}$, $\overline{DS}$, D0-D31 R/$\overline{W}$, FC0-FC2, $\overline{RMC}$, SIZ0-SIZ1	V_{OL} = 0.5V		2.5	µA
I_{OS}	Output Short-circuit Current (Any Output)	V_{CC} = 5.5V V_O = 0V (Pulsed. Duration 1 ms Duty Cycle 10:1)		200	mA

Dynamic (Switching) Characteristics

The limits and values given in this section apply over the full case temperature range -55°C to +125°C and V_{CC} in the range 4.5V to 5.5V V_{IL} = 0.5V and V_{IH} = 2.4V (See also note 12 and 13). The INTERVAL numbers refer to the timing diagrams. See Figure 5, Figure 9 and Figure 12.

Table 6. Dynamic Electrical Characteristics

Symbol	Parameter	Interval Number	68020-16		68020-20		68020-25		Unit	Notes
			Min	Max	Min	Max	Min	Max		
t_{CPW}	Clock Pulse Width	2 , 3	24	95	20	54	19	61	ns	
t_{CHAV}	Clock High to Address/FC/Size/$\overline{RMC}$ Valid	6	0	30	0	25	0	25	ns	
t_{CHEV}	Clock High to $\overline{ECS}$, $\overline{OCS}$ Asserted	6A	0	20	0	15	0	12	ns	
t_{CHAZX}	Clock High to Address/Data/FC/$\overline{RMC}$/Size High Impedance	7	0	60	0	50	0	40	ns	(11)
t_{CHAZn}	Clock High to Address/FC/Size/$\overline{RMC}$ Invalid	8	0		0		0		ns	
t_{CLSA}	Clock Low to $\overline{AS}$, $\overline{DS}$ Asserted	9	3	30	3	25	3	18	ns	
t_{STSA}	$\overline{AS}$ to $\overline{DS}$ Assertion (Read)(Skew)	9A	-15	15	-10	10	-10	10	ns	(1)
t_{ECSA}	$\overline{ECS}$ Width Asserted	10	20		15		15		ns	
t_{OCSA}	$\overline{OCS}$ Width Asserted	10A	20		15		15		ns	
t_{EOCSN}	$\overline{ECS}$, $\overline{OCS}$ Width Negated	10B	15		10		5		ns	(11)
t_{AVSA}	Address/FC/Size/$\overline{RMC}$ Valid to $\overline{AS}$ Asserted (and $\overline{DS}$ Asserted, Read)	11	15		10		6		ns	(6)
t_{CLSN}	Clock Low to $\overline{AS}$, $\overline{DS}$ Negated	12	0	30	0	25	0	15	ns	
t_{CLEN}	Clock Low to $\overline{ECS}$/$\overline{OCS}$ Negated	12A	0	30	0	25	0	15	ns	
t_{SNAI}	$\overline{AS}$, $\overline{DS}$ Negated to Address/FC/Size/$\overline{RMC}$ Invalid	13	15		10		10		ns	
t_{SWA}	$\overline{AS}$ (and $\overline{DS}$, Read) Width Asserted	14	100		85		70		ns	
t_{SWAW}	$\overline{DS}$ Width Asserted, Write	14A	40		38		30		ns	
t_{SN}	$\overline{AS}$, $\overline{DS}$ Width Negated	15	40		38		30		ns	(11)
t_{SNSA}	$\overline{DS}$ Negated to $\overline{AS}$ Asserted	15A	35		30		25		ns	(8)
t_{CSZ}	Clock High to $\overline{AS}$/$\overline{DS}$/R/$\overline{W}$/$\overline{DBEN}$ High Impedance	16		60		50		40	ns	(11)
t_{SNRN}	$\overline{AS}$, $\overline{DS}$ Negated to R/$\overline{W}$ High	17	15		10		10		ns	(6)
t_{CHRH}	Clock High to R/$\overline{W}$ High	18	0	30	0	25	0	20	ns	
t_{CHRL}	Clock High to R/$\overline{W}$ Low	20	0	30	0	25	0	20	ns	
t_{RAAA}	R/$\overline{W}$ High to $\overline{AS}$ Asserted	21	15		10		5		ns	(6)
t_{RASA}	R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write)	22	75		60		50		ns	(6)
t_{CHDO}	Clock High to Data Out Valid	23		30		25		25	ns	
t_{SNDI}	AS, DS Negated to Data Out Valid	25	15		10		5		ns	(6)
t_{DNDBN}	$\overline{DS}$ Negated to $\overline{DBEN}$ Negated (Write)	25A	15		10		5		ns	(9)

Table 6. Dynamic Electrical Characteristics (Continued)

Symbol	Parameter	Interval Number	68020-16 Min	68020-16 Max	68020-20 Min	68020-20 Max	68020-25 Min	68020-25 Max	Unit	Notes
t_{DVSA}	Data Out Valid to $\overline{DS}$ Asserted (Write) 26	26	15		10		5		ns	(6)
t_{DICL}	Data in Valid to Clock Low (Data Setup)	27	5		5		5		ns	
t_{BELCL}	Late $\overline{BERR}/\overline{HALT}$ Asserted to Clock Low Setup Time	27A	20		15		10		ns	
t_{SNDN}	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DSACKx}/\overline{BERR}/\overline{HALT}/\overline{AVEC}$ Negated	28	0	80	0	65	0	50	ns	
t_{SNDI}	$\overline{DS}$ Negated to Data On Invalid (Data in Hold Time)	29	0		0		0		ns	(6)
t_{SNDIZ}	$\overline{DS}$ Negated to Data in High Impedance	29A		60		50		40	ns	
t_{DADI}	$\overline{DSACKx}$ Asserted to Data In Valid	31		50		43		32		(2)(11)
t_{DADV}	$\overline{DSACK}$ Asserted to $\overline{DSACKx}$ Valid ($\overline{DSACK}$ Asserted Skew)	31A		15		10		10	ns	(3)(11)
t_{HRrf}	$\overline{RESET}$ Input Transition Time	32		1.5		1.5		1.5	Clks	
t_{CLBA}	Clock Low to $\overline{BG}$ Asserted	33	0	30	0	25	0	20	ns	
t_{CLBN}	Clock Low to $\overline{BG}$ Negated	34	0	30	0	25	0	20	ns	
t_{BRAGA}	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted (RMC Not Asserted)	35	1.5	3.5	1.5	3.5	1.5	3.5	Clks	(11)
t_{GAGN}	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	37	1.5	3.5	1.5	3.5	1.5	3.5	Clks	(11)
t_{GABRN}	$\overline{BGACK}$ Asserted to $\overline{BR}$ Negated	37A	0	1.5	0	1.5	0	1.5	Clks	(11)
t_{GN}	$\overline{BG}$ Width Negated	39	90		75		60		ns	(11)
t_{GA}	$\overline{BG}$ Width Asserted	39A	90		75		60		ns	
t_{CHDAR}	Clock High to $\overline{DBEN}$ Asserted (Read)	40	0	30	0	25	0	20	ns	
t_{CLDNR}	Clock Low to $\overline{DBEN}$ Negated (Read)	41	0	30	0	25	0	20	ns	
t_{CLDAW}	Clock Low to $\overline{DBEN}$ Negated (Read)	42	0	30	0	25	0	20	ns	
t_{CHDNW}	Clock High to $\overline{DBEN}$ Asserted (Read)	43	0	30	0	25	0	20	ns	
t_{RADA}	R/W Low to $\overline{DBEN}$ Asserted (Write)	44	15		10		10		ns	(6)

t_{DA}	$\overline{DBEN}$ Width Asserted
	   READ
	   WRITE
		45		60
				120
						50
						100
								40
								80
									ns
									ns
										(5)
										(5)

t_{RWA}	R/$\overline{W}$ Width Asserted (Write or Read)	46	150		125		100		ns	
t_{AIST}	Asynchronous Input Setup Time	47A	5		5		5		ns	(11)
t_{AIHT}	Asynchronous Input Hold Time	47B	15		15		10		ns	(11)
t_{DABA}	$\overline{DSACKx}$ Asserted to $\overline{BERR}/\overline{HALT}$ Asserted	48		30		20		18	ns	(4)(11)
t_{DOCH}	Data Out Hold from Clock High	53	0		0		0		ns	
t_{BNHN}	$\overline{BERR}$ Negated to $\overline{HALT}$ Negated (Rerun)			0		0		0	ns	

Table 6. Dynamic Electrical Characteristics (Continued)

Symbol	Parameter	Interval Number	68020-16		68020-20		68020-25		Unit	Notes
			Min	Max	Min	Max	Min	Max		
f	Frequency of Operation		8.0	16.67	12.5	20.0	12.5	25	MHz	
t_{RADC}	R/W Asserted to Data Bus Impedance Change	55	30		25		20			(11)
t_{HRPW}	$\overline{RESET}$ Pulse Width (Reset Instruction)	56	512		512		512		Clks	(11)
t_{BNHN}	$\overline{BERR}$ Negated to $\overline{HALT}$ Negated (Rerun)	57	0		0		0		ns	(11)
t_{GANBD}	$\overline{BGACK}$ Negated to Bus Driven	58	1		1		1		Clks	(10)(11)
t_{GNBD}	$\overline{BG}$ Negated to Bus Driven	59	1		1		1		Clks	(10)(11)

Notes:
1. This number can be reduced to 5 nanoseconds if the strobes have equal loads.
2. If the asynchronous setup time (= 47) requirements are satisfied, the DSACKx low to data setup time (= 31) and $\overline{DSACKx}$ low to $\overline{BERR}$ low setup time (= 48) can be ignored. The data must only satisfy the data in to clock low setup time (= 27) for the following clock cycle, $\overline{BERR}$ must only satisfy the late $\overline{BERR}$ low to clock setup time (= 27) for the following clock cycle.
3. This parameter specifies the maximum allowable skew between $\overline{DSACK0}$ to $\overline{DSACK1}$ asserted or $\overline{DSACK1}$ to $\overline{DSACK0}$ asserted pattern = 47 must be met by $\overline{DSACK0}$ and $\overline{DSACK1}$.
4. In the absence of $\overline{DSACKx}$, $\overline{BERR}$ is an asynchronous input using the asynchronous input setup time (= 47).
5. $\overline{DBEN}$ may stay asserted on consecutive write cycles.
6. Actual value depends on the clock input waveform.
7. This pattern indicates the minimum high time for $\overline{ECS}$ and $\overline{OCS}$ in the event of an internal cache hit followed immediately by a cache miss or operand cycle.
8. This specification guarantees operations with the 68881 co-processor, and defines a minimum time for DS negated to AS asserted (= 13A). Without this parameter, incorrect interpretation of = 9A and = 15 would indicate that the 68020 does not meet 68881 requirements.
9. This pattern allows the systems designer to guarantee data hold times on the output side of data buffers that have output enable signals generated with $\overline{DBEN}$.
10. Guarantees that an alternate bus master has stopped driving the bus when the 68020 regains control of the bus after an arbitration sequence.
11. Cannot be tested. Provided for system design purposes only.
12. T_{case} = -55°C and +130°C in a Power off condition under Thermal soak for 4 minutes or until thermal equilibrium. Electrical parameters are tested "instant on" 100 m sec. after power is applied.
13. All outputs unload except for load capacitance. Clock = fmax,
LOW: $\overline{HALT}$, $\overline{RESET}$
HIGH: $\overline{DSACK0}$, $\overline{DSACK1}$, $\overline{CDIS}$, $\overline{IPL0-IPL2}$, $\overline{DBEN}$, $\overline{AVEC}$, $\overline{BERR}$.

Test Conditions Specific to the Device

Loading Network

The applicable loading network shall be defined in column "Test conditions" of Table 6, referring to the loading network number as shown in Figure 6, Figure 7, Figure 8 below.
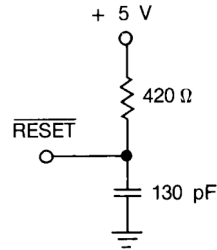
Figure 6. RESET Test Loads
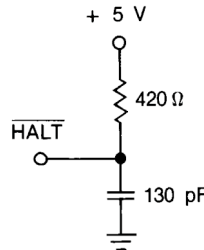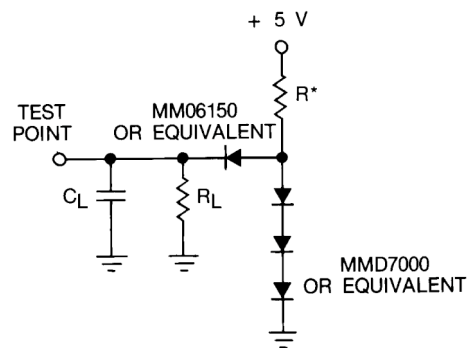

Figure 7. HALT Test Load


Figure 8. Test Load

Table 7. Load Network

Load NBR	Figure	R	R_L	C_L	Output Application
1	7	2 k	6.0 k	50 pF	$\overline{OCS}$, $\overline{ECS}$
2	7	1.22 k	6.0 k	130 pF	A0-A31, D0-D31, $\overline{BG}$, FC0-FC2, SIZ0-SIZ1
3	7	0.74 k	6.0 k	130 pF	$\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, $\overline{RMC}$, $\overline{DBEN}$, $\overline{IPEND}$

Note: 1. Equivalent loading may be simulated by the tester.

Time Definitions

The times specified in Table 6 as dynamic characteristics are defined in Figure 9 below, by a reference number given the column "interval N°" of the tables together with the relevant figure number.

Figure 9. Read Cycle Timing Diagram
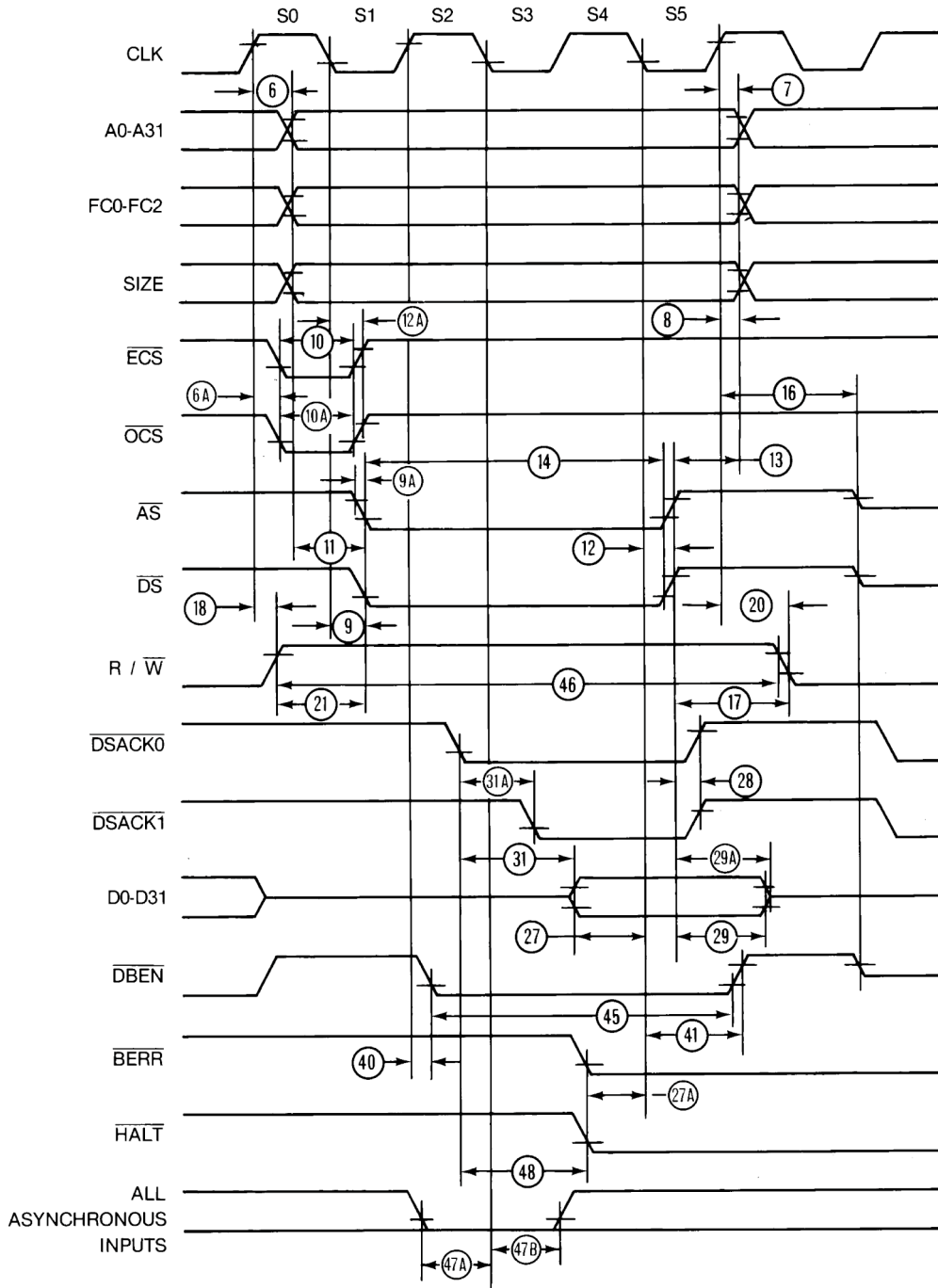
Note: Timing measurements are referenced to and from a low voltage of 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8V and 2.0V.

Figure 10. Write Cycle Timing Diagram (Continued)
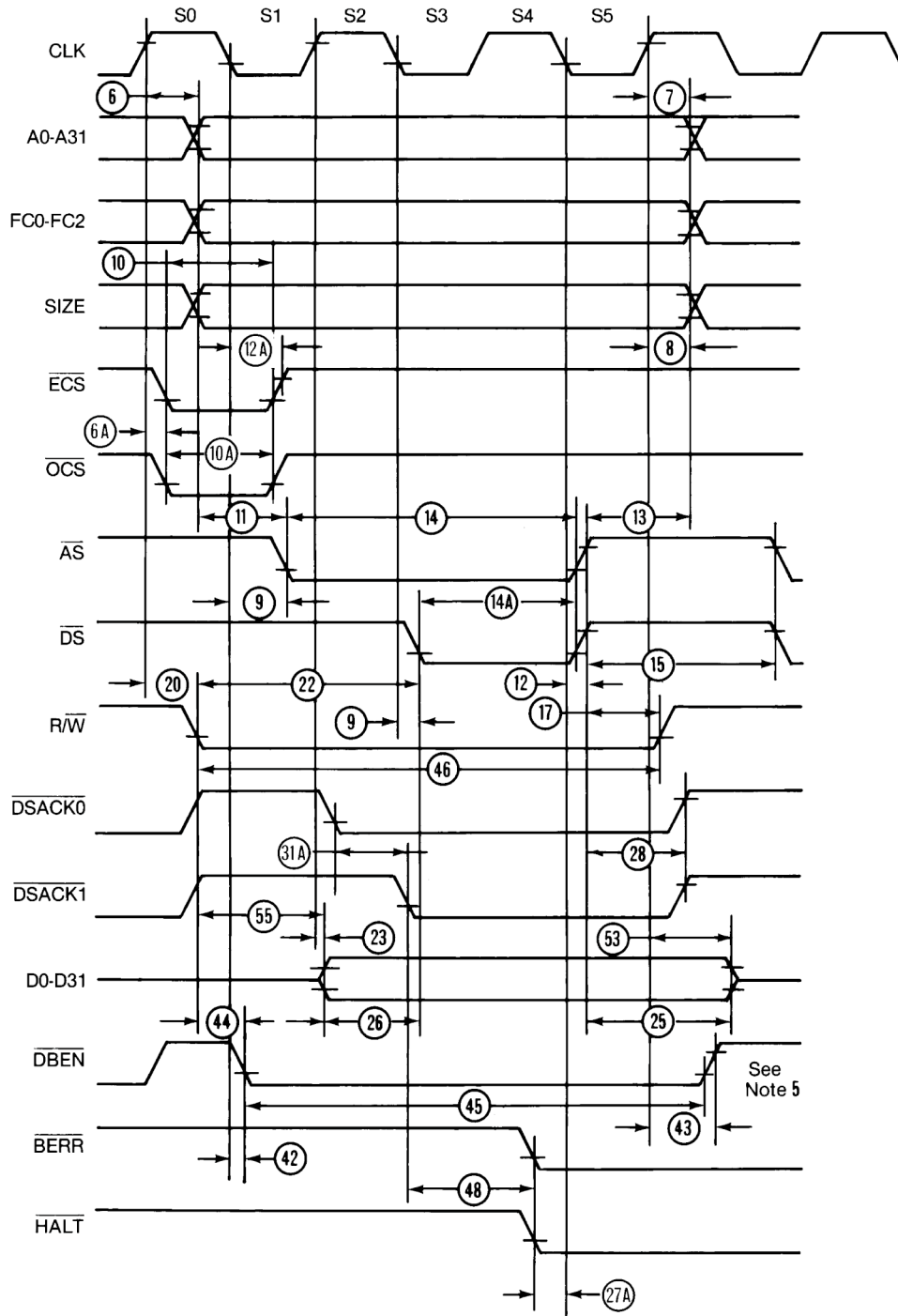
Note: Timing measurements are referenced to and from a low voltage of 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing thorough this range should start outside and pass through the range such that the rise or fall will be linear between 0.8V and 2.0V.

Figure 11. Bus Arbitration Timing Diagram
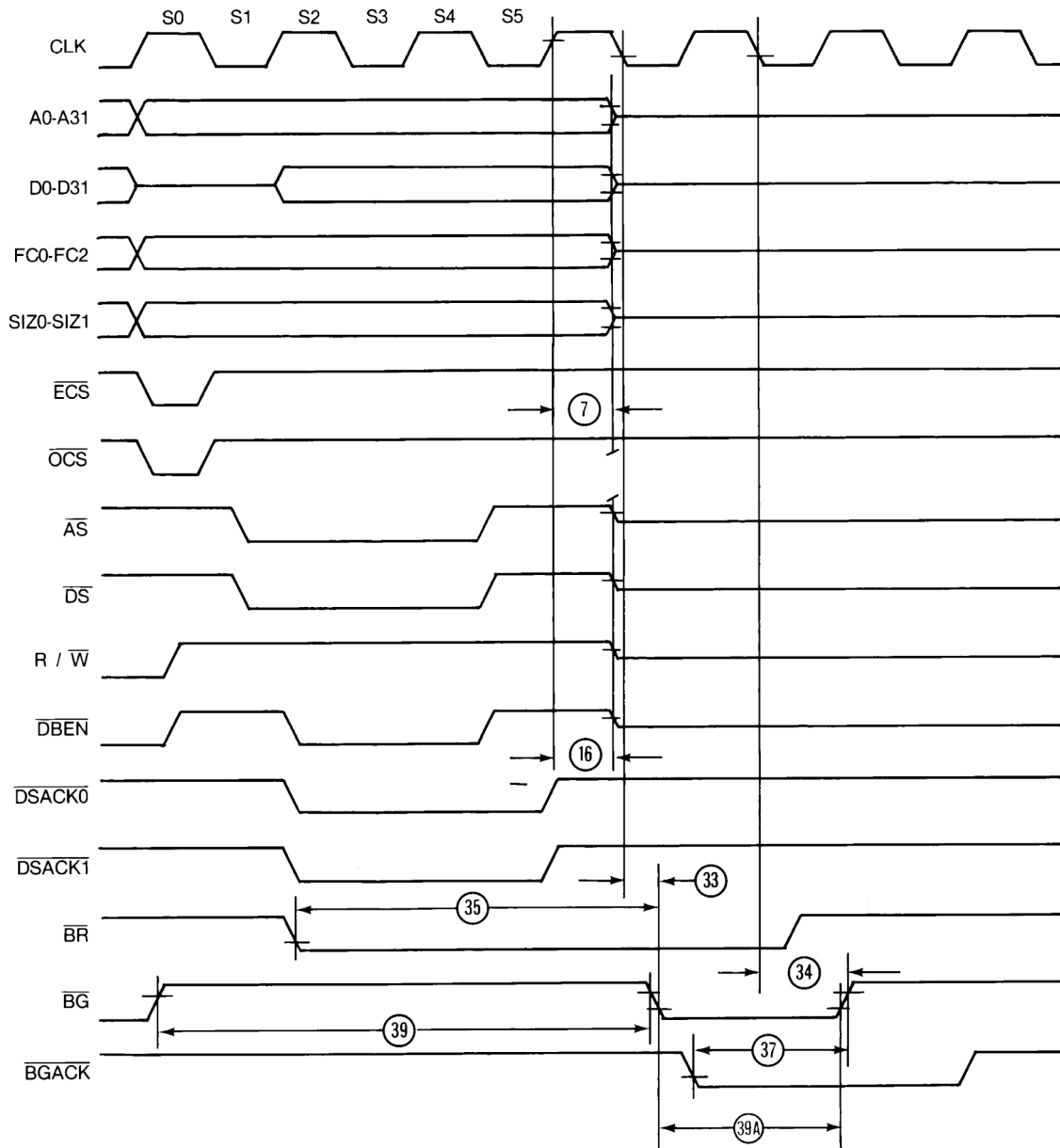
Note: Timing measurements are referenced to and from a low voltage of 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing thorough this range should start outside and pass through the range such that the rise or fall will be linear between 0.8V and 2.0V.

Input and Output Signals for Dynamic Measurements

AC Electrical Specifications Definitions

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the TS68020 clock input and, possibly, relative to one or more other signals.

The measurement of the AC specifications is defined by the waveforms in Figure 12. In order to test the parameters guaranteed by Atmel, inputs must be driven to the voltage levels specified in Figure 12. Outputs of the TS68020 are specified with minimum and/or maximum limits, as appropriate, and are measured as shown. Inputs to the TS68020 are specified with minimum and, as appropriate, maximum setup and hold times, and are measurement as shown. Finally, the measurements for signal-to-signal specification are also shown.

Note that the testing levels used to verify conformance of the TS68020 to the AC specifications does not affect the guaranteed DC operation of the device as specified in the DC electrical characteristics.

Figure 12. Drive Levels and Test Points for AC Specification
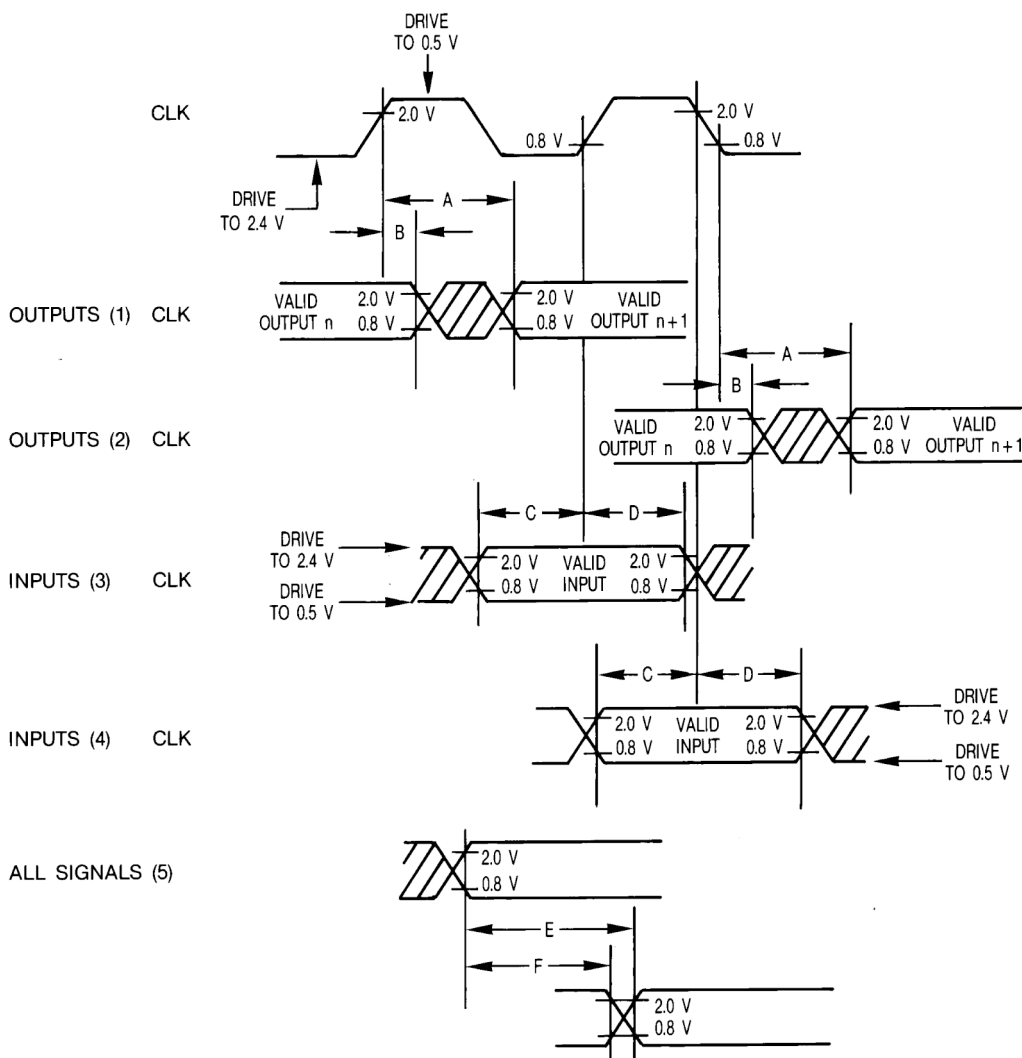
Legend:

A) Maximum Output Delay Specification

B) Minimum Output Hold Time

C) Minimum Input Setup Time Specification

D) Minimum Input Hold Time Specification

E) Signal Valid to Signal Valid Specification (Maximum or Minimum)

F) Signal Valid to Signal Invalid Specification (Maximum or Minimum)

Notes: 1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
      2. This out put timing is applicable to all parameters specified relative to the falling edge of the clock.
      3. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
      4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
      5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

Additional Information

Additional information shall not be for any inspection purposes.

Power Consideration

See Table 4.

Capacitance (Not for Inspection Purposes

Symbol	Parameter	Test Conditions	Min	Unit
C_{in}	Input Capacitance	$V_{in} = 0V$ $T_{amb} = 25°C$ $f = 1$ MHz	20	pF

Capacitance Derating Curves

Figure 13 to Figure 18 inclusive show the typical derating conditions which apply. The capacitance includes any stray capacitance. The graphs may not be linear outside the range shown.

Figure 13. Address Capacitance Derating Curve
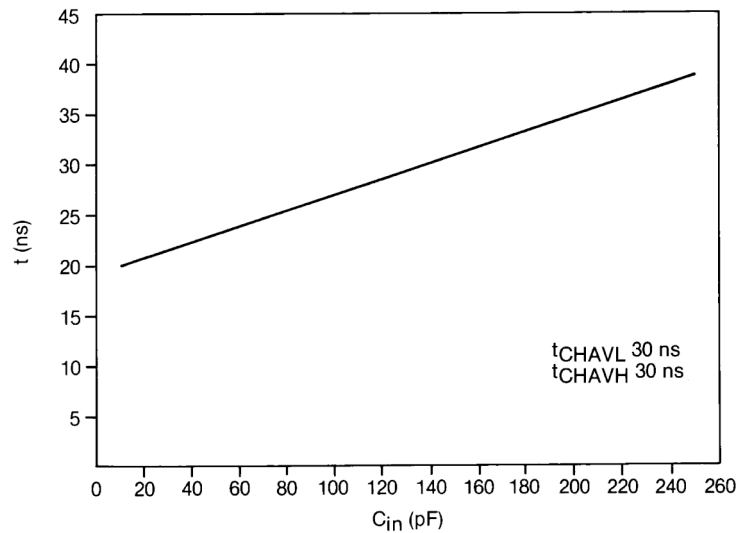
Figure 14. ECS and OCS Capacitance Derating Curve
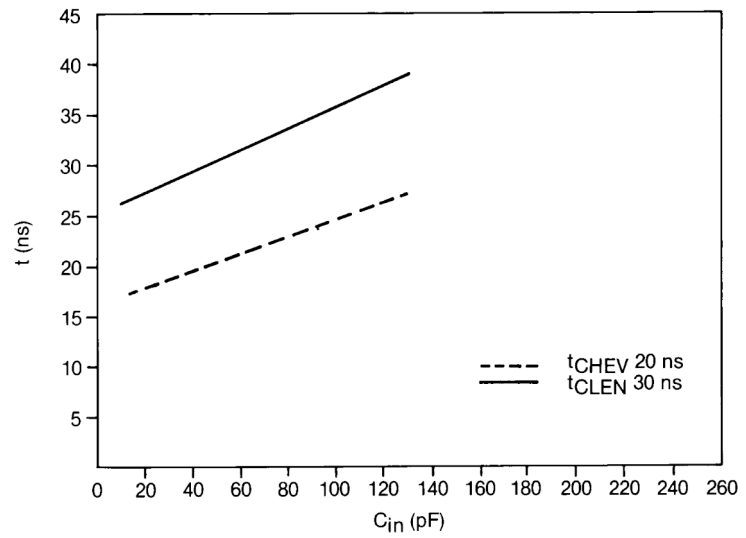
Figure 15. R/W, FC, SIZ0-SIZ1, and RMC Capacitance Derating Curve
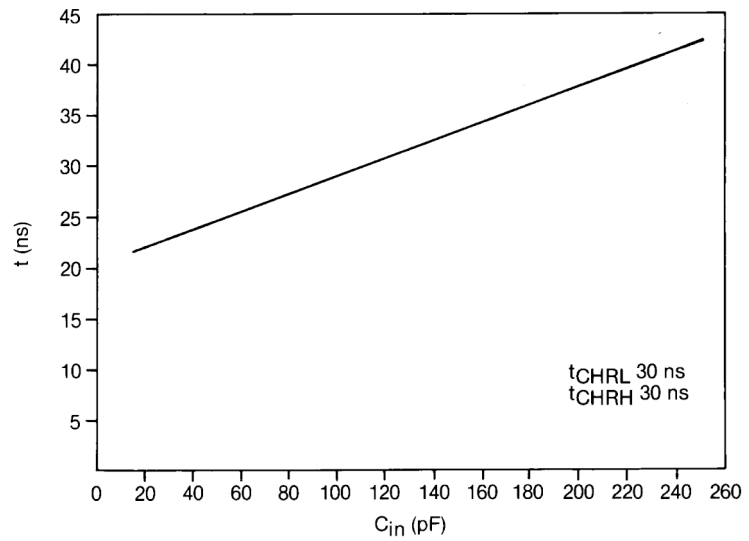
Figure 16. DS, AS, IPEND, and BG Capacitance Derating Curve
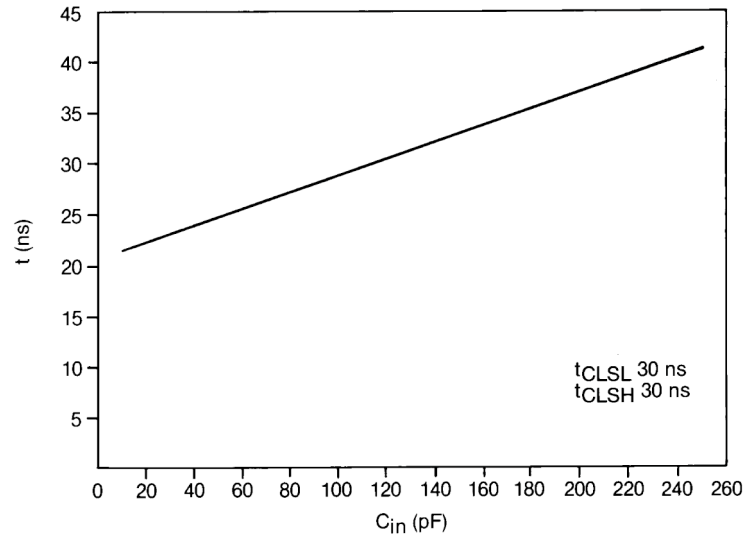
Figure 17. DBEN Capacitance Derating Curve
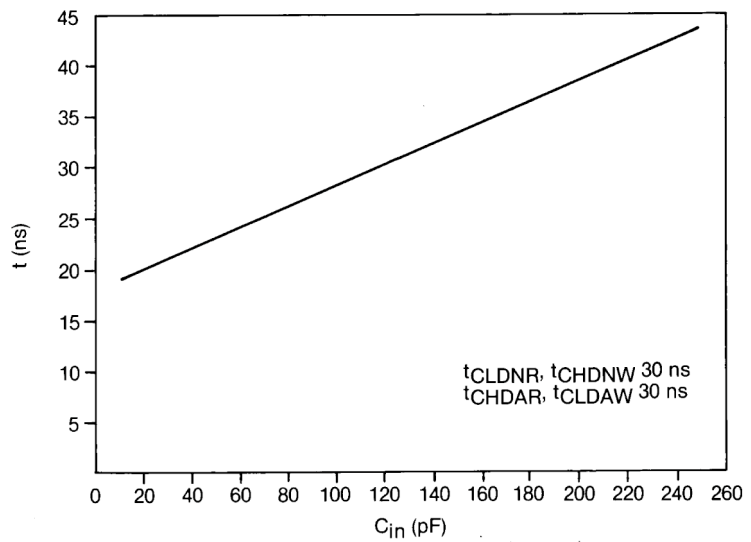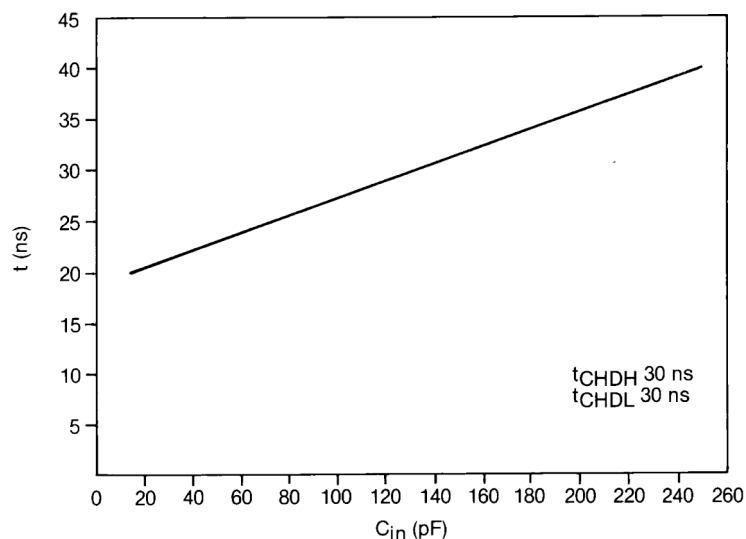
Figure 18. Data Capacitance Derating Curve

Functional Description

Description of Registers

As shown in the programming models (Figure 19 and Figure 20) the TS68020 has sixteen 32-bit general-purpose registers, a 32-bit program counter, two 32-bit supervisor stack pointers, a 16-bit status register, a 32-bit vector base register, two 3-bit alternate function code registers, and two 32-bit cache handling (address and control) registers. Registers D0-D7 are used as data registers for bit and bit field (1- to 32-bit), byte (8-bit), long word (32-bit), and quad word (64-bit) operations. Registers A0-A6 and the user, interrupt, and master stack pointers are address registers that may be used as software stack pointers or base address registers. In addition, the address registers may be used for word and long word operations. All of the 16 (D0-D7, A0-A7) registers may be used as index registers.

The status register (Figure 21) contains the interrupt priority mask (three bits) as well as the condition codes: extend (X), negated (N), zero (Z), overflow (V), and carry (C). Additional control bits indicate that the processor is in the trace mode (T1 or T0), supervisor/user state (S), and master/interrupt state (M).

All microprocessors of the TS68000 Family support instruction tracing (via the T0 status bit in the TS68020) where each instruction executed is followed by a trap to a user-defined trace routine. The TS68020 adds the capability to trace only the change of flow instructions (branch, jump, subroutine call and return, etc.) using the T1 status bit. These features are important for software program development and debug.

The vector base register is used to determine the runtime location of the exception vector table in memory, hence it supports multiple vector tables so each process or task can properly manage exceptions independent of each other.

The TS68000 Family processors distinguish address spaces as supervisor / used and program/data. These four combinations are specified by the function code pins (FC0/FC1/FC2) during bus cycles, indication the particular address space. Using the function codes, the memory sub-system can distinguish between authorized access (supervisor mode is privileged access) and unauthorized access (user mode may not have access to supervisor program or data areas). To support the full privileges of the supervisor, the alternate function code registers allow the supervisor to specify an access to user program or data areas by preloading the SFC/DFC registers appropriately.

The cache registers (control — CACR, address — CAAR) allow software manipulation of the on-chip instruction cache. Control and status accesses to the instruction cache are provided by the cache control register (CACR), while the cache address register (CAAR) holds the address for those cache control functions that require an address.
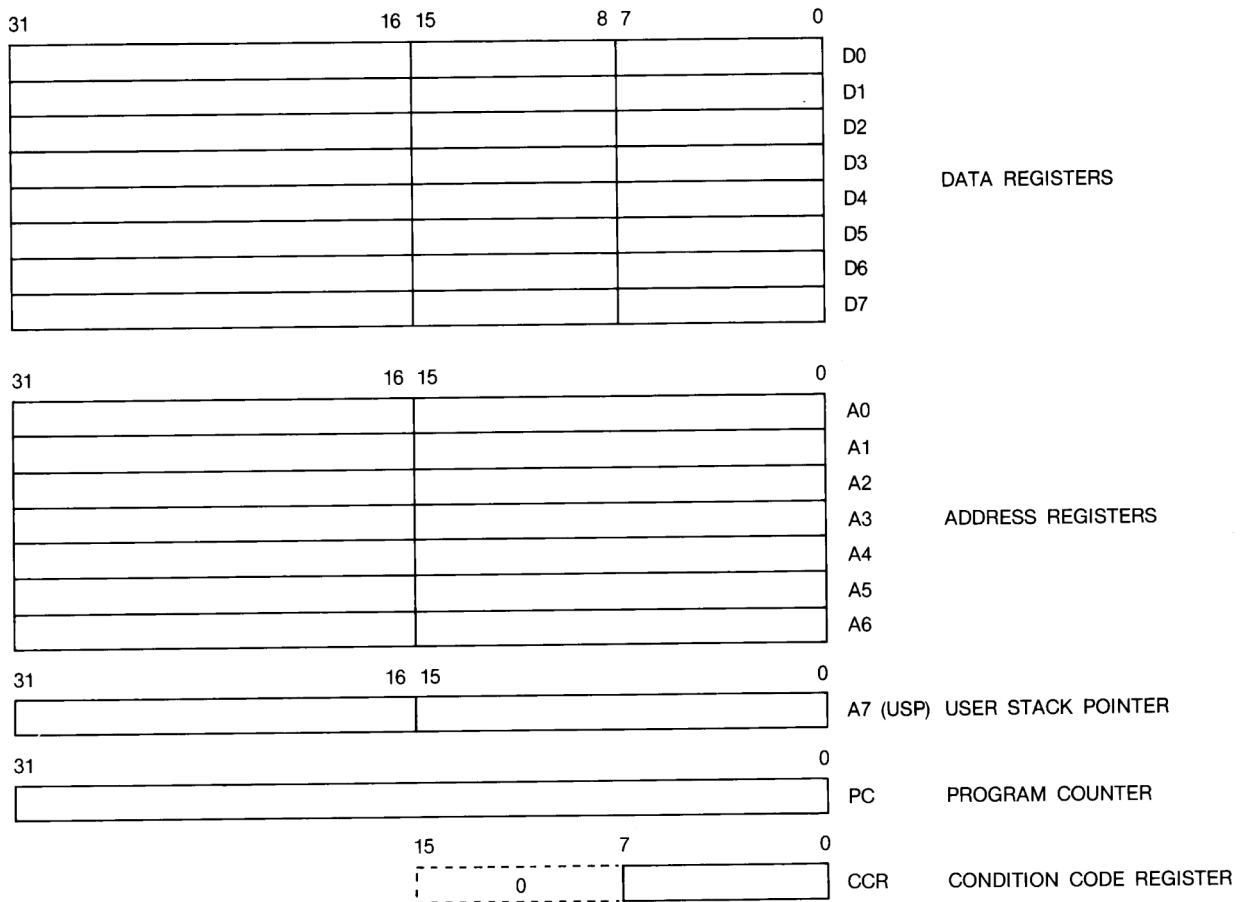
Figure 19. User Programming Model

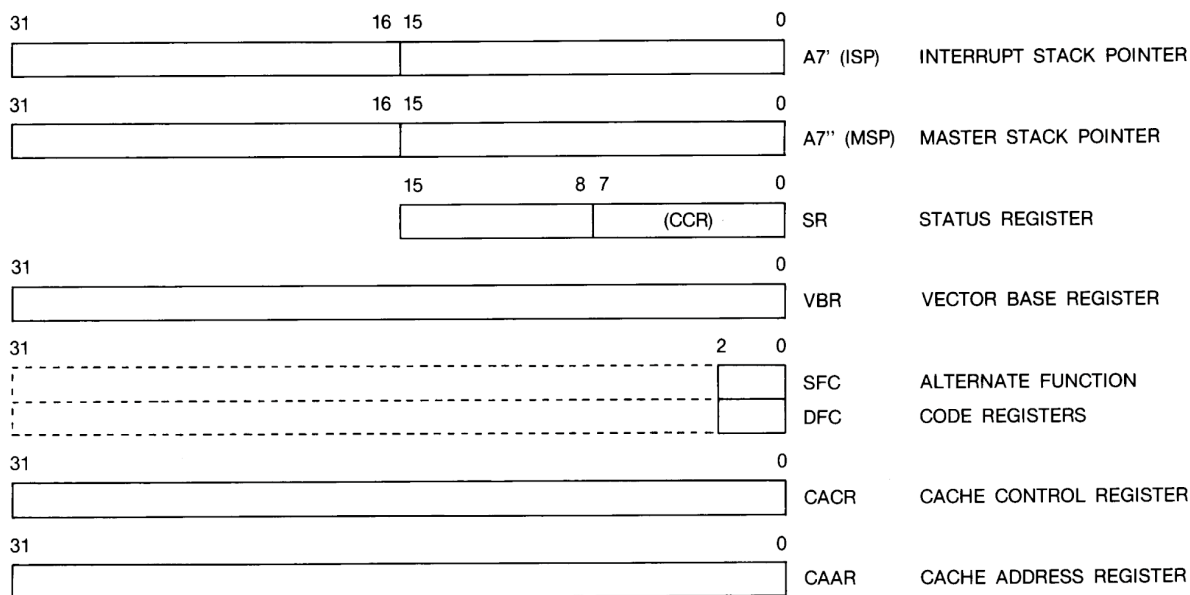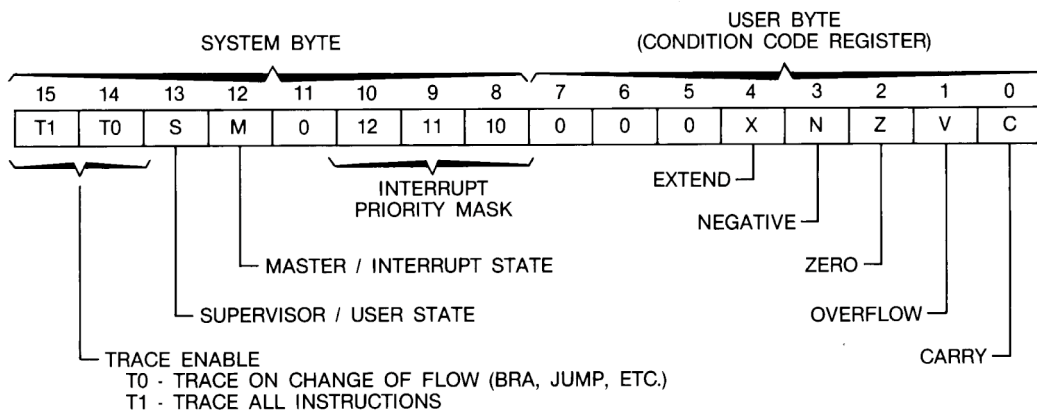**Figure 20.** Supervisor Programming Model Supplement

Figure 21. Status Register

Data Types and Addressing Modes

Seven basic types are supported. These data types are:

* Bits
* Bits Flieds (String of consecutive bits, 1-32 bits long)
* BCD Digits (Packed: 2 digits/byte, Unpacked: 1 digit/byte)
* Byte Integers (8-bit)
* Word Integers (16-bit)
* Long Word Integers (32-bit)
* Quad Word Integers (64-bit)

In addition, operations on other data types, such as memory addresses, status word data, etc...., are provided in the instruction set. The co-processor mechanism allows direct support of floating-point data type with the TS68881 and TS68882 floating-point co-processors, as well as specialized user-defined data types and functions.