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Features

- **26-42 MIPS Integer Performance**
- **3.5-5.6 MFLOPS Floating-Point-Performance**
- **IEEE 754-Compatible FPU**
- **Independent Instruction and Data MMUs**
- **4K bytes Physical Instruction Cache and 4K bytes Physical Data Cache Accessed Simultaneously**
- **32-bit, Nonmultiplexed External Address and Data Buses with Synchronous Interface**
- **User-Object-Code Compatibility with All Earlier TS68000 Microprocessors**
- **Multimaster/Multiprocessor Support via Bus Snooping**
- **Concurrent Integer Unit, FPU, MMU, Bus Controller, and Bus Snooper Maximize Throughput**
- **4G bytes Direct Addressing Range**
- **Software Support Including Optimizing C Compiler and UNIX® System V Port**
- **IEEE P 1149-1 Test Mode (JTAG)**
- **f = 25 MHz, 33 MHz; V_{CC} = 5V ± 5%; P_D = 7W**
- **The Use of the TS88915T Clock Driver is Suggested**

Third-Generation 32-bit Microprocessor

TS68040

Description

The TS68040 is Atmel's third generation of 68000-compatible, high-performance, 32-bit microprocessors. The TS68040 is a virtual memory microprocessor employing multiple, concurrent execution units and a highly integrated architecture to provide very high performance in a monolithic HCMOS device. On a single chip, the TS68040 integrates a 68030-compatible integer unit, an IEEE 754-compatible floating-point unit (FPU), and fully independent instruction and data demand-paged memory management units (MMUs), including 4K bytes independent instruction and data caches. A high degree of instruction execution parallelism is achieved through the use of multiple independent execution pipelines, multiple internal buses, and a full internal Harvard architecture, including separate physical caches for both instruction and data accesses. The TS68040 also directly supports cache coherency in multimaster applications with dedicated on-chip bus snooping logic.

The TS68040 is user-object-code compatible with previous members of the TS68000 Family and is specifically optimized to reduce the execution time of compiler-generated code. The 68040 HCMOS technology, provides an ideal balance between speed, power, and physical device size.

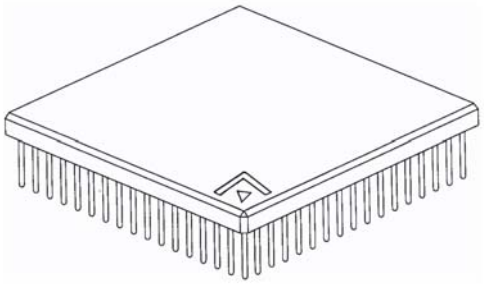
Figure 1 is a simplified block diagram of the TS68040. Instruction execution is pipelined in both the integer unit and FPU. Independent data and instruction MMUs control the main caches and the address translation caches (ATCs). The ATCs speed up logical-to-physical address translations by storing recently used translations. The bus snooper circuit ensures cache coherency in multimaster and multiprocessing applications.

Screening

- MIL-STD-883
- DESC. Drawing 5962-93143
- Atmel Standards

Rev. 2116A–HIREL–09/02

R suffix
PGA 179
Ceramic Pin Grid Array
Cavity Down



F suffix
CQFP 196
Gullwing Shape Lead
Ceramic Quad Fla Pack

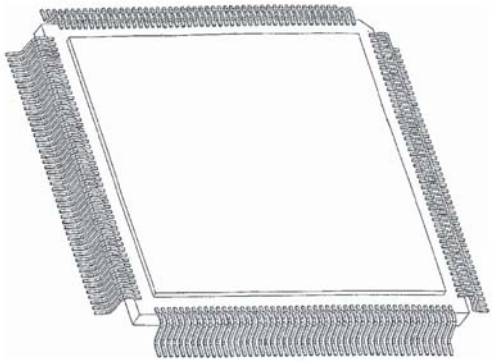
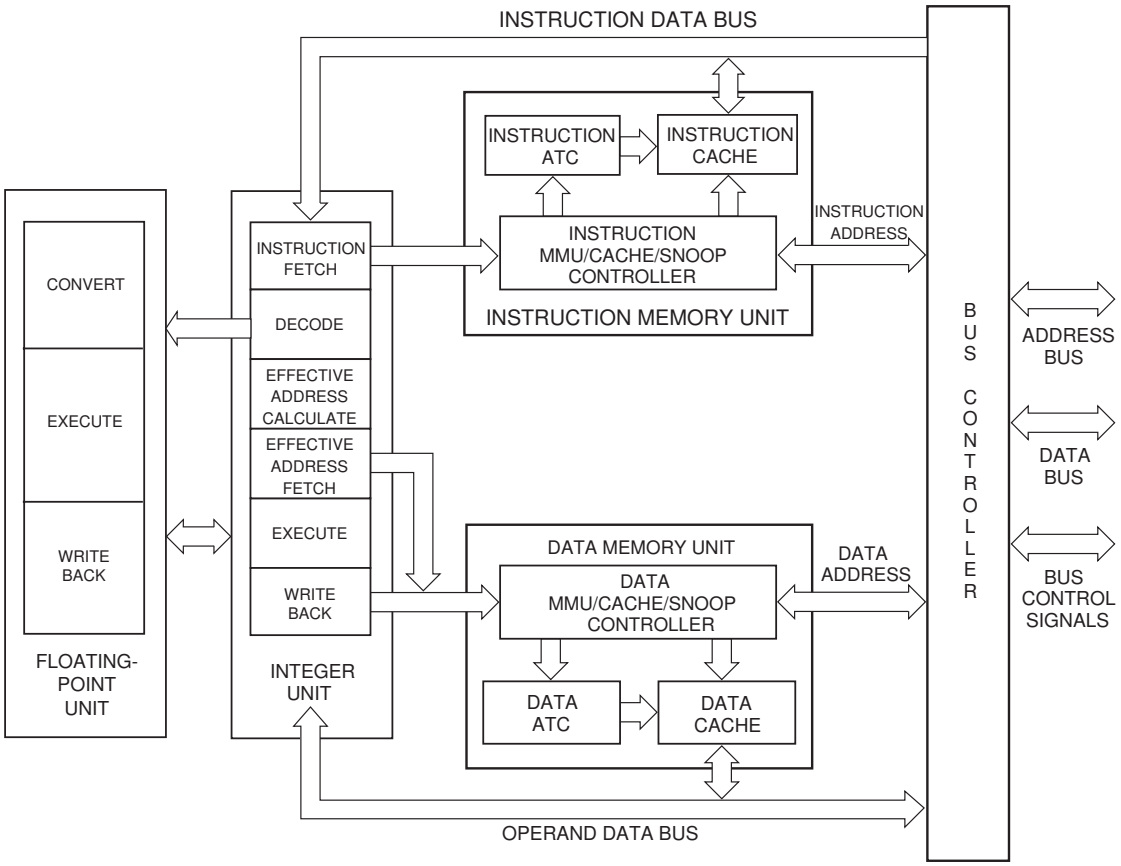


Figure 1. Block Diagram



Introduction

The TS68040 is an enhanced, 32-bit, HCMOS microprocessor that combines the integer unit processing capabilities of the TS68030 microprocessor with independent 4K bytes data and instruction caches and an on-chip FPU. The TS68040 maintains the 32-bit registers available with the entire TS68000 Family as well as the 32-bit address and data paths, rich instruction set, and versatile addressing modes. Instruction execution proceeds in parallel with accesses to the internal caches, MMU operations, and bus controller activity. Additionally, the integer unit is optimized for high-level language environments.

The TS68040 FPU is user-object-code compatible with the TS68882 floating-point coprocessor and conforms to the ANSI/IEEE Standard 754 for binary floating-point arithmetic. The FPU has been optimized to execute the most commonly used subset of the TS68882 instruction set, and includes additional instruction formats for single and double-precision rounding of results. Floating-point instructions in the FPU execute concurrently with integer instructions in the integer unit.

The MMUs support multiprocessing, virtual memory systems by translating logical addresses to physical addresses using translation tables stored in memory. The MMUs store recently used address mappings in two separate ATCs-on-chip. When an ATC contains the physical address for a bus cycle requested by the processor, a translation table search is avoided and the physical address is supplied immediately, incurring no delay for address translation. Each MMU has two transparent translation registers available that define a one-to-one mapping for address space segments ranging in size from 16M bytes to 4G bytes each.

Each MMU provides read-only and supervisor-only protections on a page basis. Also, processes can be given isolated address spaces by assigning each a unique table structure and updating the root pointer upon a task swap. Isolated address spaces protect the integrity of independent processes.

The instruction and data caches operate independently from the rest of the machine, storing information for fast access by the execution units. Each cache resides on its own internal address bus and internal data bus, allowing simultaneous access to both. The data cache provides write through or copyback write modes that can be configured on a page-by-page basis.

The TS68040 bus controller supports a high-speed, non multiplexed, synchronous external bus interface, which allows the following transfer sizes: byte, word (2 bytes), long word (4 bytes), and line (16 bytes). Line accesses are performed using burst transfers for both reads and writes to provide high data transfer rates.

Pin Assignments

PGA 179

Figure 2. Bottom View

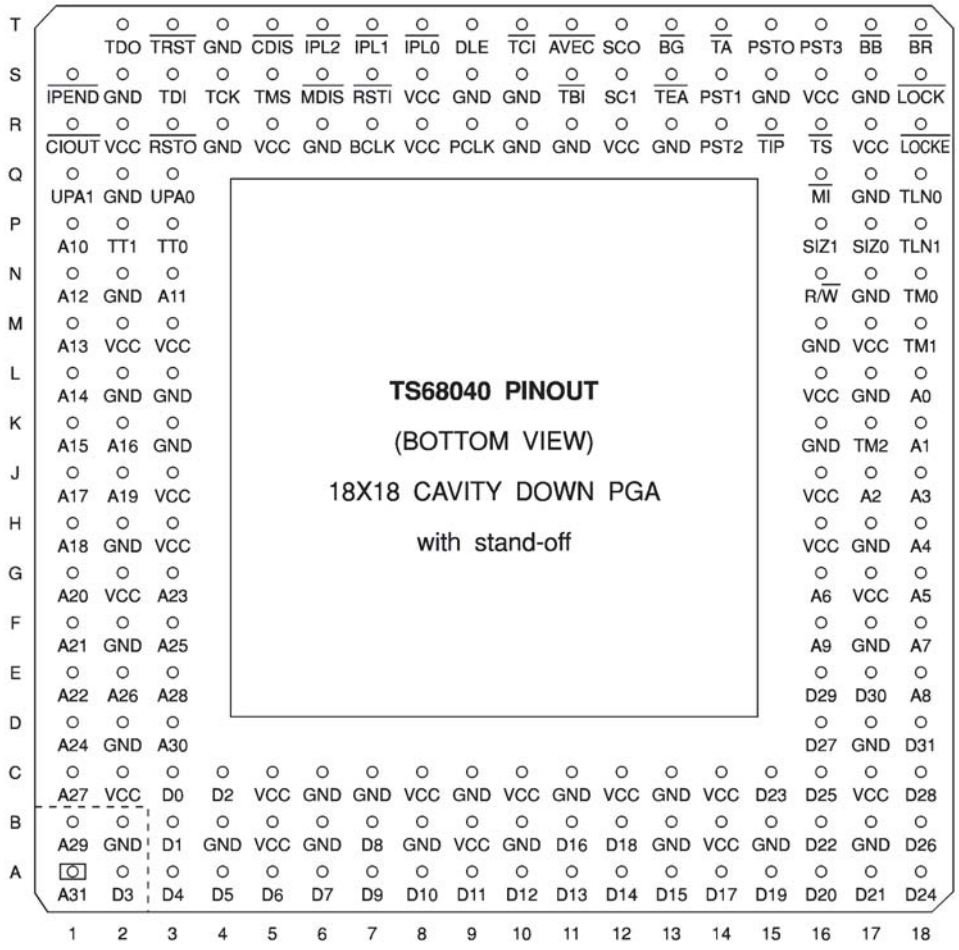


Table 1. Power Supply Affectation to PGA Body

	GND	V_{CC}
PLL		S8
Internal Logic	C6, C7, C9, C11,C13, K3, K16, L3, M16, R4, R11, R13, S10, T4, S9, R6, R10	C5, C8, C10, C12, C14, H3, H16, J3, J16, L16, M3, R5, R12, R8
Output Drivers	B2, B4, B6, B8, B10, B13, B15, B17, D2, D17, F2, F17, H2, H17, L2, L17, N2, N17, Q2, Q17, S2, S15, S17	B5, B9, B14, C2, C17, G2, G17, M2, M17, R2, R17, S16

CQFP 196

Figure 3. Pin Assignments

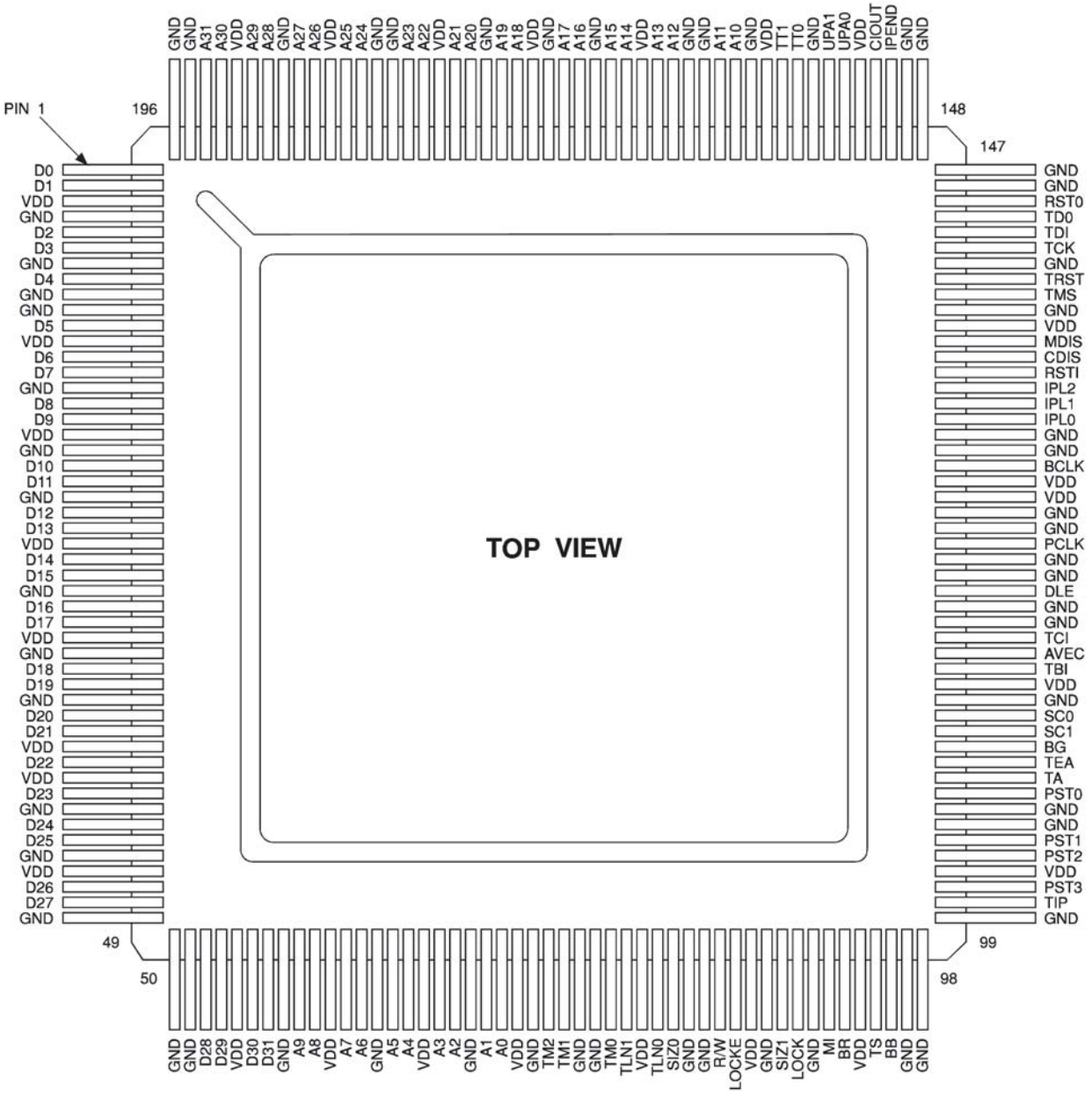


Table 2. Power Supply Affectation to CQFP Body

	GND	**V_{CC}**
PLL		127
Internal Logic	4, 9, 10, 19, 32, 45, 73, 88, 113, 119, 121, 122, 124, 125, 129, 130, 141, 159, 172	3, 18, 31, 40, 46, 60, 72, 87, 114, 126, 137, 158, 173, 186
Output Drivers	7, 15, 22, 28, 35, 42, 49, 50, 51, 57, 63, 69, 76, 77, 83, 84, 91, 97, 98, 99, 105, 106, 146, 147, 148, 149, 155, 162, 163, 169, 176, 182, 183, 189, 195, 196	12, 25, 38, 54, 66, 80, 94, 102, 152, 166, 179, 192

Signal Description

Figure 4 and Table 3 describe the signals on the TS68040 and indicate signal functions. The test signals, $\overline{TRST}$, TMS, TCK, TDI, and TDO, comply with subset P-1149.1 of the IEEE testability bus standard.

Figure 4. Functional Signal Groups

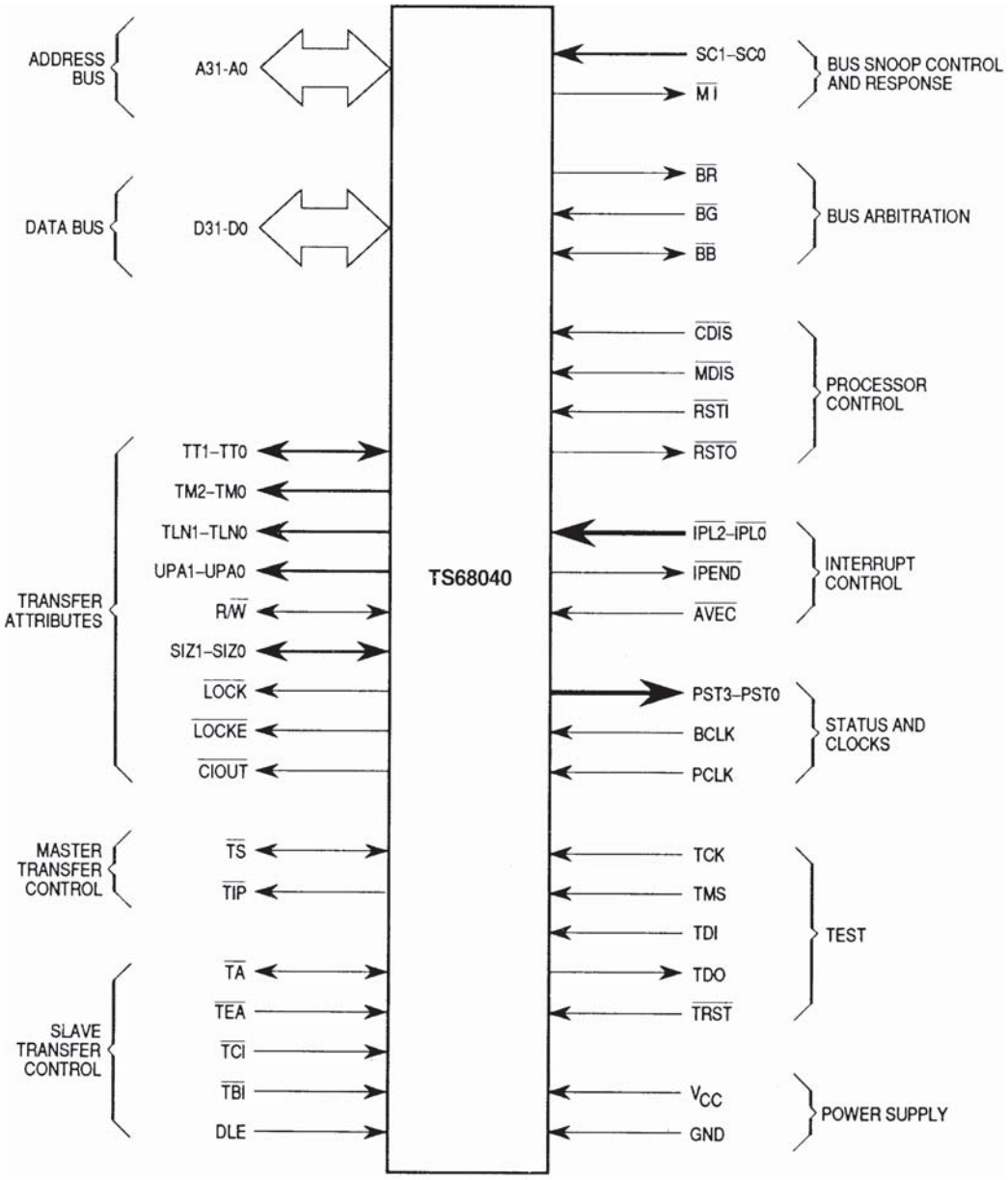


Table 3. Signal Index

Signal Name	Mnemonic	Function
Address Bus	A31-A0	32-bit address bus used to address any of 4G bytes
Data Bus	D31-D0	32-bit data bus used to transfer up to 32 bits of data per bus transfer
Transfer Type	TT1, TT0	Indicates the general transfer type: normal, MOVE 16, alternate logical function code, and acknowledge
Transfer Modifier	TM2, TM0	Indicates supplemental information about the access
Transfer Line Number	TLN1, TLN0	Indicates which cache line in a set is being pushed or loaded by the current line transfer
User Programmable Attributes	UPA1, UPA0	User-defined signals, controlled by the corresponding user attribute bits from the address translation entry
Read Write	R/$\overline{W}$	Identifies the transfer as a read or write
Transfer Size	SIZ1, SIZ0	Indicates the data transfer size. These signals, together with A0 and A1, define the active sections of the data bus
Bus Lock	$\overline{LOCK}$	Indicates a bus transfer is part of a read-modify-write operation, and that the sequence of transfers should not be interrupted
Bus Lock End	$\overline{LOCKE}$	Indicates the current transfer is the last in a locked sequence of transfer
Cache Inhibit Out	$\overline{CIOUT}$	Indicates the processor will not cache the current bus transfer
Transfer Start	$\overline{TS}$	Indicates the beginning of a bus transfer
Transfer in Progress	$\overline{TIP}$	Asserted for the duration of a bus transfer
Transfer Acknowledge	$\overline{TA}$	Asserted to acknowledge a bus transfer
Transfer Error Acknowledge	$\overline{TEA}$	Indicates an error condition exists for a bus transfer
Transfer Cache Inhibit	$\overline{TCI}$	Indicates the current bus transfer should not be cached
Transfer Burst Inhibit	$\overline{TBI}$	Indicates the slave cannot handle a line burst access
Data Latch Enable	DLE	Alternate clock input used to latch input data when the processor is operating in DLE mode
Snoop Control	SC1, SC0	Indicates the snooping operation required during an alternate master access
Memory Inhibit	$\overline{MI}$	Inhibits memory devices from responding to an alternate master access during snooping operations
Bus Request	$\overline{BR}$	Asserted by the processor to request bus mastership
Bus Grant	$\overline{BG}$	Asserted by an arbiter to grant bus mastership to the processor
Bus Busy	$\overline{BB}$	Asserted by the current bus master to indicate it has assumed ownership of the bus
Cache Disable	$\overline{CDIS}$	Dynamically disables the internal caches to assist emulator support
MMU Disable	$\overline{MDIS}$	Disables the translation mechanism of the MMUs
Reset In	$\overline{RSTI}$	Processor reset
Reset Out	$\overline{RSTO}$	Asserted during execution of the RESET instruction to reset external devices
Interrupt Priority Level	$\overline{IPL2}$-$\overline{IPL0}$	Provides an encoded interrupt level to the processor
Interrupt Pending	$\overline{IPEND}$	Indicates an interrupt is pending
Autovector	$\overline{AVEC}$	Used during an interrupt acknowledge transfer to request internal generation of the vector number
Processor Status	PST3-PST0	Indicates internal processor status

Table 3. Signal Index (Continued)

Signal Name	Mnemonic	Function
Bus Clock	BCLK	Clock input used to derive all bus signal timing
Processor Clock	PCLK	Clock input used for internal logic timing. The PCLK frequency is exactly 2X the BCLK frequency
Test Clock	TCK	Clock signal for the IEEE P1149.1 test access port (TAP)
Test Mode Select	TMS	Selects the principle operations of the test-support circuitry
Test Data Input	TDI	Serial data input for the TAP
Test Data Output	TDO	Serial data output for the TAP
Test Reset	$\overline{TRST}$	Provides an asynchronous reset of the TAP controller
Power Supply	V_{CC}	Power supply
Ground	GND	Ground connection

Scope

This drawing describes the specific requirements for the microprocessor TS68040 - 25 MHz and 33 MHz, in compliance with MIL-STD-883 class B or Atmel standard screening.

Applicable Documents

MIL-STD-883

1. MIL-STD-883: test methods and procedures for electronics.
2. MIL-I-38535: general specifications for microcircuits.
3. DESC 5962-93143.

Requirements

General

The microcircuits are in accordance with the applicable document and as specified herein.

Design and Construction

Terminal Connections

See Figure 2 and Figure 3.

Lead Material and Finish

Lead material and finish shall be as specified in MIL-STD-883 (see enclosed “MIL-STD-883 C and Internal Standard” on page 46).

Package

The macro circuits are packaged in hermetically sealed ceramic packages which conform to case outlines of MIL-STD-1835-or as follow:

- CMGA 10-179-PAK pin grid array, but see “179 pins – PGA” on page 43.
- Similar to CQCC1-F196C-U6 ceramic uniform lead chip carrier package with ceramic nonconductive tie-bar but use Atmel’s internal drawing, see “196 pins – Tie Bar CQFP Cavity Up (on request)” on page 44.
- Gullwing shape CQFP see “196 pins – Gullwing CQFP cavity up” on page 45.

The precise case outlines are described at the end of the specification (See “Package Mechanical Data” on page 43.) and into MIL-STD-1835.

Electrical Characteristics

Absolute Maximum Ratings Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	Supply Voltage Range		-0.3	7.0	V
V_I	Input Voltage Range		-0.3	7.0	V
P_D	Power Dissipation	Large buffers enabled		7.7	W
		Small buffers enabled		6.3	W
T_C	Operating Temperature		-55	T_J	°C
T_{stg}	Storage Temperature Range		-65	+150	°C
T_J	Junction Temperature(1)			+125	°C
T_{lead}	Lead Temperature	Max.10 sec soldering		+300	°C

Note: 1. This device is not tested at TC = +125°C. Testing is performed by setting the junction temperature Tj = +125°C and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

Table 5. Recommended Conditions of Use
Unless otherwise stated, all voltages are referenced to the reference terminal

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage Range		+4.75		+5.25	V
V_{IL}	Logic Low Level Input Voltage Range		GND - 0.3		0.8	V
V_{IH}	Logic High Level Input Voltage Range		+2.0		V_{CC} + 0.3	V
V_{OH}	High Level Output Voltage		2.4			V
V_{OL}	Low Level Output Voltage				0.5	V
f_c	Clock Frequency	-25 MHz Version		25		MHz
		-33 MHz Version		33		MHz
T_C	Case Operating Temperature Range(1)		-55		T_{Jmax}	°C
T_J	Maximum Operating Junction Temperature				+125	°C

Note: 1. This device is not tested at TC = +125°C. Testing is performed by setting the junction temperature T_J = +125°C and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

Thermal Considerations

General Thermal Considerations

This section is only given as user information.

As microprocessors are becoming more complex and requiring more power, the need to efficiently cool the device becomes increasingly more important. In the past, the TS68000 Family, has been able to provide a 0-70°C ambient temperature part for speeds less than 40 MHz. However, the TS68040, which has a 50 MHz arithmetic logic unit (ALU) speed, is specified with a maximum power dissipation for a particular mode, a maximum junction temperature, and a thermal resistance from the die junction to the case. This provides a more accurate method of evaluating the environment, taking into consideration both the air-flow and ambient temperature available. This also allows a user the information to design a cooling method which meets both thermal performance requirements and constraints of the board environment.

This section discusses the device characteristics for thermal management, several methods of thermal management, and an example of one method of cooling the TS68040.

Thermal Device Characteristics

The TS68040 presents some inherent characteristics which should be considered when evaluating a method of cooling the device. The following paragraphs discuss these die/package and power considerations.

Die and Package

The TS68040 is being placed in a cavity-down alumina-ceramic 179-pin PGA that has a specified thermal resistance from junction to case of 1°C/W. This package differs from previous TS68000 Family PGA packages which were cavity up. This cavity-down design allows the die to be attached to the top surface of the package, which increases the ability of the part to dissipate heat through the package surface or an attached heat sink. The maximum perimeter that the TS68040 allows for a heat sink on its surface without interfering with the capacitor pads is 1.48" x 1.48". The specific dimensions and design of the particular heat sink will need to be determined by the system designer considering both thermal performance requirements and size requirements.

Power Considerations

The TS68040 has a maximum power rating, which varies depending on the operating frequency and the output buffer mode combination being used. The large buffer output mode dissipates more power than the small, and the higher frequencies of operation dissipate more power than the lower frequencies. The following paragraphs discuss trade-offs in using the different output buffer modes, calculation of specific maximum power dissipation for different modes, and the relationship of thermal resistances and temperatures.

Output Buffer Mode

The 68040 is capable of resetting to enable for a combination of either large buffers or small buffers on the outputs of the miscellaneous control signals, data bus, and address bus/transfer attribute pins. The large buffers offer quicker output times, which allow for an easier logic design. However, they do so by driving about 11 times as much current as the small buffers (refer to TS68040 Electrical specifications for current output). The designer should consider whether the quicker timings present enough advantage to justify the additional consideration to the individual signal terminations, the die power consumption, and the required cooling for the device. Since the TS68040 can be powered-up in one of eight output buffer modes upon reset, the actual maximum power consumption for TS68040 rated at a particular maximum operating frequency is dependent upon the power up mode. Therefore, the TS68040 is rated at a maximum power dissipation for either the large buffers or small buffers at a particular frequency (refer to TS68040 Electrical specifications). This allows the possibility of some of the thermal management to be controlled upon reset. The following equation provides a rough method to calculate the maximum power consumption for a chosen output buffer mode:

$$P_D = P_{DSB} + (P_{DLB} - P_{DSB}) \cdot (PINS_{LB}/PINS_{CLB}) \qquad (1)$$

where:

P_D = Max. power dissipation for output buffer mode selected

P_{DSB} = Max. power dissipation for small buffer mode (all outputs)

P_{DLB} = Max. power dissipation for large buffer mode (all outputs)

$PINS_{LB}$ = Number of pins large buffer mode

$PINS_{CLB}$ = Number of pins capable of the large buffer mode

Table 6 shows the simplified relationship on the maximum power dissipation for eight possible configurations of output buffer modes.

Table 6. Maximum Power Dissipation for Output Buffer Mode Configurations

Output Configuration			Maximum Power Dissipation
Data Bus	**Address Bus and Transfer Attrib.**	**Misc. Control Signals**	**PD**
Small Buffer	Small Buffer	Small Buffer	P_{DSB}
Small Buffer	Small Buffer	Large Buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) \cdot 13\%$
Small Buffer	Large Buffer	Small Buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) \cdot 52\%$
Small Buffer	Large Buffer	Large Buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) \cdot 65\%$
Large Buffer	Small Buffer	Small Buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) \cdot 35\%$
Large Buffer	Small Buffer	Large Buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) \cdot 48\%$
Large Buffer	Large Buffer	Small Buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) \cdot 87\%$
Large Buffer	Large Buffer	Large Buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) \cdot 100\%$

To calculate the specific power dissipation of a specific design, the termination method of each signal must be considered. For example, a signal output that is not connected would not dissipate any additional power if it were configured in the large buffer rather than the small buffer mode.

Relationships Between Thermal Resistances and Temperatures

Since the maximum operating junction temperature has been specified to be 125°C. The maximum case temperature, TC, in °C can be obtained from:

$$T_C = T_J - P_D \cdot \Phi_{JC} \quad (2)$$

where:

T_C = Maximum case temperature

T_J = Maximum junction temperature

P_D = Maximum power dissipation of the device

Φ_{JC} = Thermal resistance between the junction of the die and the case

In general, the ambient temperature, T_A, in °C is a function of the following formula:

$$T_A = T_J - P_D \cdot \Phi_{JC} - P_D \cdot \Phi_{CA} \quad (3)$$

Where the thermal resistance from case to ambient, Φ_{CA}, is the only user-dependent parameter once a buffer output configuration has been determined. As seen from equation (3), reducing the case to ambient thermal resistance increases the maximum operating ambient temperature. Therefore, by utilizing such methods as heat sinks and ambient air cooling to minimize the Φ_{CA}, a higher ambient operating temperature and/or a lower junction temperature can be achieved.

However, an easier approach to thermal evaluation uses the following formulas:

$$T_A = T_J - P_D \cdot \Phi_{JA} \quad (4)$$

or alternatively,

$$T_J = T_A - P_D \cdot \Phi_{JA} \quad (5)$$

where:

Φ_{JA} = thermal resistance from the junction to the ambient ($\Phi_{JC} + \Phi_{CA}$).

This total thermal resistance of a package, Φ_{JA}, is a combination of its two components, Φ_{JC} and Φ_{CA}. These components represent the barrier to heat flow from the semiconductor junction to the package (case) surface (Φ_{JC}) and from the case to the outside ambient (Φ_{JC}). Although Φ_{JC} is device related and cannot be influenced by the user, Φ_{CA} is user dependent. Thus, good thermal management by the user can significantly reduce Φ_{CA} achieving either a lower semiconductor junction temperature or a higher ambient operating temperature.

Thermal Management Techniques

To attain a reasonable maximum ambient operating temperature, a user must reduce the barrier to heat flow from the semiconductor junction to the outside ambient (Φ_{JA}). The only way to accomplish this is to significantly reduce Φ_{CA} by applying such thermal management techniques as heat sinks and ambient air cooling.

The following paragraphs discuss some results of a thermal study of the TS68040 device without using any thermal management techniques; using only air-flow cooling, using only a heat sink, and using heat sink combined with air-flow cooling.

Thermal Characteristics in Still Air

A sample size of three TS68040 packages was tested in free-air cooling with no heat sink. Measurements showed that the average Φ_{JA} was 22.8°C/W with a standard deviation of 0.44°C/W. The test was performed with 3W of power being dissipated from within the package. The test determined that Φ_{JA} will decrease slightly for the increasing power dissipation range possible. Therefore, since the variance in Φ_{JA} within the possible power dissipation range is negligible, it can be assumed for calculation purposes that Φ_{JA} is valid at all power levels. Using the formulas introduced previously, Table 7 shows the results of a maximum power dissipation of 3 and 5W with no heat sink or air-flow (refer to Table 6 to calculate other power dissipation values).

Table 7. Thermal Parameters With No Heat Sink or Air-flow

Defined Parameters			Measured	Calculated		
P_D	T_J	Φ_{JC}	Φ_{JA}	$\Phi_{CA} = \Phi_{JA} - \Phi_{JC}$	$T_C = T_J - P_D * \Phi_{JC}$	$T_A = T_J - P_D * \Phi_{JA}$
3 Watts	125°C	1°C/W	21.8°C/W	20.8°C/W	122°C	59.6°C
5 Watts	125°C	1°C/W	21.8°C/W	20.8°C/W	120°C	16°C

As seen by looking at the ambient temperature results, most users will want to implement some type of thermal management to obtain a more reasonable maximum ambient temperature.

Thermal Characteristics in Forced Air

A sample size of three TS68040 packages was tested in forced air cooling in a wind tunnel with no heat sink. This test was performed with 3W of power being dissipated from within the package. As previously mentioned, since the variance in ΦJA within the possible power range is negligible, it can be assumed for calculation purposes that Φ_{JA} is constant at all power levels. Using the previous formulas, Table 8 shows the results of the maximum power dissipation at 3 and 5W with air-flow and no heat sink (refer to Table 6 to calculate other power dissipation values).

Table 8. Thermal Parameters With Forced Air Flow and No Heat Sink

Thermal Mgmt. Technique	Defined Parameters			Measured	Calculated		
Air-flow velocity	P_D	T_J	Φ_{JC}	Φ_{JA}	Φ_{CA}	T_C	T_A
100 LFM	3W	125°C	1°C/W	11.7°C/W	10.7°C/W	122°C	89.9°C
250 LFM	3W	125°C	1°C/W	10°C/W	9°C/W	122°C	95°C
500 LFM	3W	125°C	1°C/W	8.9°C/W	7.9°C/W	122°C	98.3°C
750 LFM	3W	125°C	1°C/W	8.5°C/W	7.5°C/W	122°C	99.5°C
1000 LFM	3W	125°C	1°C/W	8.3°C/W	7.3°C/W	122°C	100.1°C
100 LFM	5W	125°C	1°C/W	11.7°C/W	10.7°C/W	120°C	66.5°C
250 LFM	5W	125°C	1°C/W	10°C/W	9°C/W,	120°C	75°C
500 LFM	5W	125°C	1°C/W	8.9°C/W	7.9°C/W	120°C	80.5°C
750 LFM	5W	125°C	1°C/W	8.5°C/W	7.5°C/W	120°C	82.5°C
1000 LFM	5W	125°C	1°C/W	8.3°C/W	7.3°C/W	120°C	83.5°C

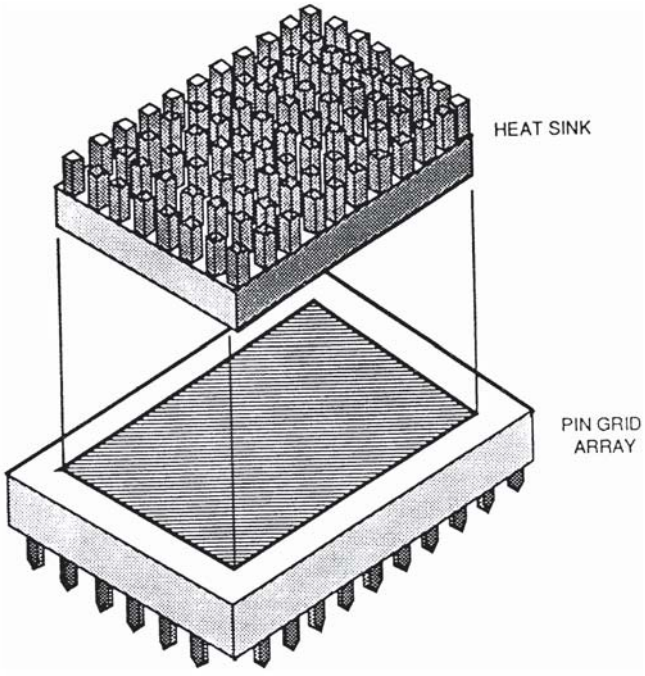
By reviewing the maximum ambient operating temperatures, it can be seen that by using the all-small-buffer configuration of the TS68040 with a relatively small amount of air flow (100 LFM), a 0-70°C ambient operating temperature can be achieved. However, depending on the output buffer configuration and available forced-air cooling, additional thermal management techniques may be required.

Thermal Characteristics with a Heat Sink

In choosing a heat sink the designer must consider many factors: heat sink size and composition, method of attachment, and choice of a wet or dry connection. The following paragraphs discuss the relationship of these decisions to the thermal performance of the design noticed during experimentation.

The heat sink size is one of the most significant parameters to consider in the selection of a heat sink. Obviously a larger heat sink will provide better cooling. However, it is less obvious that the most benefit of the larger heat sink of the pin fin type used in the experimentation would be at still air conditions. Under forced-air conditions as low as 100 LFM, the difference between the ΦCA becomes very small (0.4°C/W or less). This difference continues to decrease as the forced air flow increases. The particular heat sink used in our testing fit the perimeter package surface area available within the capacitor pads on the TS68040 (1.48" x 1.48") and showed a nice compromise between height and thermal performance needs. The heat sink base perimeter area was 1.24" x 1.30" and its height was 0.49". It was a pin-fin-type (i.e. bed of nails) design composed of Al alloy. The heat sink is shown in Figure 5 can be obtained through Thermalloy Inc. by referencing part number 2338B.

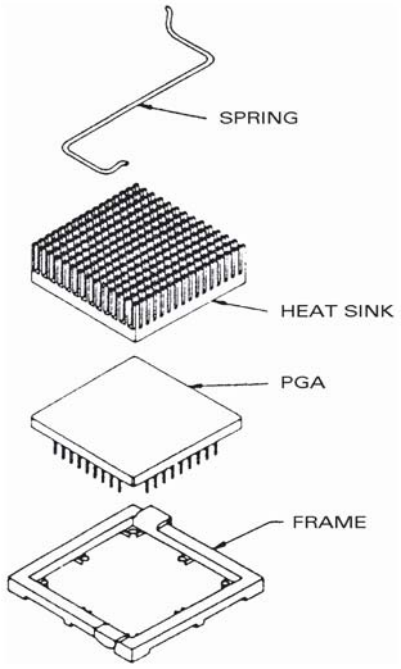
Figure 5. Heat Sink Example



All pin fin heat sinks tested were made from extrusion Al products. The planar face of the heat sink mating to the package should have a good degree of planarity; if it has any curvature, the curvature should be convex at the central region of the heat sink surface to provide intimate physical contact to the PGA surface. All heat sinks tested met this criteria. Nonplanar, concave curvature the central regions of the heat sink will result in poor thermal contact to the package. A specification needs to be determined for the planarity of the surface as part of any heat sink design.

Although there are several ways to attach a heat sink to the package, it was easiest to use a demountable heat sink attach called “E-Z attach for PGA packages” developed by Thermalloy (see Figure 6). The heat sink is clamped to the package with the help of a steel spring to a plastic frame (or plastic shoes Besides the height of the heat sink and plastic frame, no additional height added to the package. The interface between the ceramic package and the heat sink was evaluated for both dry and wet (i.e., thermal grease) interfaces in still air. The thermal grease reduced the Φ_{CA} quite significantly (about 2.5 °C/W) in still air. Therefore, it was used in all other testing done with the heat sink. According to other testing, attachment with thermal grease provided about the same thermal performance as if a thermal epoxy were used.

Figure 6. Heat Sink with Attachment



A sample size of one TS68040 package was tested in still air with the heat sink and attachment method previously described. This test was performed with 3W of power being dissipated from within the package. Since the variance in Φ_{JA} within the possible power range is negligible, it can be assumed for calculation purposes that Φ_{JA} is constant at all power levels. Table 9 shows the result assuming a maximum power dissipation of the part at 3 and 5W (refer to Table 6 to calculate other power dissipation values).

Table 9. Thermal Parameters With Heat Sink and No Air Flow

Thermal Mgmt. Technique	Defined Parameters			Measured	Calculated		
Heat Sink	P_D	T_J	Φ_{JC}	Φ_{JA}	Φ_{CA}	T_C	T_A
2338B	3W	125°C	1°C/W	14°C/W	13°C/W	122°C	83°C
2338B	5W	125°C	1°C/W	14°C/W	13°C/W	120°C	55°C

Thermal Characteristics with a Heat Sink and Forced Air

A sample size of three TS68040 packages was tested in forced-air cooling in a wind tunnel with a heat sink. This test was performed with 3W of power being dissipated from within the package. As mentioned previously, the variance in Φ_{JA} within the possible power range is negligible; it can be assumed for calculation purposes that Φ_{JA} is valid at all power levels. Table 10 shows the results, assuming a maximum power dissipation at 3 and 5W with air flow and heat sink thermal management (refer to Table 6 to calculate other power dissipation values).

Table 10. Thermal Parameters with Heat Sink and Air Flow

Thermal Mgmt. Technique		Defined Parameters			Measured	Calculated		
Air-flow	Heat sink	P_D	T_J	Φ_{JC}	Φ_{JA}	Φ_{CA}	T_C	T_A
100 LFM	2338B	3W	125°C	1°C/W	3.1°C/W	2.1°C/W	122°C	115.7°C
250 LFM	2338B	3W	125°C	1°C/W	2.2°C/W	1.2°C/W	122°C	118.4°C
500 LFM	2338B	3W	125°C	1°C/W	1.7°C/W	0.7°C/W	122°C	119.9°C
750 LFM	2338B	3W	125°C	1°C/W	1.5°C/W	0.5°C/W	122°C	120.5°C
1000 LFM	2338B	3W	125°C	1°C/W	1.4°C/W	0.4°C/W	122°C	120.8°C
100 LFM	2338B	5W	125°C	1°C/W	3.1°C/W	2.1°C/W	120°C	109.5°C
250 LFM	2338B	5W	125°C	1°C/W	2.2°C/W	1.2°C/W	120°C	114°C
500 LFM	2338B	5W	125°C	1°C/W	1.7°C/W	0.7°C/W	120°C	116.5°C
750 LFM	2338B	5W	125°C	1°C/W	1.5°C/W	0.5°C/W	120°C	117.5°C
1000 LFM	2338B	5W	125°C	1°C/W	1.4°C/W	0.4°C/W	120°C	118°C

Thermal Testing Summary

Testing proved that a heat sink in combination with a relatively small amount of air-flow (100 LFM or less) will easily realize a 0-70°C ambient operating temperature for the TS68040 with almost any configuration of the output buffers. A heat sink alone may be capable of providing all necessary cooling, depending on the particular heat sink height/size restraints, the maximum ambient operating temperature required, and the output buffer configuration chosen. Also forced air cooling alone may attain a 0-70°C ambient operating temperature. However this factor is highly dependent on the output buffer configuration chosen and the available forced air for cooling. Figure 7 is a summary of the test results of the relationship between Φ_{JA} and air-flow for the TS68040.

Figure 7. Relationship of Φ_{JA} Air-Flow for PGA

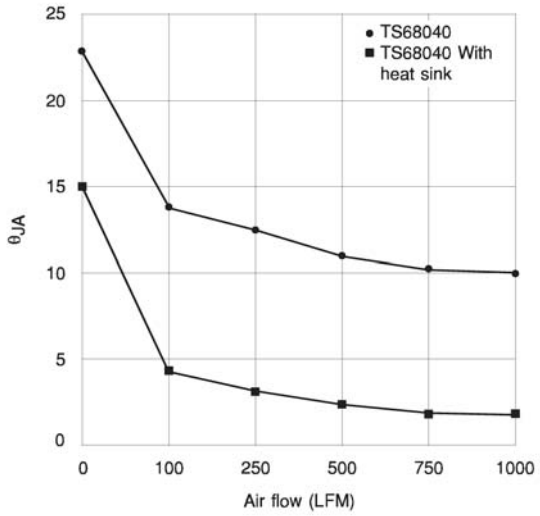


Table 11. Characteristics Guaranteed

Package	Symbol	Parameter	Value	Unit
PGA 179	θ_{J-A}	Thermal Resistance Junction-to-ambient	See Figure 7	°C/W
	θ_{J-C}	Thermal Resistance Junction-to-case	1	°C/W
CQFP 196	θ_{J-A}	Thermal Resistance Junction-to-ambient	TBD	°C/W
	θ_{J-C}	Thermal Resistance Junction-to-case	1	°C/W

Mechanical and Environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or for Atmel standard screening.

Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum:

- Atmel Logo
- Manufacturer's Part Number
- Class B Identification
- Date-code Of Inspection Lot
- ESD Identifier If Available
- Country Of Manufacturing

Quality Conformance Inspection

DESC/MIL-STD-883

Is in accordance with MIL-M-38535 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Groups C and D inspection are performed on a periodical basis.

Electrical Characteristics

General Requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below:

- Table 12: Static electrical characteristics for the electrical variants.
- Table 13: Dynamic electrical characteristics for TS68040 (25 MHz, 33 MHz).

For static characteristics (Table 12), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics (Table 13), test methods refer to clause “Static Characteristics” on page 18 of this specification.

Indication of “min.” or “max.” in the column «test temperature» means minimum or maximum operating temperature as defined in sub-clause Table 5 here above.

Static Characteristics

Table 12. Electrical Characteristics
$-55°C \leq T_C \leq T_{Jmax}$; $4.75V \leq V_{CC} \leq 5.25V$ unless otherwise specified(1)(2)(3)(4)

Symbol	Characteristic		Min	Max	Unit
V_{IH}	Input High Voltage		2	V_{CC}	V
V_{IL}	Input Low Voltage		GND	0.8	V
V_U	Undershoot			- 0.8	V
I_{in}	Input Leakage Current at 0.5/2.4V	$\overline{AVEC}$, BCLK $\overline{BG}$, $\overline{CDIS}$, $\overline{IPLn}$, $\overline{MDIS}$, PCLK, $\overline{RSTI}$, SCn, $\overline{TBI}$, $\overline{TCI}$, TCK, $\overline{TEA}$	-20	20	µA
I_{TSI}	Hi-z (Off-state) Leakage Current at 0.5/2.4V	An, $\overline{BB}$, $\overline{CIOUT}$, Dn, $\overline{LOCK}$, $\overline{LOCKE}$, R/$\overline{W}$, SIZn, $\overline{TA}$, TDO, $\overline{TIP}$, TLNn, TMn, $\overline{TS}$, TTn, UPAn	-20	20	µA
I_{IL}	Signal Low Input Current V_{IL} = 0.8V	TMS, TDI, $\overline{TRST}$	-1.1	-0.18	mA
I_{IH}	Signal High Input Current V_{IH} = 2.0V	TMS, TDI, $\overline{TRST}$	-0.94	-0.16	mA
V_{OH}	Output High Voltage Larger Buffers - I_{OH} = 35 mA Small Buffers - I_{OH} = 5 mA		2.4		V

Table 12. Electrical Characteristics (Continued)
$-55°C \leq T_C \leq T_{Jmax}$; $4.75V \leq V_{CC} \leq 5.25V$ unless otherwise specified(1)(2)(3)(4)

Symbol	Characteristic	Min	Max	Unit
V_{OL}	Output Low Voltage Larger buffers - I_{OL} = 35 mA Small buffers - I_{OL} = 5 mA		0.5	V
P_D	Power Dissipation (T_J = 125°C) Larger Buffers Enabled Small Buffers Enabled		7.7 6.3	W
C_{in}	Capacitance - Note 4 V_{in} = 0V, f = 1 MHz		25	pF

Notes: 1. All testing to be performed using worst-case test conditions unless otherwise specified.
2. Maximum operating junction temperature (T_J) = +125°. Minimum case operating temperature (T_C) = -55°. This device is not tested at T_C = +125°. Testing is performed by setting the junction temperature T_J = +125°and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.
3. Capacitance is periodically sampled rather than 100% tested.
4. Power dissipation may vary in between limits depending on the application.

Dynamic Characteristics

Table 13. Clock AC Timing Specifications (see Figure 8)
$-55°C \leq T_C \leq T_{Jmax}$; $4.75V \leq V_{CC} \leq 5.25V$ unless otherwise specified(1)(2)(3)(4)

Num	Characteristic	25 MHz		33 MHz		Unit
		Min	Max	Min	Max	
Frequency of Operation		20	25	20	33	MHz
1	PCLK Cycle Time	20	25	15	25	ns
2	PCLK Rise Time(4)		1.7		1.7	ns
3	PCLK Fall Time(4)		1.6		1.6	ns
4	PCLK Duty Cycle Measured at 1.5V(4)	47.5	52.5	46.67	53.33	%
4a	PCLK Pulse Width High Measured at 1.5V(3)(4)	9.5	10.5	7	8	ns
4b	PCLK Pulse Width Low Measured at 1.5V(3)(4)	9.5	10.5	7	8	ns
5	BCLK Cycle Time	40	50	30	60	ns
6, 7	BCLK Rise and Fall Time		4		3	ns
8	BCLK Duty Cycle Measured at 1.5V(4)	40	60	40	60	%
8a	BCLK Pulse Width High Measured at 1.5V(4)	16	24	12	18	ns
8b	BCLK Pulse Width Low Measured at 1.5V(4)	16	24	12	18	ns
9	PCLK, BCLK Frequency Stability(4)		1000		1000	ppm
10	PCLK to BCLK Skew		9		n/a	ns

Notes: 1. All testing to be performed using worst-case test conditions unless otherwise specified.
2. Maximum operating junction temperature (T_J) = +125°. Minimum case operating temperature (T_C) = -55°. This device is not tested at T_C = +125°. Testing is performed by setting the junction temperature T_J = +125°and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.
3. Specification value at maximum frequency of operation.
4. If not tested, shall be guaranteed to the limits specified.

Figure 8. Clock Input Timing

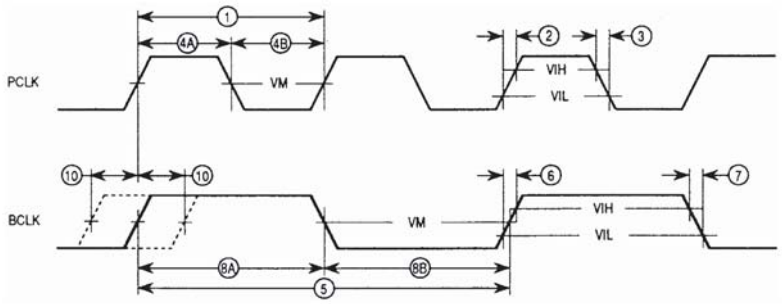


Table 14. Output AC Timing Specifications[1] (Figure 9 to Figure 15)

These output specifications are only for 25 MHz. They must be scaled for lower operating frequencies. Refer to TS6804DH/AD for further information. -55°C ≤T_C ≤T_{Jmax}; 4.75V ≤V_{CC} ≤5.25V unless otherwise specified.[2][3][4]

		25 MHz				33 MHz				
		Large Buffer[1]		Small Buffer[1]		Large Buffer[1]		Small Buffer[1]		
Num	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
11	BCLK to address $\overline{CIOUT}$, $\overline{LOCK}$, $\overline{LOCKE}$, R/$\overline{W}$, SIZn, TLN, TMn, UPAn valid[5]	9	21	9	30	6.50	18	6.50	25	ns
12	BCLK to output invalid (output hold)	9		9		6.50		6.50		ns
13	BCLK to $\overline{TS}$ valid	9	21	9	30	6.50	18	6.50	25	ns
14	BCLK to $\overline{TIP}$ valid	9	21	9	30	6.50	18	6.50	25	ns
18	BCLK to data-out valid[6]	9	23	9	32	6.50	20	6.50	27	ns
19	BCLK to data-out invalid (output hold)[6]	9		9		6.50		6.50		ns
20	BCLK to output low impedance[5][6]	9		9		6.50		6.50		ns
21	BCLK to data-out high impedance	9	20	9	20	6.50	17	6.50	17	ns
26	BCLK to multiplexed address valid[5]	19	31	19	40	14	26	14	33	ns
27	BCLK to multiplexed address driven[5]	19		19		14		14		ns
28	BCLK to multiplexed address high impedance[5][6]	9	18	9	18	6.50	15	6.50	15	ns
29	BCLK to multiplexed data driven[6]	19		19		14	20	14	20	ns
30	BCLK to multiplexed data valid[6]	19	33	19	42	14	28	14	35	ns
38	BCLK to address $\overline{CIOUT}$, $\overline{LOCK}$, $\overline{LOCKE}$, R/$\overline{W}$, SIZn, $\overline{TS}$, TLNn, TMn, TTn, UPAn high impedance[5]	9	18	9	18	6.50	15	6.50	15	ns
39	BCLK to $\overline{BB}$, $\overline{TA}$, $\overline{TIP}$ high impedance	19	28	19	28	14	23	14	23	ns
40	BCLK to $\overline{BR}$, $\overline{BB}$ valid	9	21	9	30	6.50	18	6.50	25	ns
43	BCLK to $\overline{MI}$ valid	9	21	9	30	6.50	18	6.50	25	ns
48	BCLK to $\overline{TA}$ valid	9	21	9	30	6.50	18	6.50	25	ns
50	BCLK to $\overline{IPEND}$, PSTn, $\overline{RSTO}$ valid	9	21	9	30	6.50	18	6.50	25	ns

Notes:
1. Output timing is specified for a valid signal measured at the pin. Large buffer timing is specified driving a 50Ω transmission line with a length characterized by a 2.5 ns one-way propagation delay, terminated through 50Ω to 2.5V. Large buffer output impedance is typically 3Ω, resulting in incident wave switching for this environment. Small buffer timing is specified driving an unterminated 30Ω transmission line with a length characterized by a 2.5 ns one-way propagation delay. Small buffer output impedance is typically 30Ω; the small buffer specifications include approximately 5 ns for the signal to propagate the length of the transmission line and back.
2. All testing to be performed using worst-case test conditions unless otherwise specified.
3. The following pins are active low: $\overline{AVEC}$, $\overline{BG}$, $\overline{BS}$, $\overline{BR}$, $\overline{CDIS}$, $\overline{CIOUT}$, $\overline{IPEND}$, $\overline{IPLO}$, $\overline{IPL1}$, $\overline{IPL2}$, $\overline{LOCK}$, $\overline{LOCKE}$, $\overline{MDIS}$, $\overline{MI}$, $\overline{RST0}$, $\overline{RSTI}$, $\overline{TA}$, $\overline{TBI}$, $\overline{TCI}$, $\overline{TEA}$, $\overline{TIP}$, $\overline{TRST}$, $\overline{TS}$ and $\overline{W}$ of R/$\overline{W}$.
4. Maximum operating junction temperature (T_J) = +125°. Minimum case operating temperature (T_C) = -55°. This device is not tested at T_C = +125°. Testing is performed by setting the junction temperature T_J = +125°and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.
5. Timing specifications 11, 20 and 38 for address bus output timing apply when normal bus operation is selected. Specifications 26, 27 and 28 should be used when the multiplexed bus mode of operation is enabled.
6. Timing specifications 18 and 19 for data bus output timing apply when normal bus operation is selected. Specifications 28 and 29 should be used when the multiplexed bus mode of operation is enabled.

Table 15. Input AC Timing Specifications (Figure 9 to Figure 15)
-55°C ≤T_C ≤T_{Jmax}; 4.75V ≤V_{CC} ≤5.25V unless otherwise specified[1][2][3][4]

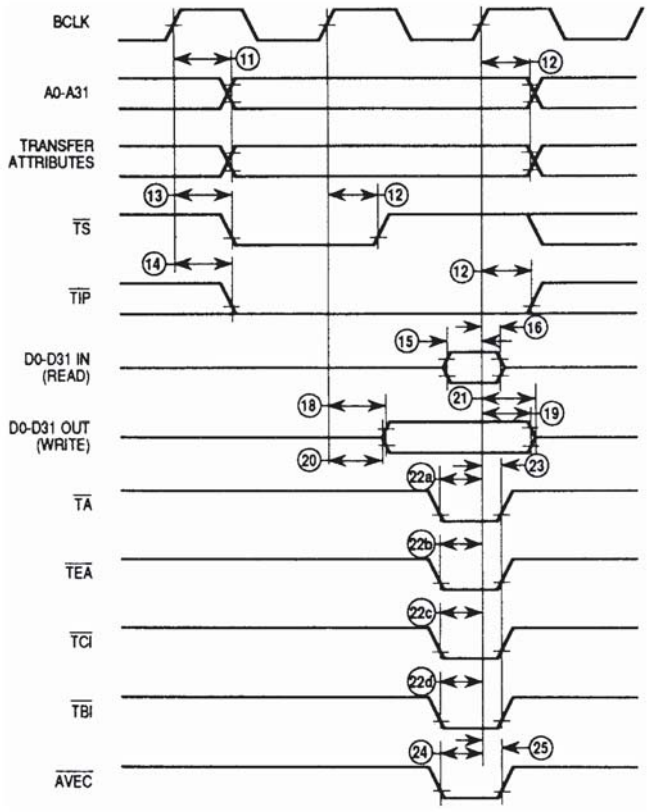
Num	Characteristic	25 MHz		33 MHz		Unit
		Min.	Max.	Min.	Max.	
15	Data-in Valid to BCLK (Setup)	5		4		ns
16	BCLK to Data-in Invalid (Hold)	4		4		ns
17	BCLK to Data-in High Impedance (Read Followed By Write)		49		36.5	ns
22a	$\overline{TA}$ Valid to BCLK (Setup)	10		10		ns
22b	$\overline{TEA}$ Valid to BCLK (Setup)	10		10		ns
22c	$\overline{TCI}$ Valid to BCLK (Setup)	10		10		ns
22d	$\overline{TBI}$ Valid to BCLK (Setup)	11		10		ns
23	BCLK to $\overline{TA}$, $\overline{TEA}$, $\overline{TCI}$, $\overline{TBI}$ Invalid (Hold)	2		2		ns
24	$\overline{AVEC}$ Valid to BCLK (Setup)	5		5		ns
25	BCLK to $\overline{AVEC}$ Invalid (Hold)	2		2		ns
31	DLE Width High	8		8		ns
32	Data-in Valid to DLE (Setup)	2		2		ns
33	DLE to Data-in Invalid (Hold)	8		8		ns
34	BCLK to DLE Hold	3		3		ns
35	DLE High to BCLK	16		12		ns
36	Data-in Valid to BCLK (DLE Mode Setup)	5		5		ns
37	BCLK Data-in Invalid (DLE Mode Hold)	4		4		ns
41a	$\overline{BB}$ Valid to BCLK (Setup)	7		7		ns
41b	$\overline{BG}$ Valid to BCLK (Setup)	8		7		ns
41c	$\overline{CDIS}$, $\overline{MDIS}$ Valid to BCLK (Setup)	10		8		ns
41d	$\overline{IPLn}$ Valid to BCLK (Setup)	4		3		ns
42	BCLK to $\overline{BB}$, $\overline{BG}$, $\overline{CDIS}$, $\overline{IPLn}$, $\overline{MDIS}$ Invalid (Hold)	2		2		ns
44a	Address Valid to BCLK (Setup)	8		7		ns
44b	SIZn Valid BCLK (Setup)	12		8		ns

Table 15. Input AC Timing Specifications (Figure 9 to Figure 15) (Continued)
-55°C ≤T_C ≤T_{Jmax}; 4.75V ≤V_{CC} ≤5.25V unless otherwise specified[1][2][3][4]

Num	Characteristic	25 MHz		33 MHz		Unit
		Min.	Max.	Min.	Max.	
44c	TTn Valid to BCLK (Setup)	6		8.5		ns
44d	R/$\overline{W}$ Valid to BCLK (Setup)	6		5		ns
44e	SCn Valid to BCLK (Setup)	10		11		ns
45	BCLK to Address SIZn, TTn, R/$\overline{W}$, SCn Invalid (Hold)	2		2		ns
46	$\overline{TS}$ Valid to BCLK (Setup)	5		9		ns
47	BCLK to $\overline{TS}$ Invalid (Hold)	2		2		ns
49	BCLK to $\overline{BB}$ High Impedance (68040 Assumes Bus Mastership)		9		9	ns
51	$\overline{RSTI}$ Valid to BCLK	5		4		ns
52	BCLK to $\overline{RSTI}$ Invalid	2		2		ns
53	Mode Select Setup to $\overline{RSTI}$ Negated[4]	20		20		ns
54	$\overline{RSTI}$ Negated to Mode Selects Invalid[4]	2		2		ns

Notes:
1. All testing to be performed using worst-case test conditions unless otherwise specified.
2. The following pins are active low: $\overline{AVEC}$, $\overline{BG}$, $\overline{BS}$, $\overline{BR}$, $\overline{CDIS}$, $\overline{CIOUT}$, $\overline{IPEND}$, $\overline{IPLO}$, $\overline{IPL1}$, $\overline{IPL2}$, $\overline{LOCK}$, $\overline{LOCKE}$, $\overline{MDIS}$, $\overline{MI}$, $\overline{RST0}$, $\overline{RSTI}$, $\overline{TA}$, $\overline{TBI}$, $\overline{TCI}$, $\overline{TEA}$, $\overline{TIP}$, $\overline{TRST}$, $\overline{TS}$ and $\overline{W}$ of R/$\overline{W}$.
3. Maximum operating junction temperature (T_J) = +125°. Minimum case operating temperature (T_C) = -55°. This device is not tested at T_C = +125°. Testing is performed by setting the junction temperature T_J = +125°and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.
4. The levels on $\overline{CDIS}$, $\overline{MDIS}$, and the $\overline{IPL2}$-$\overline{IPL0}$ signals enable or disable the multiplexed bus mode, data latch enable mode, and driver impedance selection respectively.

Figure 9. Read/Write Timing



Note: Transfer attribute signals UPAN, SIZN, TTN, TMN, TLNN, R/$\overline{W}$, $\overline{LOCK}$, $\overline{LOCKE}$, $\overline{CIOUT}$

Table 16. JTAG Timing Application (Figure 16 to Figure 19)
-55°C ≤T_C ≤$T_J$max; 4.75V ≤V_{CC} ≤5.25V unless otherwise specified(1)(2)

Num	Characteristic	Min	Max	Unit
	TCK Frequency	0	10	MHz
1	TCK Cycle Time	100		ns
2	TCK Clock Pulse Width Measured at 1.5V	40		ns
3	TCK Rise and Fall Times	0	10	ns
4	$\overline{TRST}$ Setup Time to TCK Falling Edge	40		ns
5	$\overline{TRST}$ Assert Time	100		ns
6	Boundary Scan Input Data Setup Time	50		ns
7	Boundary Scan Input Data Hold Time	50		ns
8	TCK to Output Data Valid	0	50	ns
9	TCK to Output High Impedance	0	50	ns
10	TMS, TDI Data Setup Time	20		ns
11	TMS, TDI Data Hold Time	5		ns
12	TCK to TDO Data Valid	0	20	ns
13	TCK to TDO High Impedance	0	20	ns

Notes: 1. All testing to be performed using worst-case test conditions unless otherwise specified.
2. Maximum operating junction temperature (T_J) = +125°. Minimum case operating temperature (T_C) = -55°. This device is not tested at T_C = +125°. Testing is performed by setting the junction temperature T_J = +125° and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

Table 17. Boundary Scan Instruction Codes

Bit 2	Bit 1	Bit 0	Instruction Selected	Test Data Register Accessed
0	0	0	Extest	Boundary Scan
0	0	1	Highz	Bypass
0	1	0	Sample/Preload	Boundary Scan
0	1	1	DRVCTLT	Boundary Scan
1	0	0	Shutdown	Bypass
1	0	1	Private	Bypass
1	1	0	DRVCTLS	Boundary Scan
1	1	1	Bypass	Bypass

Switching Test Circuit and Waveforms

Figure 10. Address and Data Bus Timing — Multiplexed Bus Mode

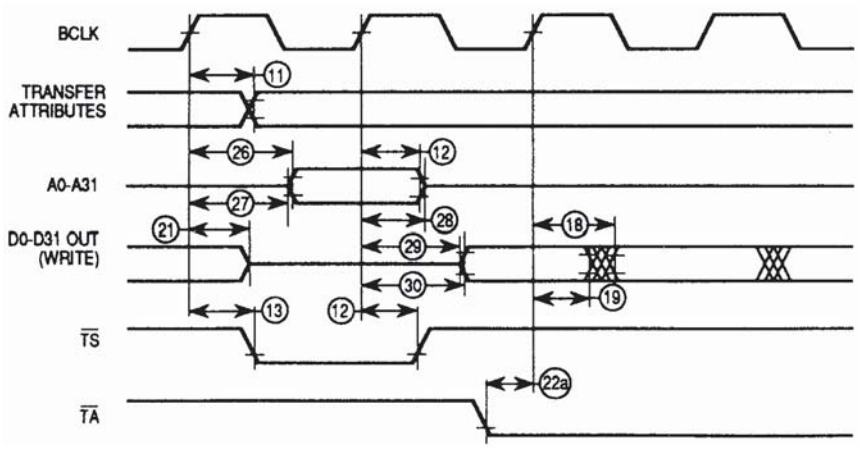


Figure 11. DLE Timing Burst Access

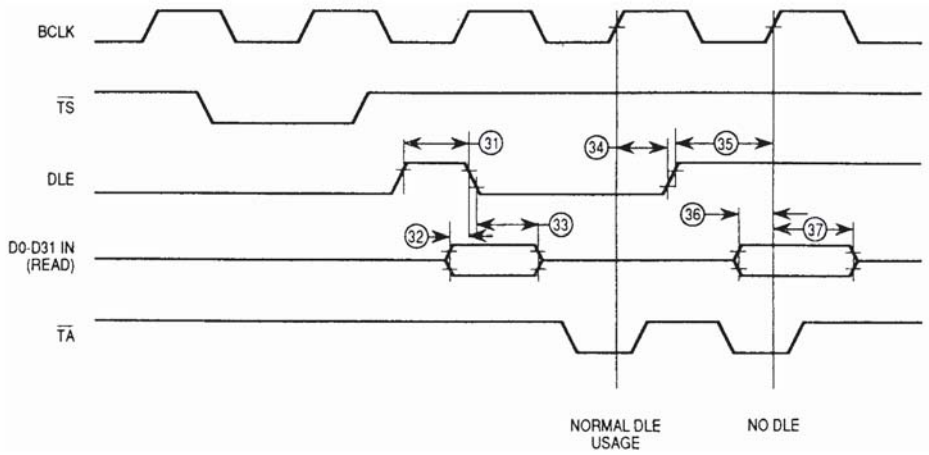


Figure 12. Bus Arbitration Timing