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Features

- **16-/32-bit Data and Address Register**
- **16-Mbyte Direct Addressing Range**
- **56 Powerful Instruction Types**
- **Operations on Five Main Data Types**
- **Memory Mapped Input/Output**
- **14 Addressing Modes**
- **Three Available Versions: 8 MHz/10 MHz and 12.5 MHz**
- **Military Temperature Range: -55/+125°C**
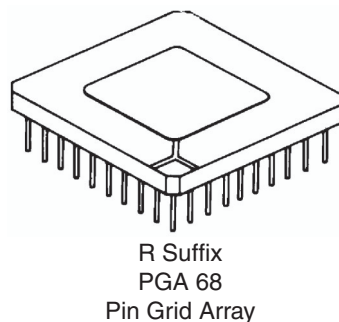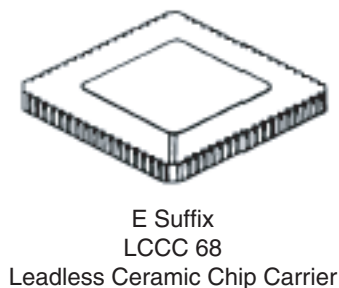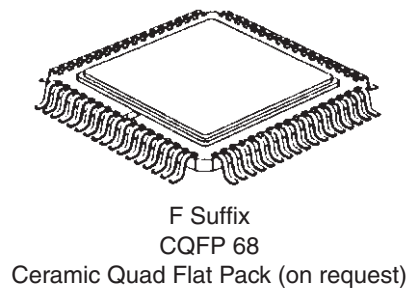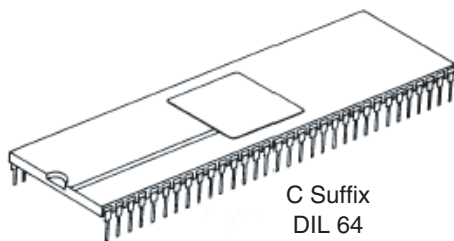- **Power Supply: $5V_{DC} \pm 10\%$**

Description

The TS68C000 reduced power consumption device dissipates an order of magnitude less power than the HMOS TS68000. The TS68C000 is an implementation of the TS68000 16/32 microprocessor architecture. The TS68C000 has a 16-bit data bus and 24-bit address bus while the full architecture provides for 32-bit address and data-buses. It is completely code-compatible with the HMOS TS68000, TS68008 8-bit data bus implementation of the TS68000 and the TS68020 32-bit implementation of the architecture. Any user-mode programs written using the TS68C000 instruction set will run unchanged on the TS68000, TS68008 and TS68020. This is possible because the user programming model is identical for all processors and the instruction sets are proper sub-sets of the complete architecture.

Screening/Quality

This product is manufactured in full compliance with:

- **MIL-STD-883 class B**
- **DESC drawing 5962-89462**
- **Atmel standards**

C Suffix
DIL 64
Ceramic Package

F Suffix
CQFP 68
Ceramic Quad Flat Pack (on request)

E Suffix
LCCC 68
Leadless Ceramic Chip Carrier

R Suffix
PGA 68
Pin Grid Array

Rev. 2170A–HIREL–09/05

1. General Description

1.1 Introduction

This detail specification contains both a summary of the TS68C000 as well as detailed set of parametrics. The purpose is twofold to provide an instruction to the TS68C000 and support for the sophisticated user. For detail information on the TS68C000, refer to "68000 16-bit microprocessor user's manual".

1.2 Detailed Block Diagram

The functional block diagram is given in Figure 1-1 below.

Figure 1-1. Block Diagram
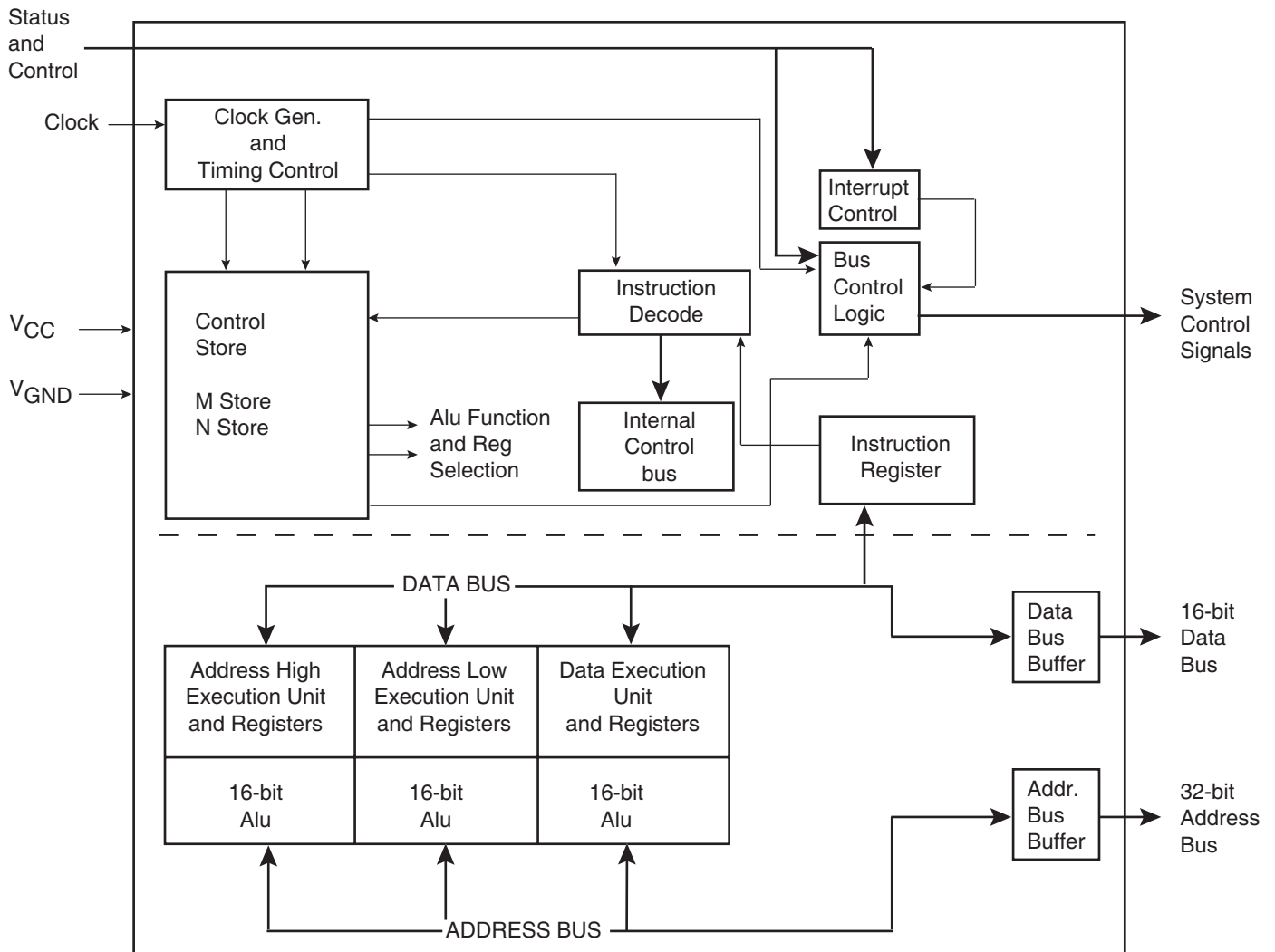
1.3   Pin Assignments

Figure 1-2.   64-lead Dual-in-Line Package

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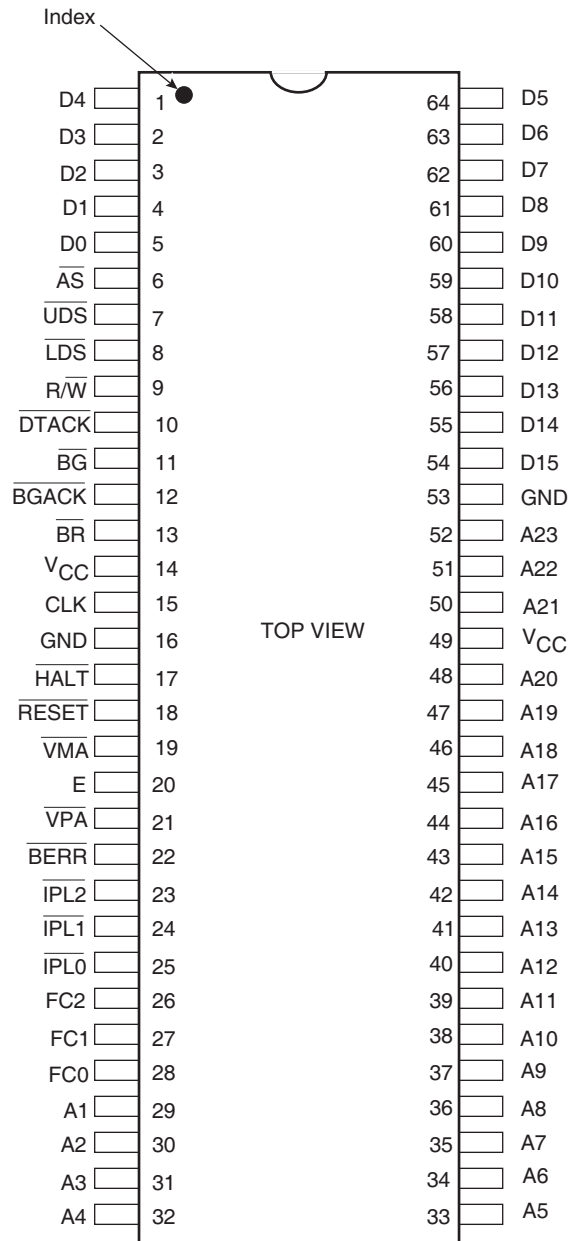|			
D4	1	64	D5
D3	2	63	D6
D2	3	62	D7
D1	4	61	D8
D0	5	60	D9
$\overline{AS}$	6	59	D10
$\overline{UDS}$	7	58	D11
$\overline{LDS}$	8	57	D12
R/$\overline{W}$	9	56	D13
$\overline{DTACK}$	10	55	D14
$\overline{BG}$	11	54	D15
$\overline{BGACK}$	12	53	GND
$\overline{BR}$	13	52	A23
V$_{CC}$	14	51	A22
CLK	15	50	A21
GND	16	49	V$_{CC}$
$\overline{HALT}$	17	48	A20
$\overline{RESET}$	18	47	A19
$\overline{VMA}$	19	46	A18
E	20	45	A17
$\overline{VPA}$	21	44	A16
$\overline{BERR}$	22	43	A15
$\overline{IPL2}$	23	42	A14
$\overline{IPL1}$	24	41	A13
$\overline{IPL0}$	25	40	A12
FC2	26	39	A11
FC1	27	38	A10
FC0	28	37	A9
A1	29	36	A8
A2	30	35	A7
A3	31	34	A6
A4	32	33	A5

TOP VIEW

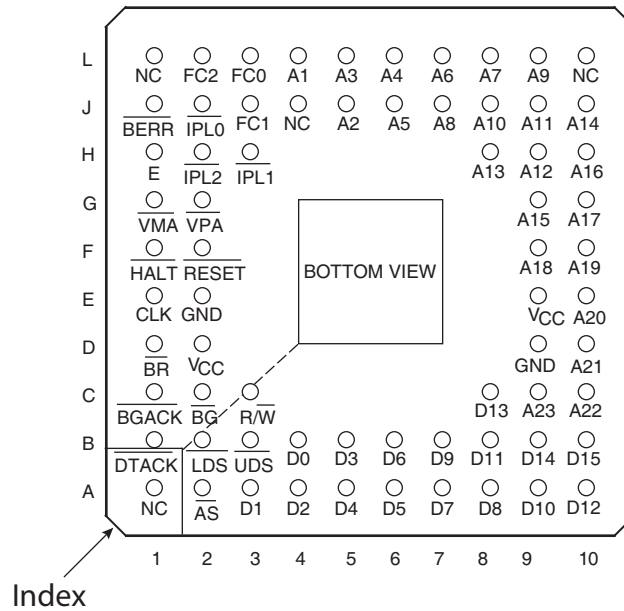**Figure 1-3.** 68-terminal Pin Grid Array

Index
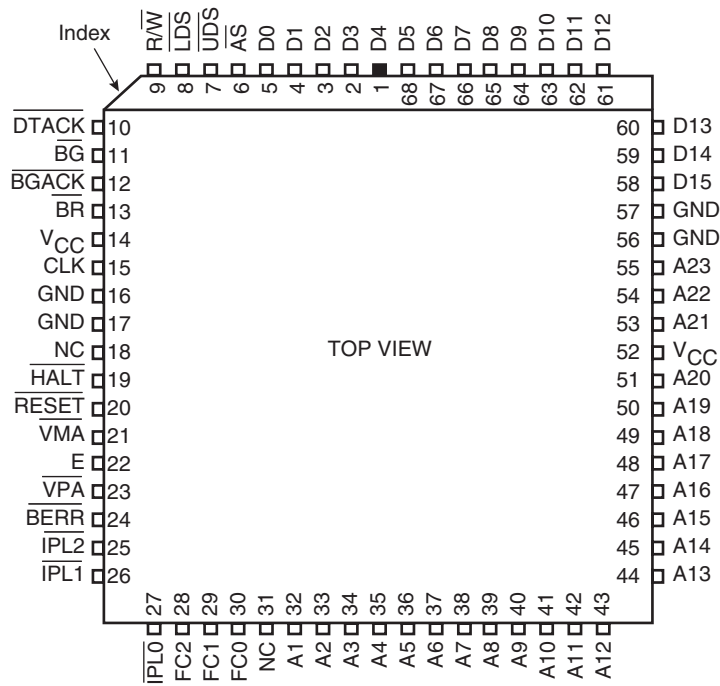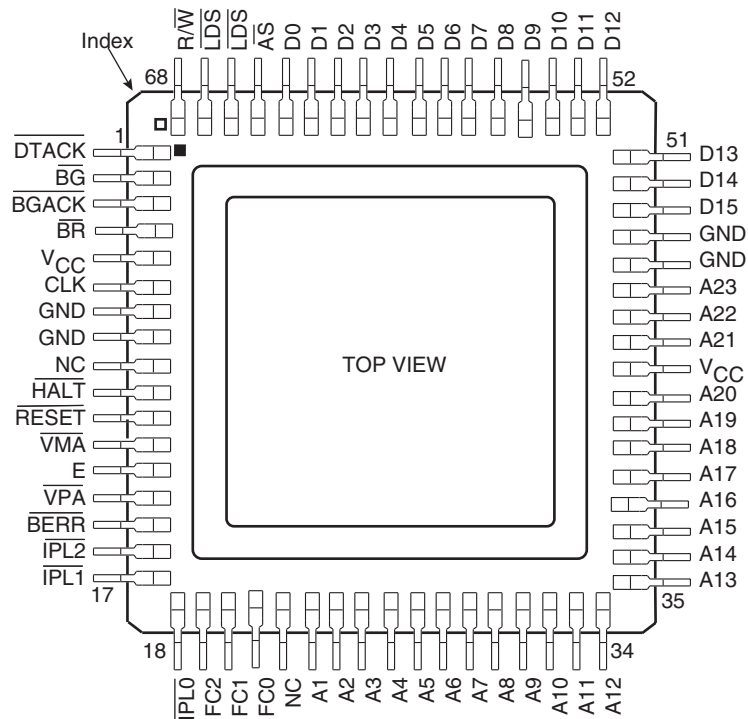
Figure 1-4. 68-lead Quad Pack

Figure 1-5. 68-ceramic Quad Flat Pack

1.4 Terminal Designations

The function, category and relevant symbol of each terminal of the device are given in the following table.

Table 1-1. Terminal Designations

Symbol	Function	Category
V_{CC}	Power supply (2 terminals)	Supply
V_{SS}[1]	Power supply (2 terminals)	Terminals
FC0 to FC2	Processor status	Outputs
$\overline{IPL0}$ to $\overline{IPL2}$	Interrupt control	Inputs
A1 to A23	Address bus	Outputs
$\overline{AS}$	Asynchronous bus control	Outputs
R/$\overline{W}$		
$\overline{UDS}$		
$\overline{LDS}$		
$\overline{DTACK}$		Input
$\overline{BR}$	Bus arbitration control	Inputs
$\overline{BGACK}$		
$\overline{BG}$		Output

Table 1-1. Terminal Designations (Continued)

Symbol	Function	Category
$\overline{\text{BERR}}$	System control	Input
$\overline{\text{RESET}}$		Input/Output
$\overline{\text{HALT}}$		
$\overline{\text{VPA}}$	6800 peripheral control	Input
$\overline{\text{VMA}}$		Output
E		Output
CLK	Clock	Input
D0 to D15	Data bus	Input/Output

Note: 1. V_{SS} is the reference terminal for the voltages

1.5 Signal Description

The input and output signals are illustrated functionally in Figure 1-6 and are described in the following paragraphs.

Figure 1-6. Input and Output Signals
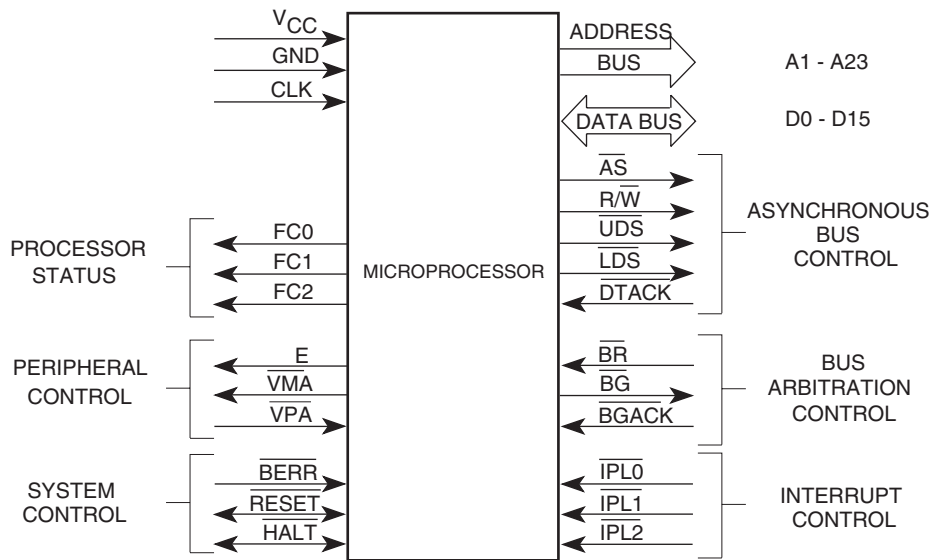
Table 1-2. Data Strobe Control of Data Bus

$\overline{\text{UDS}}$	$\overline{\text{LDS}}$	R/$\overline{\text{W}}$	D8-D15	D0-D7
High	High		No valid data	No valid data
Low	Low	High	Valid data bits 8-15	Valid data bits 0-7
High	Low	High	No valid data	Valid data bits 0-7
Low	High	High	Valid data bits 8-15	No valid data
Low	Low	Low	Valid data bits 8-15	Valid data bits 0-7
High	Low	Low	Valid data bits 0-7	Valid data bits 0-7
Low	High	High	Valid data bits 8-15	Valid data bits 8-15

1.5.0.1   Address Bus (A1 through A23)

This 24-bit, unidirectional, three-state bus is capable of addressing 16 megabytes of data. It provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines A1, A2 and A3 provide information about what level interrupt is being serviced while address lines A4 through A23 are set to a logic high.

1.5.0.2   Data Bus (D0 Through D15)

This 16-bit, bidirectional, three-state bus is the general-purpose data path. It can transfer and accept data in either word or byte length. During an interrupt acknowledge cycle, the external device supplies the vector number on data lines D0-07.

1.5.0.3   Asynchronous Bus Control

Asynchronous data transfers are handled using the following control signals: address strobe, read/write, upper and lower data strobes, and data transfer acknowledge. These signals are explained in the following paragraphs.

ADDRESS STROBE ($\overline{AS}$)

This signal indicates that there is a valid address on the address bus.

READ/WRITE (R/$\overline{W}$)

This signal defines the data bus transfer as a read or write cycle. The R/$\overline{W}$ signal also works in conjunction with the data strobes as explained in the following paragraph.

UPPER AND LOWER DATA STROBE ($\overline{UDS}$, $\overline{LDS}$)

These signals control the flow of data on the data bus, as shown in Table 1-2. When the R/$\overline{W}$ line is high, the processor will read from the data bus as indicated. When the R/W line is low, the processor will write to the data bus as shown.

DATA TRANSFER ACKNOWLEDGE ($\overline{DTACK}$)

This input indicates that the data transfer is completed. When the processor recognizes $\overline{DTACK}$ during a read cycle, data is latched and the bus cycle terminated. When $\overline{DTACK}$ is recognized during a write cycle, the bus cycle is terminated.

1.5.0.4   Bus Arbitration Control

The three signals, bus request, bus grant, and bus grant acknowledge, form a bus arbitration circuit to determine which device will be the bus master device.

BUS REQUEST ($\overline{BR}$)

This input is wire ORed with all other devices that could be bus masters. This input indicates to the processor that some other device desires to become the bus master.

BUS GRANT ($\overline{BG}$)

This output indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle.

BUS GRANT ACKNOWLEDGE ($\overline{BGACK}$)

This input indicates that some other device has become the bus master.

This signal should not be asserted until the following four conditions are met:

1. a bus grant has been received,
2. address strobe is inactive which indicates that the microprocessor is not using the bus,
3. data transfer acknowledge is Inactive which indicates that neither memory nor peripherals are using the bus, and
4. bus grant acknowledge is inactive which indicates that no other device is still claiming bus mastership.

1.5.0.5   *Interrupt Control ($\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$)*

These Input pins indicate the encoded priority level of the device requesting an interrupt. Level seven is the highest priority white level zero indicates that no interrupts are requested. Level seven cannot be masked. The least significant bit is given in IPLO and the most significant bit is contained in $\overline{IPL2}$. These lines must remain stable until the processor signals interrupt acknowledge (FC0-FC2 are all high) to insure that the interrupt is recognized.

1.5.0.6   *System Control*

The system control inputs are used to either reset or halt the processor and to indicate to the processor that bus errors have occurred. The three system control inputs are explained in the following paragraphs.

BUS ERROR ($\overline{BERR}$)

This input informs the processor that there is a problem with the cycle currently being executed. Problems may be a result of:

1. nonresponding devices,
2. interrupt vector number acquisition failure,
3. illegal access request as determined by a memory management unit, or
4. other application dependent errors.

The bus error signal interacts with the halt signal to determine if the current bus cycle should be re-executed or if exception processing should be performed.

RESET ($\overline{RESET}$)

This bidirectional signal line acts to reset (start a system initialization sequence) to processor in response to an external reset signal. An internally generated reset (result of a $\overline{RESET}$ instruction) causes all external devices to be reset and the internal of the processor is not affected. A total system reset (processor and external devices) is the result of external $\overline{HALT}$ and $\overline{RESET}$ signals applied at the same time.

HALT ($\overline{HALT}$)

When this bldirectional line is driven by an external device, it will cause the processor to stop at the completion of the current bus cycle. When the processor has been halted using this input, all control signals are inactive and all three-state lines are put in their high-impedance state.

When the processor has stopped executing Instructions, such as in a double bus fault condition, the $\overline{HALT}$ line is driven by the processor to indicate to external devices that the processor has stopped.

1.5.0.7   EF 6800 Peripheral Control

These control signals are used to allow the interfacing of synchronous EF 6800 peripheral devices with the asynchronous TS68C000. These signals are explained in the following paragraphs.

ENABLE (E)

This signal is the standard enable signal common to all EF 6800 type peripheral devices. The period for this output is ten TS68C000 clock periods (six clocks low, four clocks high). Enable is generated by an internal ring counter which may come up in any state (i.e., at power on, it Is impossible to guarantee phase relationship of E to CLK). E is a free-running crack and runs regardless of the state of the bus on the MPU.

VALID PERIPHERAL ADDRESS ($\overline{\text{VPA}}$)

This input indicates that the device or region addressed is an TS68000 Family device and that data transfer should be synchronized with the enable (E) signal. This Input also indicates that the processor should use automatic vectoring for an interrupt during an IACK cycle.

VALID MEMORY ADDRESS ($\overline{\text{VMA}}$)

This output is used to indicate to TS68000 peripheral devices that there is a valid address on the address bus and the processor is synchronized to enable. This signal only responds to a valid peripheral address ($\overline{\text{VPA}}$) input which indicates that the peripheral is an TS68000 Family device.

1.5.0.8   Processor Status (FC0, FC1, FC2)

These function code outputs indicate the state (user or supervisor) and the cycle type currently being executed, as shown in Table 1-3. The information indicated by the function code outputs is valid whenever address strobe ($\overline{\text{AS}}$) is active.

Table 1-3.   Processor Status Table

Function Code Output			
FC2	**FC1**	**FC0**	**Cycle Time**
Low	Low	Low	(Undefined, reserved)
Low	Low	High	User data
Low	High	Low	User program
Low	High	High	(Undefined, reserved)
High	Low	Low	(Undefined, reserved)
High	Low	High	Supervisor data
High	High	Low	Supervisor program
High	High	High	Interrupt acknowledge

1.5.0.9   Clock (CLK)

The clock input is a TTL-compatible signal that is internally buffered for development of the internal clocks needed by the processor. The clock input should not be gated off at any time and the clock signal must conform to minimum and maximum pulse width times. The clock is a constant frequency square wave with no stretching or shaping techniques required.

2. Detailed Specifications

2.1 Scope

This drawing describes the specific requirements for the microprocessor TS68C000, 8 MHz, 10 MHz and 12.5 MHz, in compliance with MIL-STD-883 class B.

2.2 Applicable Documents

2.2.1 MIL-STD-883

1. MIL-STD-883: Test Methods and Procedures For Electronics
2. MIL-PRF-38535 Appendix A: General Specifications for Microcircuits

2.3 Requirements

2.3.1 General

The microcircuits are in accordance with the applicable document and as specified herein.

2.4 Design and Construction

2.4.1 Terminal Connections

Depending on the package, the terminal connections shall be as shown in Figure 1-2, Figure 1-3, Figure 1-4 and Figure 1-5.

2.4.2 Lead Material and Finish

Lead material and finish shall be any option of MIL-PRF-38535 Appendix A-3-5-6 "Package Element Material and Finsh".

2.4.3 Package

The macrocircuits are packaged in hermetically sealed ceramic package which is conform to case outlines of MIL-PRF-38535 Appendix A-3-5-1.

- PGA68 64 LEAD DIP
- 64 DILSQ. LCC 68 PINS
- 68 LCCC68 TERMINALS JCC
- 68 CQFP

The precise case outlines are described on figures and into MIL-M-38510.

2.4.4 Electrical Characteristics

2.4.4.1 Absolute Maximum Ratings

Limiting conditions (ratings) defined below shall not be for inspection purposes. However some limiting conditions (ratings) may be taken in other parts of this specification as detail conditions for an applicable test.

Unless otherwise stated, all voltages are referenced to the reference terminal as defined in Table 1-1, "Terminal Designations" on page 5 of this specification.

Table 2-1. Absolute Maximum Ratings

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{CC}	Supply voltage		-0.3	+6.5	V
V_I	Input voltage		-0.3	+6.5	V
V_O	Output voltage		NA	NA	V
V_{OZ}	Off state voltage		-0.3	11.0	V
I_O	Output currents		NA	NA	mA
I_i	Input currents		NA	NA	mA
P_{DMAX}	Max power dissipation	T_{CASE} = -55°C		0.27	W
		T_{CASE} = +125°C		0.27	W
T_{STG}	Storage temperature		-55	+150	°C
T_J	Junction temperature			+150	°C
T_{LEADS}	Lead temperature	Max 5 sec. Soldering		+270	°C

2.4.4.2   Recommended Condition of Use and Guaranteed Characteristics

• Guaranteed Characteristics (Table 2-5 and Table 2-8)

The characteristics associated to a specified measurement in the detail specification shall only be for inspection purposes.

Such characteristic defined in this specification is guaranteed only under the conditions and within the limits which are specified for the relevant measurement. Unless otherwise specified, this guarantee applies within all the recommended operating ranges specified below.

• Recommended conditions of use (Table 2-2)

To the correct operation of the device, the conditions of use shall be within the ranges specified below (see also above).

These conditions shall not be for inspection purposes.

Some recommended values may, however, be taken in other parts of this specification as detail conditions for an applicable test (Table 2-9).

• Additional Electrical Characteristics (Table 2-9), see "Additional Electrical Characteristics" on page 30.

Figure 2-1. Clock Input Timing Diagram
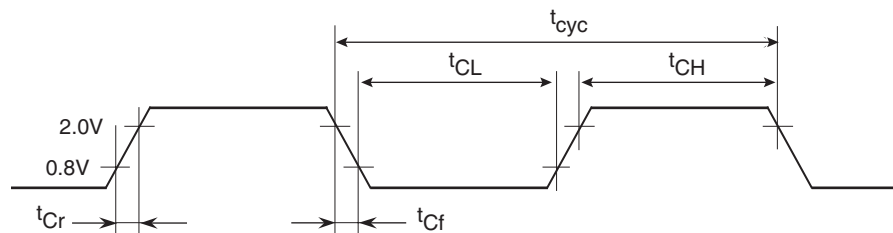
Note: Timing measurements are referenced to and from a low voltage of 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing through this range should start outside, and pass through, the range such that the rise of fall will be linear between 0.8V and 2.0V.

Unless otherwise stated, all voltages are referenced to the reference terminal (see Table 1-1).

Table 2-2. Recommended Condition of Use

Symbol	Parameter	Operating Range			
		Model	Min	Max	Unit
V_{CC}	Supply voltage	All	4.5	5.5	V
V_{IL}	Low level input voltage	All	0	0.8	V
V_{IH}	High level input voltage (see also "Package" on page 10)	All	2.0	V_{CC}	V
T_{CASE}	Operating temperature	All	-55	+125	°C
R_L	Value of output load resistance	All	(1)		Ω
C_L	Output loading capacitance	All		(1)	pF
$t_{r(c)}$	Clock rise time (see Figure 2-1)	All		10	ns
$t_{f(c)}$	Clock fall time (see Figure 2-1)	All		10	ns
f_C	Clock frequency (see Figure 2-1)	TS68C000-8	4.0	8.0	MHz
		TS68C000-10	4.0	10.0	MHz
		TS68C000-12	4.0	12.5	MHz
t_{CYC}	Clock time (see Figure 2-1)	TS68C000-8	125	250	ns
		TS68C000-10	100	250	ns
		TS68C000-12	80	250	ns
$t_{W(CL)}$	Clock pulse width low (see Figure 2-1)	TS68C000-8	55	125	ns
		TS68C000-10	45	125	ns
		TS68C000-12	35	125	ns
$t_{W(CH)}$	Cycle pulse width high (see Figure 2-1)	TS68C000-8	55	125	ns
		TS68C000-10	45	125	ns
		TS68C000-12	35	125	ns

Note: 1. Load networks number 1 to 4 as specified in "Test Conditions Specific to the Device" on page 26 (Figure 2-2 and Figure 2-3) gives the maximum loading for the relevant output.

2.4.4.3 Special Recommended Conditions for CMOS Devices

1. CMOS Latch-up

The CMOS cell is basically composed of two complementary transistors (a P-channel and an N-channel), and, in the steady state, only one transistor is turned-on. The active P-channel transistor sources current when the output is a logic high and presents a high impedance when the output is a logic low. Thus the overall result is extremely low power consumption because there is no power loss through the active P.channel transistor. Also since only once transistor is determined by leakage currents.

Because the basic CMOS cell is composed of two complementary transistors, a virtual semiconductor controlled rectifier (SCR) may be formed when an input exceeds the supply voltage. The SCR that is formed by this high input causes the device to become "latched" in a mode that may result in excessive current drain and eventual destruction of the device. Although the device is Implemented with input protection diodes, care should be exercised to ensure that the maximum input voltages specification is not exceeded tram voltage transients; others may require no additional circuitry.

2. CMOS Applications

• The TS68C000 completely satisfies the input/output drive requirements of CMOS logic devices.

• The HCMOS TS68C000 provides an order of magnitude power dissipation reduction when compared to the HMOS TS68000. However, the TS68C000 does not offer a "power down" or "halt" mode. The minimum operating frequency of the TS68C000 is 4 MHz.

2.4.5 Thermal Characteristics

Table 2-3. Thermal Characteristics

Package	Symbol	Parameter	Value	Unit
DIL 64	θ_{JA}	Thermal resistance junction to ambient	25	°C/W
	θ_{JC}	Thermal resistance junction to case	6	°C/W
PGA 68	θ_{JA}	Thermal resistance junction to ambient	30	°C/W
	θ_{JC}	Thermal resistance junction to case	6	°C/W
LCCC 68	θ_{JA}	Thermal resistance junction to ambient	40	°C/W
	θ_{JC}	Thermal resistance junction to case	8	°C/W
CQFP 68	θ_{JA}	Thermal resistance junction to ambient	40	°C/W
	θ_{JC}	Thermal resistance junction to case	10	°C/W

2.4.5.1 Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \qquad\qquad (1)$$

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts – Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins – User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An Approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K: (T_J + 273) \qquad\qquad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273) + \theta_{JA} \cdot P_D{}^2 \qquad\qquad (3)$$

where K is constant pertaining to the particular part K can be determined from the equation (3) by measuring PD (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}).

These terms are related by the equation:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \qquad\qquad (4)$$

θ_{JA} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals $\theta_{JC.}$ Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

2.4.6   Mechanical and Environmental

The microcircuits shall meet all mechanical environmental requirements of MIL-STD-883 for class B devices.

2.4.7   Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit is legible and permanently marked with the following information as minimum:

- Atmel Logo
- Manufacturer's Part Number
- Class B Identification
- Date-code of inspection lot
- ESD Identifier if Available
- Country of Manufacturing

2.5   Quality Conformance Inspection

2.5.1   DESC/MIL-STD-883

Is in accordance with MIL-PRF-38535 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

2.6   Electrical Characteristics

2.6.1   General Requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurements conditions are given below:

- Table 2-4: Static Electrical Characteristics for all electrical variants.
- Table 2-5, Table 2-6, Table 2-7 and Table 2-8: Dynamic electrical characteristics for 8 MHz, 10 MHz and 12.5 MHz.

For static characteristics (Table 2-4), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics, test methods refer to clause "Test Conditions Specific to the Device" on page 26 of this specification (Table 2-5, Table 2-6, Table 2-7 and Table 2-8).

Indication of "min" or "max" in the column "test temperature" means minimum or maximum operating temperatures as defined in sub-clause "Recommended Condition of Use and Guaranteed Characteristics" on page 11 here above.

14   TC68C000

Table 2-4. Static Characteristics

V_{CC} = 5.0V V_{DC} ± 10%; GND = 0 V_{DC}; Tc = -55/+125°C and -40°C/+85°C

Test Number	Symbol	Parameter	Ref Number (**)	Test Conditions	Test Temperature	Limits Min (*)	Limits Max (*)	Unit
1	I_{CC}	Supply current	41	V_{CC} = 5.5V F_C = 8 MHz F_C = 10 MHz F_C = 12 MHz	All		42 45 50	mA
2	V_{OL}[1]	Low level output voltage for: A1 to A23 FC0 to FC2; $\overline{BG}$	37	V_{CC} = 4.5V I_{OL} = 3.2 mA	25°C max min		0.5	V
3	V_{OL}[2]	Low level output voltage for: $\overline{HALT}$	37	V_{CC} = 4.5V I_{OL} = 1.6 mA	25°C max min		0.5	V
4	V_{OL}[3]	Low level output voltage for: $\overline{AS}$; R/$\overline{W}$: D0 to D15 UDS; $\overline{LDS}$; $\overline{VMA}$ and E	37	V_{CC} = 4.5V I_{OL} = 5.3 mA	25°C max min		0.5	V
5	V_{OL}[4]	Low level output voltage for: $\overline{RESET}$	37	V_{CC} = 4.5V I_{OL} = 5.0 mA	25°C max min		0.5	V
6	V_{OH}	High level output voltage for all outputs	37	V_{CC} = 4.5V I_{OH} = -400 µA	25°C max min	2.4	V_{CC} – 0.75	V
7	I_{IH}[1]	High level input current for all inputs excepted $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.5V V_I = 5.5V	25°C max min		2.5	µA
8	I_{IL}[1]	Low level input current for all inputs excepted $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.5V V_I = 0V	25°C max min	-2.5		µA
9	I_{IH}[2]	High level input current for: $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.5V V_I = 5.5V	25°C max min		20	µA
10	I_{IL}[2]	Low level input current for: $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.5V V_I = 0V	25°C max min	-20		µA

Table 2-4. Static Characteristics (Continued)
V_{CC} = 5.0V V_{DC} ± 10%; GND = 0 V_{DC}; Tc = -55/+125°C and -40°C/+85°C

Test Number	Symbol	Parameter	Ref Number (**)	Test Conditions	Test Temperature	Limits Min (*)	Limits Max (*)	Unit
11	I_{OHZ}	High level output 3-state leakage current		V_{CC} = 5.5V	25°C		20	µA
					max			
				V_{OH} = 2.4V	min			
12	I_{OLZ}	Low level output 3-state leakage current		V_{CC} = 5.5V	25°C		20	µA
					max			
				V_{OL} = 0.4V	min			
13	V_{IH}	High level input voltage for all inputs		V_{CC} = 4.5V	25°C	2.0		V
					max			
				V_{CC} = 5.5V	min			
14	V_{IL}	Low level input voltage for all inputs		V_{CC} = 4.5V	25°C		0.8	V
					max		0.8	V
				V_{CC} = 5.5V	min		0.8	V
14A	C_{IN}	Input capacitance (all inputs)	11	Reverse voltage = 0V f = 1.0 MHz	25°C		25	pF
					max		NA	pF
					min		NA	pF
14B	C_{OUT}	Output capacitance (all inputs)	11	Reverse voltage = 0V f = 1.0 MHz	25°C		20	pF
					max		NA	pF
					min		NA	pF
14C	V_{TEST}	Internal protection Transient energy rating		See note[9] 5 cycles	25°C	-500	+500	V

Note: * Algebraic values
** Measurement method: see "General Requirements" on page 14 and "Test Conditions Specific to the Device" on page 26.

Referred notes are given on page 25.

Table 2-5. Dynamic Characteristics – TS68C000-8
V_{CC} = 5.0 V_{DC} ± 10%; GND = 0 V_{DC}; Tc = -55/+125°C and Tc = -40°C/+85°C

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Limits Min (*)	Limits Max (*)	Unit
27	t_{SU} (DICL)	Set-up time Data-in to clock low[1]	10 – 11	See "Input and Output Signals for Dynamic Measurements" on page 29 (a) to (c) f_C = 8 MHz	25°C	20[10]		ns
					max			
					min			

Table 2-5. Dynamic Characteristics – TS68C000-8 (Continued)
V_{CC} = 5.0 V_{DC} ± 10%; GND = 0 V_{DC}; Tc = -55/+125°C and Tc = -40°C/+85°C

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Limits Min (*)	Limits Max (*)	Unit
47	t_{SU} (SDTCL)	Set-up time $\overline{DTACK}$ low to clock low[1]	10 – 11	Idem test 27	25°C / max / min	20[10]		ns
47	t_{SU} (SBRCL)	Set-up time $\overline{BR}$ low to clock low [1]	10 – 11	Idem test 27	25°C / max / min	20[10]		ns
47	t_{SU} (SBGCL)	Set-up time $\overline{BGACK}$ low to clock low[1]	10 – 11	Idem test 27	25°C / max / min	20[10]		ns
47	t_{SU} (SVPACL)	Set-up time $\overline{VPA}$ low to clock low [1]	10 – 11	Idem test 27	25°C / max / min	20[10]		ns
47	t_{SU} (SBERCL)	Set-up time $\overline{BERR}$ low to clock low[1]	10 – 11	Idem test 27	25°C / max / min	20[10]		ns
2	t_{w} (CL)	Clock width low	10 – 11	Idem test 27	25°C / max / min	55[10]	125	ns
3	t_{w} (CH)	Clock width high	10 – 11	Idem test 27	25°C / max / min	55	125	ns
6A	t_{PLH} t_{PHL} (CHFCV)	Propagation time clock high to FC valid	10 – 11	Idem test 27 Load: 3	25°C / max / min		70	ns
9	t_{PHL} (CHSLX)	Propagation time clock high to $\overline{AS}$ low	10 – 11	Idem test 27 Load: 4	25°C / max / min		60[3]	
9	t_{PHL} (CHSL)	Propagation time CLK high to $\overline{LDS}$, $\overline{UDS}$ low	10 – 11	Idem test 27 Load: 4	25°C / max / min		60[3]	ns
12	t_{PLH} (CLSH)	Propagation time CLK low to $\overline{AS}$ high	10 – 11	Idem test 27 Load: 4	25°C / max / min		70[3]	ns

Table 2-5. Dynamic Characteristics – TS68C000-8 (Continued)
V_{CC} = 5.0 V_{DC} ± 10%; GND = 0 V_{DC}; Tc = -55/+125°C and Tc = -40°C/+85°C

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Limits Min (*)	Limits Max (*)	Unit
12	t_{PLH} (CLSH)	Propagation time CLK low to $\overline{LDS}$, $\overline{UDS}$ high	10 – 11	Idem test 27 Load: 4	25°C / max / min		70[3]	ns
18	t_{PLH} (CHRHX)	Propagation time CLK high to R/$\overline{W}$ high	10 – 11	Idem test 27 Load: 4	25°C / max / min		70[3]	ns
20	t_{PHL} (CHRL)	Propagation time CLK high to R/$\overline{W}$ low	10 – 11	Idem test 27 Load: 4	25°C / max / min		70[3]	ns
23	t_{PZL} t_{PZH} (CLDO)	Propagation time CLK low to Data-out valid	10 – 11	Idem test 27 Load: 4	25°C / max / min		70[3]	ns
6	t_{PZL} t_{PZH} (CLAV)	Propagation time CLK low to Address valid	10 – 11	Idem test 27 Load: 3	25°C / max / min		70	ns
32	t_{HRRF}	$\overline{RESET}$/$\overline{HALT}$ input transition time	10 – 11	Idem test 27	25°C / max / min		200	ns
33	t_{PHL} (CHGL)	Propagation time CLK high to $\overline{BG}$ low	12	Idem test 27 Load: 3	25°C / max / min		70	ns
34	t_{PLH} (CHGH)	Propagation time CLK high to $\overline{BG}$ high	12	Idem test 27 Load: 3	25°C / max / min		70	ns
40	t_{PHL} (CLVM)	Propagation time CLK low to $\overline{VMA}$ low	13	Idem test 27 Load: 4	25°C / max / min		70	ns
41	t_{PHL} (CLE)	Propagation time CLK low to E low	13	Idem test 27 Load: 4	25°C / max / min		70	ns
8	t_h (SHAZ)	Hold time CLK high to Address	10 – 11	Idem test 27 Load: 3	25°C / max / min	0		ns

Table 2-5. Dynamic Characteristics – TS68C000-8 (Continued)
V_{CC} = 5.0 V_{DC} ± 10%; GND = 0 V_{DC}; Tc = -55/+125°C and Tc = -40°C/+85°C

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Limits Min (*)	Max (*)	Unit
11	t_{SU} (AVSL)	Set-up time Address valid to $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ low	10 – 11	Idem test 27 Load: 4	25°C	30[4]		ns
					max			
					min			
35	t_{PHL} (BRLGL)	Propagation time $\overline{BR}$ low to $\overline{BG}$ low	12	Idem test 27 Load: 3	25°C	1.5	3.5	CLKS [2]
					max			
					min		+90	ns
37	t_{PLH} (GALEH)	Propagation time $\overline{BGACK}$ low to $\overline{BG}$ high	12	Idem test 27 Load: 3	25°C	1.5	3.5	CLKS [2]
					max			
					min		+90	ns
48	t_{SU} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	11	Idem test 27	25°C	20[5]	–	ns
					max			
					min			
48	t_{SU} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	10 – 11	Idem test 27	25°C	20[5]	–	ns
					max			
					min			
26	t_h (DOSL)	Hold time Data-out valid to $\overline{LDS}$, $\overline{UDS}$ low	11	Idem test 27 Load: 4	25°C	30[4]	–	ns
					max			
					min			

Note: * Algebraic values
          ** Measurement method: see "General Requirements" on page 14 and "Test Conditions Specific to the Device" on page 26
Referred notes are given on page 25.

Table 2-6. Dynamic Characteristics – TS68C000-10

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Limits Min (*)	Max (*)	Unit
27	t_{SU} (DICL)	Set-up time Data-in to clock low[1]	10 – 11	See "Input and Output Signals for Dynamic Measurements" on page 29 (a) to (c) fc = 10 MHz	25°C	20[10]		ns
					max			
					min			
47	t_{SU} (SDTCL)	Set-up time $\overline{DTACK}$ low to clock low[1]	10 – 11	Idem test 27	25°C	20[10]		ns
					max			
					min			

Table 2-6. Dynamic Characteristics – TS68C000-10 (Continued)

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Limits Min (*)	Limits Max (*)	Unit
47	t_{SU} (SBRCL)	Set-up time $\overline{BR}$ low to clock low [1]	10 – 11	Idem test 27	25°C	20[10]		ns
					max			
					min			
47	t_{SU} (SBGCL)	Set-up time $\overline{BGACK}$ low to clock low[1]	10 – 11	Idem test 27	25°C	20[10]		ns
					max			
					min			
47	t_{SU} (SVPACL)	Set-up time $\overline{VPA}$ low to clock low [1]	10 – 11	Idem test 27	25°C	20[10]		ns
					max			
					min			
47	t_{SU} (SBERCL)	Set-up time $\overline{BERR}$ low to clock low[1]	10 – 11	Idem test 27	25°C	20[10]		ns
					max			
					min			
2	t_w (CL)	Clock width low	10 – 11	Idem test 27	25°C	45	125	ns
					max			
					min			
3	t_w (CH)	Clock width high	10 – 11	Idem test 27	25°C	45	125	ns
					max			
					min			
6A	t_{PLH} t_{PHL} (CHFCV)	Propagation time clock high to FC valid	10 – 11	Idem test 27 Load: 3	25°C		60	ns
					max			
					min			
9	t_{PHL} (CHSLX)	Propagation time clock high to AS low	10 – 11	Idem test 27 Load: 4	25°C		55[3]	ns
					max			
					min			
9	t_{PHL} (CHSL)	Propagation time CLK high to LDS, UDS low	10 – 11	Idem test 27 Load: 4	25°C		55[3]	ns
					max			
					min			
12	t_{PLH} (CLSH)	Propagation time CLK low to AS high	10 – 11	Idem test 27 Load: 4	25°C		55[3]	ns
					max			
					min			
12	t_{PLH} (CLSH)	Propagation time CLK low to LDS, UDS high	10 – 11	Idem test 27 Load: 4	25°C		55[3]	ns
					max			
					min			

Table 2-6. Dynamic Characteristics – TS68C000-10 (Continued)

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Min (*)	Max (*)	Unit
18	t_{PLH} (CHRHX)	Propagation time CLK high to R/W high	10 – 11	Idem test 27 Load: 4	25°C / max / min		60[3]	ns
20	t_{PHL} (CHRL)	Propagation time CLK high to R/W low	10 – 11	Idem test 27 Load: 4	25°C / max / min		60[3]	ns
23	t_{PZL} t_{PZH} (CLDO)	Propagation time CLK low to Data-out valid	10 – 11	Idem test 27 Load: 4	25°C / max / min		55[3]	ns
6	t_{PZL} t_{PZH} (CLAV)	Propagation time CLK low to Address valid	10 – 11	Idem test 27 Load: 4	25°C / max / min		60	ns
32	t_{HRRF} (CHGL)	RESET/HALT input transition time	10 – 11	Idem test 27	25°C / max / min		200	ns
33	t_{PHL} (CHGL)	Propagation time CLK high to BG low	12	Idem test 27 Load: 3	25°C / max / min		60	ns
34	t_{PLH} (CHGH)	Propagation time CLK high to BG high	12	Idem test 27 Load: 3	25°C / max / min		60	ns
40	t_{PHL} (CLVM)	Propagation time CLK low to VMA low	13	Idem test 27 Load: 4	25°C / max / min		70	ns
41	t_{PHL} (CLE)	Propagation time CLK low to E low	13	Idem test 27 Load: 4	25°C / max / min		55	ns
8	t_H (SHAZ)	Hold time CLK high to Address	10 – 11	Idem test 27 Load: 3	25°C / max / min	0		ns
11	t_{SU} (AVSL)	Set-up time Address valid to AS, LDS, UDS low	10 – 11	Idem test 27 Load: 4	25°C / max / min	20[4]		ns

Table 2-6. Dynamic Characteristics – TS68C000-10 (Continued)

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Limits Min (*)	Limits Max (*)	Unit
35	t$_{PHL}$ (BRLGL)	Propagation time BR low to BG low	12	Idem test 27 Load: 3	25°C		3.5	CLKS [2]
					max	1.5		
					min		+80	ns
37	t$_{PLH}$ (GALGH)	Propagation time BGACK low to BG high	12	Idem test 27 Load: 3	25°C		3.5	CLKS [2]
					max	1.5		
					min		+80	ns
48	t$_{SU}$ (BELDAL)	Set-up time BERR low to DTACK low	11	Idem test 27	25°C	20 [5]		ns
					max			
					min			
48	t$_{SU}$ (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	10 – 11	Idem test 27	25°C	20 [5]		ns
					max			
					min			
26	t$_{H}$ (DOSL)	Hold time Data-out valid to $\overline{LDS}$, $\overline{UDS}$ low	11	Idem test 27 Load: 4	25°C	20 [4]		ns
					max			
					min			

Note: * Algebraic values
          ** Measurement method: see "General Requirements" on page 14 and "Test Conditions Specific to the Device" on page 26

Table 2-7. Dynamic Characteristics – TS68C000-12

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Limits Min (*)	Limits Max (*)	Unit
27	t$_{SU}$ (DICL)	Set-up time Data-in to clock low [1]	10 – 11	See "Input and Output Signals for Dynamic Measurements" on page 29 (a) to (c) f$_C$ = 12 MHz	25°C	10 [10]		ns
					max			
					min			
47	t$_{SU}$ (SDTCL)	Set-up time $\overline{DTACK}$ low to clock low [1]	10 – 11	Idem test 27	25°C	20 [10]		ns
					max			
					min			
47	t$_{SU}$ (SBRCL)	Set-up time $\overline{BR}$ low to clock low [1]	10 – 11	Idem test 27	25°C	20 [10]		ns
					max			
					min			

Table 2-7. Dynamic Characteristics – TS68C000-12 (Continued)

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Limits Min (*)	Limits Max (*)	Unit
47	t_{SU} (SBGCL)	Set-up time $\overline{BGACK}$ low to clock low[1]	10 – 11	Idem test 27	25°C	20[10]		ns
					max			
					min			
47	t_{SU} (SVPACL)	Set-up time $\overline{VPA}$ low to clock low[1]	10 – 11	Idem test 27	25°C	20[10]		ns
					max			
					min			
47	t_{SU} (SBERCL)	Set-up time $\overline{BERR}$ low to clock low[1]	10 – 11	Idem test 27	25°C	20[10]		ns
					max			
					min			
2	t_w (CL)	Clock width low	10 – 11	Idem test 27	25°C	35	125	ns
					max			
					min			
3	t_w (CH)	Clock width high	10 – 11	Idem test 27	25°C	35	125	ns
					max			
					min			
6A	t_{PLH} t_{PHL} (CHFCV)	Propagation time clock high to FC valid	10 – 11	Idem test 27 Load: 3	25°C		55	ns
					max			
					min			
9	t_{PHL} (CHSLX)	Propagation time clock high to $\overline{AS}$ low	10 – 11	Idem test 27 Load: 4	25°C		55[3]	ns
					max			
					min			
9	t_{PHL} (CHSL)	Propagation time CLK high to $\overline{LDS}$, $\overline{UDS}$ low	10 – 11	Idem test 27 Load: 4	25°C		55[3]	ns
					max			
					min			
12	t_{PLH} (CLSH)	Propagation time CLK low to $\overline{LDS}$, $\overline{UDS}$ high	10 – 11	Idem test 27 Load: 4	25°C		50[3]	ns
					max			
					min			
12	t_{PLH} (CLSH)	Propagation time CLK low to $\overline{LDS}$, $\overline{UDS}$ high	10 – 11	Idem test 27 Load: 4	25°C		50[3]	ns
					max			
					min			
18	t_{PLH} (CHRHX)	Propagation time CLK high to R/$\overline{W}$ high	10 – 11	Idem test 27 Load: 4	25°C		60[3]	ns
					max			
					min			

Table 2-7. Dynamic Characteristics – TS68C000-12 (Continued)

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Min (*)	Max (*)	Unit
20	t_{PHL} (CHRL)	Propagation time CLK high to R/$\overline{W}$ low	11	Idem test 27 Load: 4	25°C / max / min		60[3]	ns
23	t_{PZL} t_{PZH} (CLDO)	Propagation time CLK low to Data-out valid	11	Idem test 27 Load: 4	25°C / max / min		55[3]	ns
6	t_{PZL} t_{PZH} (CLAV)	Propagation time CLK low to Address valid	10 – 11	Idem test 27 Load: 4	25°C / max / min		55	ns
32	t_{HRRF}	$\overline{RESET}$/$\overline{HALT}$ transition time	10 – 11	Idem test 27	25°C / max / min		150	ns
33	t_{PHL} (CHGL)	Propagation time CLK high to $\overline{BG}$ low	8 – 9	Idem test 27 Load: 3	25°C / max / min		50	ns
34	t_{PLH} (CHGH)	Propagation time CLK high to $\overline{BG}$ high	12	Idem test 27 Load: 3	25°C / max / min		50	ns
40	t_{PHL} (CLVM)	Propagation time CLK low to $\overline{VMA}$ low	13	Idem test 27 Load: 4	25°C / max / min		70	ns
41	t_{PHL} (CLE)	Propagation time CLK low to E low	13	Idem test 27 Load: 4	25°C / max / min		45	ns
8	t_H (SHAZ)	Hold time CLK high to Address	10 – 11	Idem test 27 Load: 3	25°C / max / min	0		ns
11	t_{SU} (AVSL)	Set-up time Address valid to $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ low	10 – 11	Idem test 27 Load: 4	25°C / max / min	15[4]		ns
35	t_{PHL} (BRLGL)	Propagation time $\overline{BR}$ low to $\overline{BG}$ low	12	Idem test 27 Load: 3	25°C / max / min	1.5	3.5 / +70	CLKS [2] ns

Table 2-7. Dynamic Characteristics – TS68C000-12 (Continued)

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Min (*)	Max (*)	Unit
37	t_{PLH} (GALGH)	Propagation time $\overline{BGACK}$ low to $\overline{BG}$ high	12	Idem test 27 Load: 3	25°C		3.5	CLKS [2]
					max	1.5		
					min		+70	ns
48	t_{SU} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	11	Idem test 27	25°C	20 [5]		ns
					max			
					min			
48	t_{SU} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	10 – 11	Idem test 27	25°C	20 [5]		ns
					max			
					min			
26	t_{H} (DOSL)	Hold time Data-out valid to $\overline{LDS}$, $\overline{UDS}$ low	11	Idem test 27 Load: 4	25°C	15 [4]		ns
					max			
					min			

Note: * Algebraic values
** Measurement method: see "General Requirements" on page 14 and "Test Conditions Specific to the Device" on page 26

2.6.1.1   Referred notes to Table 2-4, Table 2-5, Table 2-6, Table 2-7

The following notes shall apply where referred into Table 2-4, Table 2-5, Table 2-6 and Table 2-7.

Notes: 1. If the asynchronous setup tlme (47) requirements are satisfied, the $\overline{DTACK}$ low-to-data setup time (31) requirement Gan be ignored. The data must only satisfy the data-in to clock-low setup time (27) for the following cycle.
2. Where "CLKS" is stated as unit time limit, the relevant time in nanoseconds shall be calculated as the actual cycle time of clock signal input multiply by the given number of CLKS limits.
3. For a loading capacitance of less than or equal to 50 picofarads, substrate 5 nanoseconds from the value given in the maximum columns.
4. Actual value depends on period.
5. If 47 is satisfied for bath $\overline{DTACK}$ and $\overline{BERR}$, 48 may be 0 nanoseconds.
6. The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.
7. The falling edge of 56 triggers bath the negation of the strobes ($\overline{AS}$, and X DS) and the falling edge of E. either of these events can occur first depending upon the loading on each signal. Specification 49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.
8. When $\overline{AS}$ and R/$\overline{W}$ are equally loaded (±20%), substrate 10 nanoseconds from the values in these columns.
9. Each terminal of the device under test shall be tested separately against all existing VCC and VSS terminals of the device which shall be shorted together for the test. The other untested terminals shall be unconnected during the test. One cycle consists of the application of the bath limits as given in Table 2-5, Table 2-6 and Table 2-7.
10. This value should be treated as a min for design purpose. For the conformance testing the value shall be regarded as the maximum time.