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Features

- **CPU32+ Processor (4.5 MIPS at 25 MHz)**
  - **32-bit Version of the CPU32 Core (Fully Compatible with the CPU32)**
  - **Background Debug Mode**
  - **Byte-misaligned Addressing**
- **Up to 32-bit Data Bus (Dynamic Bus Sizing for 8 and 16 Bits)**
- **Up to 32 Address Lines (At Least 28 Always Available)**
- **Complete Static Design (0 - 25 MHz Operation)**
- **Slave Mode to Disable CPU32+ (Allows Use with External Processors)**
  - **Multiple QUICCs Can Share One System Bus (One Master)**
  - **TS68040 Companion Mode Allows QUICC to be a TS68040 Companion Chip and Intelligent Peripheral (22 MIPS at 25 MHz)**
  - **Peripheral Device of TSPC603e (see DC415/D note)**
- **Four General-purpose Timers**
  - **Superset of MC68302 Timers**
  - **Four 16-bit Timers or Two 32-bit Timers**
  - **Gate Mode Can Enable/Disable Counting**
- **Two Independent DMAs (IDMAs)**
- **System Integration Module (SIM60)**
- **Communications Processor Module (CPM)**
- **Four Baud Rate Generators**
- **Four SCCs (Ethernet/IEEE 802.3 Optional on SCC1-Full 10 Mbps Support)**
- **Two SMC**
- **V_{CC} = +5V ± 5%**
- **f_{max} = 25 MHz and 33 MHz**
- **Military Temperature Range: -55°C < T_C < +125°C**
- **P_D = 1.4 W at 25 MHz; 5.25V**
  2 W at 33 MHz; 5.25V

Description

The TS68EN360 QUad Integrated Communication Controller (QUICC™) is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications. It particularly excels in communications activities. The QUICC (pronounced “quick”) can be described as a next-generation TS68302 with higher performance in all areas of device operation, increased flexibility, major extensions in capability, and higher integration. The term “quad” comes from the fact that there are four serial communications controllers (SCCs) on the device; however, there are actually seven serial channels: four SCCs, two serial management controllers (SMCs), and one serial peripheral interface (SPI).

Screening/Quality

This product is manufactured in full compliance with:

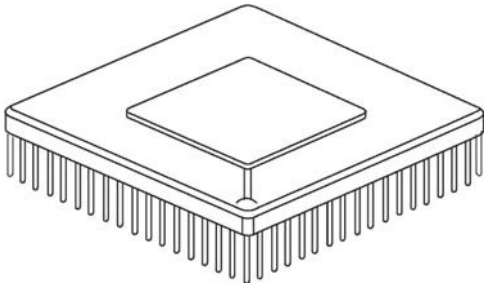
- MIL-STD-883 (class B)
- QML (class Q)
- or according to Atmel standards

32-bit Quad Integrated Communication Controller

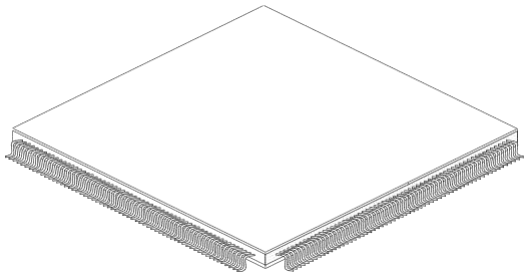
TS68EN360

Rev. 2113A–HIREL–03/02

R suffix
PGA 241
Ceramic Pin Grid Array Cavity Up



A suffix
CERQUAD 240
Ceramic Leaded Chip Carrier Cavity Down



Introduction

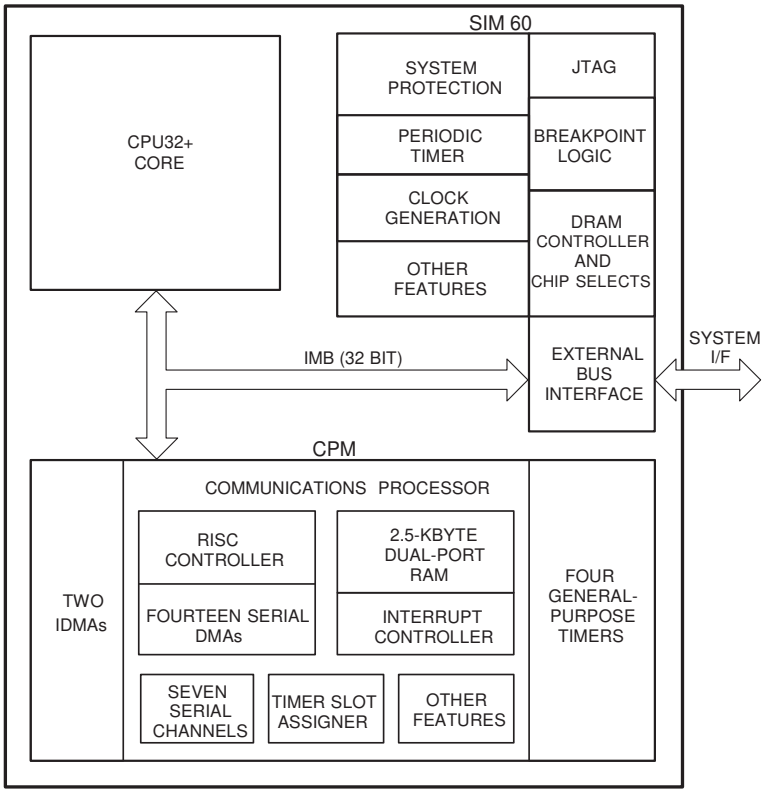
QUICC Architecture Overview

The QUICC is 32-bit controller that is an extension of other members of the TS68300 family. Like other members of the TS68300 family, the QUICC incorporates the inter-module bus (IMB). The TS68302 is an exception, having an 68000 bus on chip. The IMB provides a common interface for all modules of the TS68300 family, which allows the development of new devices more quickly by using the library of existing modules. Although the IMB definition always included an option for an on-chip 32-bit bus, the QUICC is the first device to implement this option.

The QUICC is comprised of three modules: the CPU32+ core, the SIM60, and the CPM. Each module utilizes the 32-bit IMB.

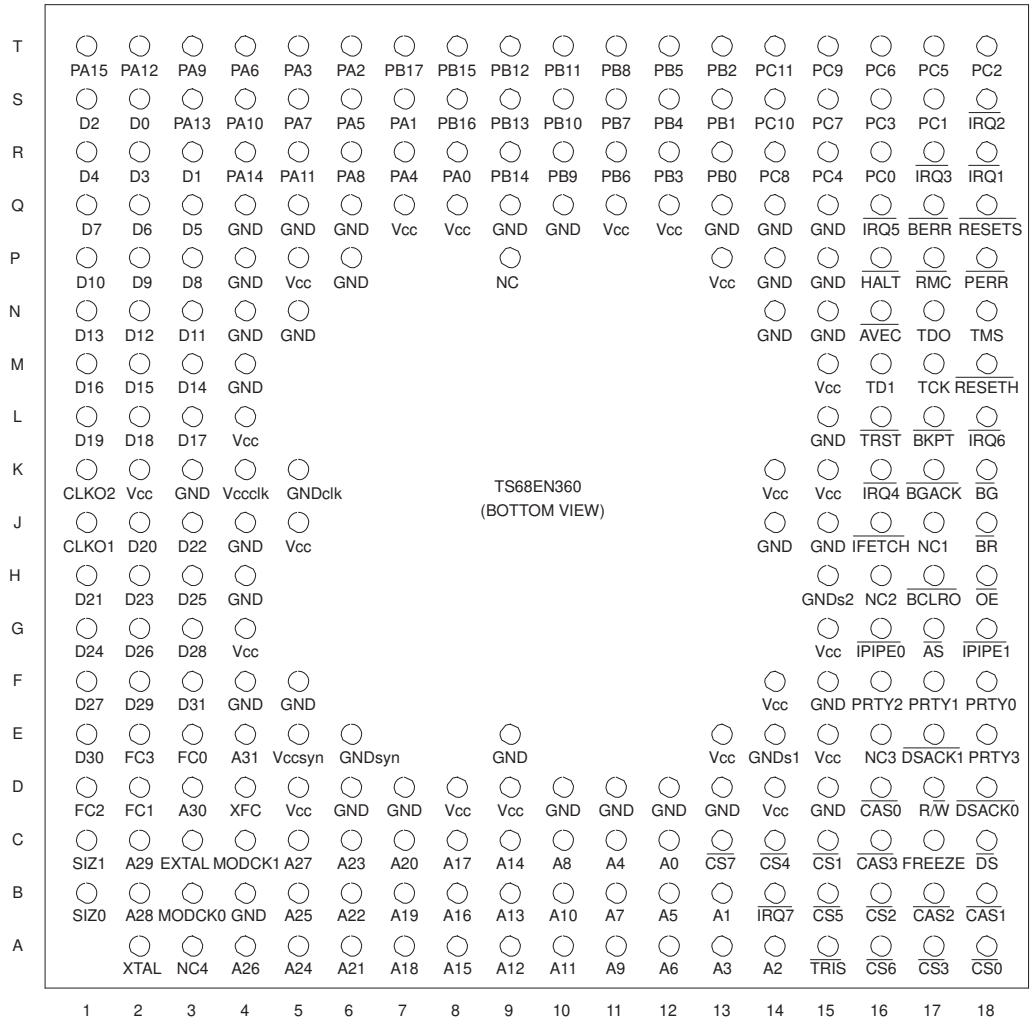
The TS68EN360 QUICC block diagram is shown in Figure 1.

Figure 1. QUICC Block Diagram



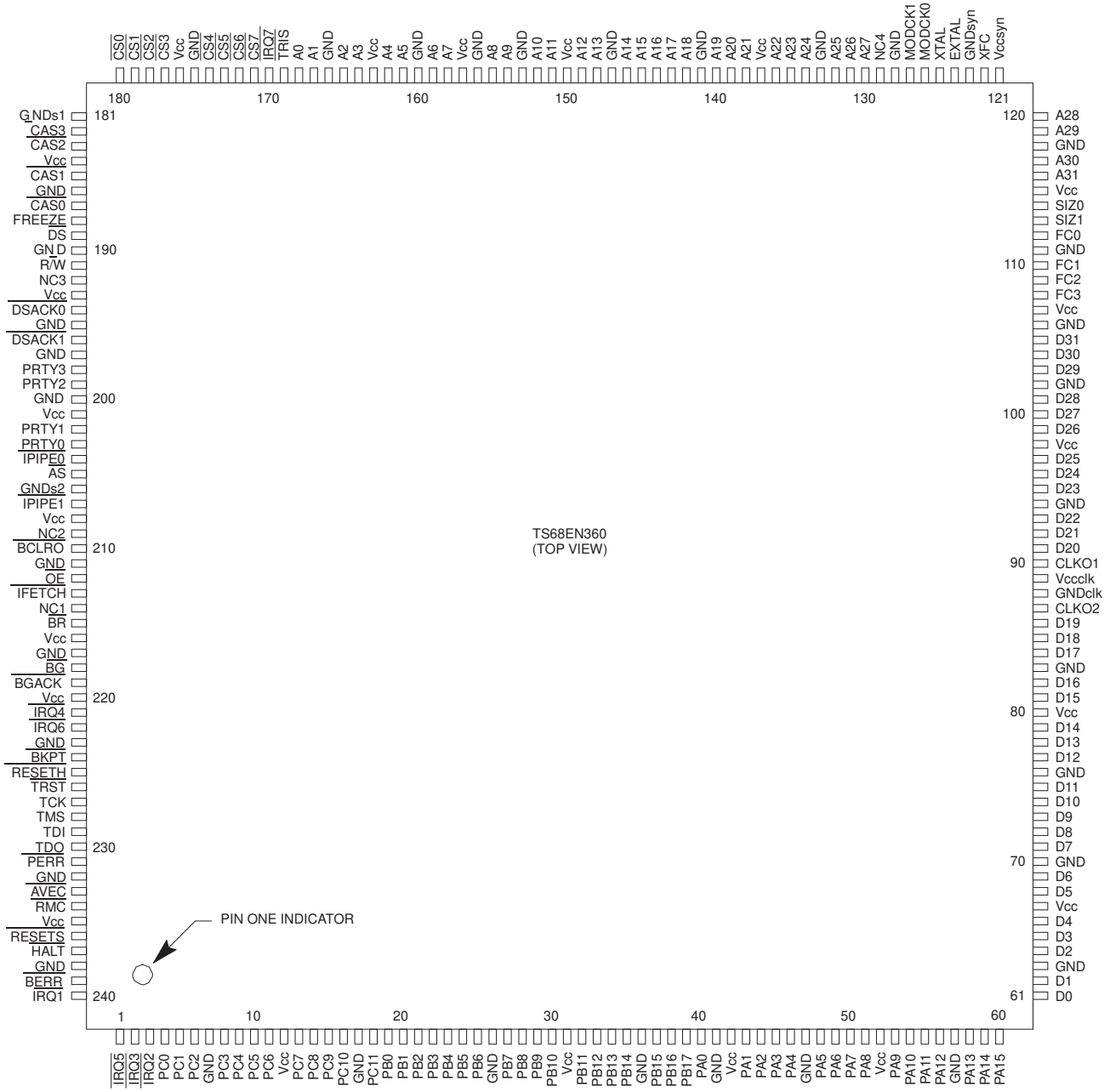
Pin Assignments

Figure 2. 241-lead Pin Grid Array (PGA)



Note: Pin P9 “NC” is for guide purposes only.

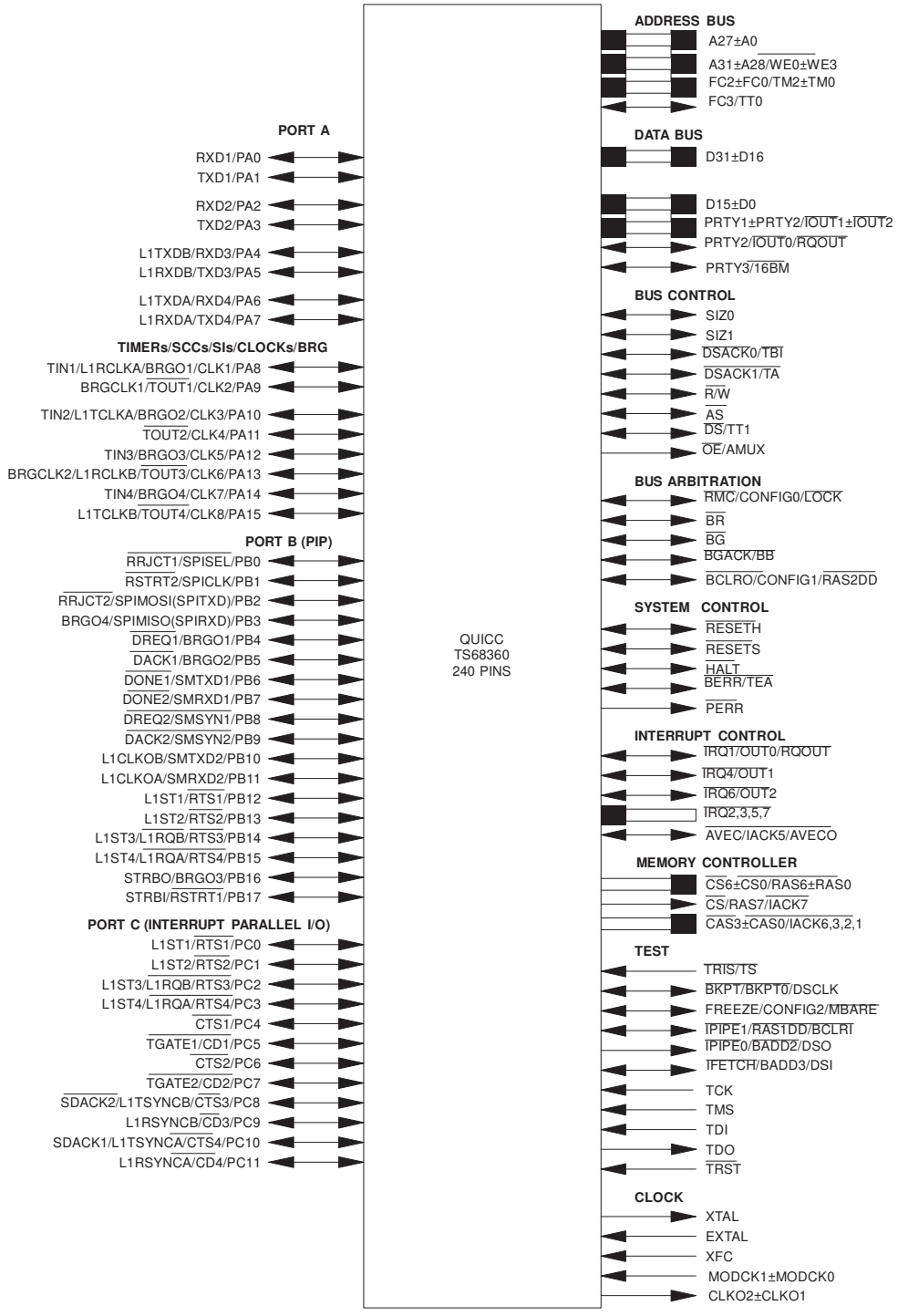
Figure 3. 240-lead Cerquad



Signal Description

Functional Signal Group

Figure 4. QUICC Functional Signal Groups



Signal Index

Table 1. System Bus Signal Index (Normal Operation)

Group	Signal Name	Mnemonic	Function
Address	Address Bus	A27-A0	Lower 27 bits of address bus. (I/O)
	Address Bus/Byte Write Enables	A31-A28 $\overline{\text{WE3-WE0}}$	Upper four bits of address bus (I/O), or byte write enable signals (O) for accesses to external memory or peripherals.
	Function Codes	FC3-FC0	Identifies the processor state and the address space of the current bus cycle. (I/O)
Data	Data Bus 31 - 16	D31-D16	Upper 16-bit data bus used to transfer byte or word data. Used in 16-bit bus mode. (I/O)
	Data Bus 15 - 0	D15-D0	Lower 16-bit data bus used to transfer 3-byte or long-word data. (I/O) Not used in 16-bit bus mode.
Parity	Parity 2 - 0	PRTY2-PRTY0	Parity signals for byte writes/reads from/to external memory module. (I/O)
	Parity 3/$\overline{\text{16BM}}$	PRTY3/$\overline{\text{16BM}}$	Parity signals for byte writes/reads from/to external memory module or defines 16-bit bus mode. (I/O)
	Parity Error	$\overline{\text{PERR}}$	Indicates a parity error during a read cycle. (O)
Memory Controller	Chip Select Row Address Select 7 Interrupt Acknowledge 7	$\overline{\text{CS}}$ $\overline{\text{RAS7}}$ $\overline{\text{IACK7}}$	Enables peripherals or DRAMs at programmed addresses (O) or interrupt level 7 acknowledge line. (O)
	Chip Select 6-0 Row Address Select 6-0	$\overline{\text{CS6-CS0}}$ $\overline{\text{RAS6-RAS0}}$	Enables peripherals or DRAMs at programmed addresses. (O)
	Column Address Select 3 - 0/Interrupt Acknowledge 1, 2, 3, 6	$\overline{\text{CAS3-CAS0}}$/ $\overline{\text{IACK6,3,2,1}}$	DRAM column address select or interrupt level acknowledge lines. (O)
Bus Arbitration	Bus Request	$\overline{\text{BR}}$	Indicates that an external device requires bus mastership. (I)
	Bus Grant	$\overline{\text{BG}}$	Indicates that the current bus cycle is complete and the QUICC has relinquished the bus. (O)
	Bus Grand Acknowledge	$\overline{\text{BGACK}}$	Indicates that an external device has assumed bus mastership. (I)
	Read-Modify-Write Cycle Initial Configuration 0	$\overline{\text{RMC}}$ CONFIG0	Identifies the bus cycle as part of an indivisible read-modify-write operation (I/O) or initial QUICC configuration select. (I)
	Bus Clear Out/Initial Configuration 1/Row Address Select 2 Double-Drive	$\overline{\text{BCLRO}}$/CONFIG1/ $\overline{\text{RAS2DD}}$	Indicates that an internal device requires the external bus (Open-Drain O) or initial QUICC configuration select (I) or row address select 2 double-drive output. (O)

Table 1. System Bus Signal Index (Normal Operation) (Continued)

Group	Signal Name	Mnemonic	Function
Bus Control	Data and Size Acknowledge	DSACK1 - DSACK0	Provides asynchronous data transfer acknowledgement and dynamic bus sizing (open-drain I/O but driven high before three-stated).
	Address Strobe	AS	Indicates that a valid address is on the address bus. (I/O)
	Data Strobe	DS	During a read cycle, DS indicates that an external device should place valid data on the data bus. During a write cycle, DS indicates that valid data is on the data bus. (I/O)
	Size	SIZ1-SIZ0	Indicates the number of bytes remaining to be transferred for this cycle. (I/O)
	Read/Write	R/W	Indicates the direction of data transfer on the bus. (I/O)
	Output Enable Address Multiplex	OE/AMUX	Active during a read cycle indicates that an external device should place valid data on the data bus (O) or provides a strobe for external address multiplexing in DRAM accesses if internal multiplexing is not used. (O)
Interrupt Control	Interrupt Request Level 7-1	IRQ7-IRQ1	Provides external interrupt requests to the CPU32+ at priority levels 7-1. (I)
	Autovector/Interrupt Acknowledge 5	AVEC/IACK5	Autovector request during an interrupt acknowledge cycle (open-drain I/O) or interrupt level 5 acknowledge line. (O)
System Control	Soft Reset	RESETS	Soft system reset. (open-drain I/O)
	Hard Reset	RESETH	Hard system reset. (open-drain I/O)
	Halt	HALT	Suspends external bus activity. (open-drain I/O)
	Bus Error	BERR	Indicates an erroneous bus operation is being attempted. (open-drain I/O)
Clock and Test	System Clock Out 1	CLKO1	Internal system clock output 1. (O)
	System Clock Out 2	CLKO2	Internal system clock output 2 - normally 2x CLKO1. (O)
	Crystal Oscillator	EXTAL, XTAL	Connections for an external crystal to the internal oscillator circuit. EXTAL (I), XTAL (O).
	External Filter Capacitor	XFC	Connection pin for an external capacitor to filter the circuit of the PLL. (I)
	Clock Mode Select 1-0	MODCK1-MODCK0	Selects the source of the internal system clock. (I) THESE PINS SHOULD NOT BE SET TO 00
	Instruction Fetch/ Development Serial Input	IFETCH/DSI	Indicates when the CPU32+ is performing an instruction word prefetch (O) or input to the CPU32+ background debug mode. (I)
	Instruction Pipe 0/ Development Serial Output	IPIPE0/DSO	Used to track movement of words through the instruction pipeline (O) or output from the CPU32+ background debug mode. (O)
	Instruction Pipe 1/Row Address Select 1 Double-Drive	IPIPE1/RAS1DD	Used to track movement of words through the instruction pipeline (O), or a row address select 1 “double-drive” output (O).
	Breakpoint/Development Serial Clock	BKPT/DSCLK	Signals a hardware breakpoint to the QUICC (open-drain I/O), or clock signal for CPU32+ background debug mode (I).
	Freeze/Initial Configuration 2	FREEZE/CONFIG2	Indicates that the CPU32+ has acknowledged a breakpoint (O), or initial QUICC configuration select (I).

Table 1. System Bus Signal Index (Normal Operation) (Continued)

Group	Signal Name	Mnemonic	Function
Clock and Test (Cont'd)	Three-State	$\overline{\text{TRIS}}$	Used to three-state all pins if QUICC is configured as a master. Always Sampled except during system reset. (I)
	Test Clock	TCK	Provides a clock for Scan test logic. (I)
	Test Mode Select	TMS	Controls test mode operations. (I)
	Test Data In	TDI	Serial test instructions and test data signal. (I)
	Test Data Out	TDO	Serial test instructions and test data signal. (O)
	Test Reset	$\overline{\text{TRST}}$	Provides an asynchronous reset to the test controller. (I)
Power	Clock Synthesizer Power	VCCSYN	Power supply to the PLL of the clock synthesizer.
	Clock Synthesizer Ground	GNDSYN	Ground supply to the PLL of the clock synthesizer.
	Clock Out Power	VCCCLK	Power supply to clock out pins.
	Clock Out Ground	GNDCLK	Ground supply to clock out pins.
	Special Ground 1	GNDS1	Special ground for fast AC timing on certain system bus signals.
	Special Ground 2	GNDS2	Special ground for fast AC timing on certain system bus signals.
	System Power Supply and Return	VCC, GND	Power supply and return to the QUICC.
--	No Connect	NC4-NC1	Four no-connect pins.

Note: 1. I denotes input, O denotes output and I/O is input/output.

Table 2. Peripherals Signal Index

Group	Signal Name	Mnemonic	Function
SCC	Receive Data	RXD4-RXD1	Serial receive data input to the SCCs. (I)
	Transmit Data	TXD4-TXD1	Serial transmit data output from the SCCs. (O)
	Request to Send	~~RTS4-RTS1~~	Request to send outputs indicate that the SCC is ready to transmit data. (O)
	Clear to Send	~~CTS4-CTS1~~	Clear to send inputs indicate to the SCC that data transmission may begin. (I)
	Carrier Detect	~~CD4-CD1~~	Carrier detect inputs indicate that the SCC should begin reception of data. (I)
	Receive Start	~~RSTRT1~~	This output from SCC1 identifies the start of a receive frame. Can be used by an Ethernet CAM to perform address matching. (O)
	Receive Reject	RRJCT1	This input to SCC1 allows a CAM to reject the current Ethernet frame after it determines the frame address did not match. (I)
	Clocks	CLK8-CLK1	Input clocks to the SCCs, SCMs, SI, and the baud rate generators. (I)
IDMA	DMA Request	~~DREQ2-DREQ1~~	A request (input) to an IDMA channel to start an IDMA transfer. (I)
	DMA Acknowledge	~~DACK2-DACK1~~	An acknowledgement (output) by the IDMA that an IDMA transfer is in progress. (O)
	DMA Done	~~DONE2-DONE1~~	A bidirectional signal that indicates the last IDMA transfer in a block of data. (I/O)
TIMER	Timer Gate	~~TGATE2-TGATE1~~	An input to a timer that enables/disables the counting function. (I)
	Timer Input	TIN4-TIN1	Time reference input to the timer that allows it to function as a counter. (I)
	Timer Output	~~TOUT4-TOUT1~~	Output waveform (pulse or toggle) from the timer as a result of a reference value being reached. (O)
SPI	SPI Master In Slave Out	SPIMISO	Serial data input to the SPI master (I); serial data output from an SPI slave. (O)
	SPI Master Out Slave In	SPIMOSI	Serial data output from the SPI master (O); serial data input to an SPI slave. (I)
	SPI Clock	SPICLK	Output clock from the SPI master (O); input clock to the SPI slave. (I)
	SPI Select	~~SPISEL~~	SPI slave select input. (I)
SMC	SMC Receive Data	SMRXD2-SMRXD1	Serial data input to the SMCs. (I)
	SMC Transmit Data	SMTXD2-SMTXD1	Serial data output from the SMCs. (O)
	SMC Sync	~~SMSYN2-SMSYN1~~	SMC synchronization signal. (I)

Table 2. Peripherals Signal Index (Continued)

Group	Signal Name	Mnemonic	Function
SI	SI Receive Data	L1RXDA, L1RXDB	Serial input to the time division multiplexed (TDM) channel A or channel B.
	SI Transmit Data	L1TXDA, L1TXDB	Serial output from the TDM channel A or channel B.
	SI Receive Clock	L1RCLKA, L1RCLKB	Input receive clock to TDM channel A or channel B.
	SI Transmit Clock	L1TCLKA, L1TCLKB	Input transmit clock to TDM channel A or channel B.
	SI Transmit Sync Signals	L1TSYNCA, L1TSYNCB	Input transmit data sync signal to TDM channel A or channel B.
	SI Receive Sync Signals	L1RSYNCA, L1RSYNCB	Input receive data sync signal to TDM channel A or channel B.
	IDL Interface Request	L1RQA, L1RQB	IDL interface request to transmit on the D channel. Output from the SI.
	SI Output Clock	L1CLKOA, L1CLKOB	Output serial data rate clock. Can output a data rate clock when the input clock is 2x the data rate.
	SI Data Strobes	L1ST4-L1ST1	Serial data strobe outputs can be used to gate clocks to external devices that do not have a built-in time slot assigner (TSA).
BRG	Baud Rate Generator Out 4-1	BRGO4-BRGO1	Baud rate generator output clock allows baud rate generator to be used externally.
	BRG Input Clock	CLK2, CLK6	Baud rate generator input clock from which BRG will derive the baud rates.
PIP	Port B 15-0	PB15-BP0	PIP Data I/O Pins.
	Strobe Out	STRBO	This input causes the PIP output data to be placed on the PIP data pins.
	Strobe In	STRBI	This input causes data on the PIP data pins to be latched by the PIP as input data.
SDMA	SDMA Acknowledge 2-1	$\overline{\text{SDACK2}}$-$\overline{\text{SDACK1}}$	SDMA output signals used in RISC receiver to mark fields in the Ethernet receive frame.

Scope

This drawing describes the specific requirements for the microcontroller TS68EN360 - 25 MHz and 33 MHz in compliance with MIL-STD-883 class B or Atmel standard screening.

Applicable Documents

MIL-STD-883

1. MIL-STD-883: test methods and procedures for electronics.
2. MIL-PRF-38535: general specifications for microcircuits.
3. DESC 5962-SMD-97607

Requirements

General

This microcircuits are in accordance with the applicable document and as specified herein.

Design and Construction

Terminal Connections

Depending on the package, the terminal connections shall be as shown in Figure 2 and Figure 3.

Lead Material and Finish

Lead material and finish shall be as specified in MIL-STD-883 (see enclosed “Ordering Information” on page 79).

Package

The macrocircuits are packaged in hermetically sealed ceramic packages which are conform to case outlines of MIL-STD-1835 or as follow:

- PGA but see “241-pin – PGA” on page 77
- CERQUAD

The precise case outlines are described at the end of the specification (“Package Mechanical Data” on page 77) and into MIL-STD-1835.

Electrical Characteristics

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage(1)(2)	V_{CC}	-0.3 to +6.5	V
Input Voltage(1)(2)	V_{IN}	-0.3 to +6.5	V
Storage Temperature Range	T_{STG}	-55 to +150	°C

Note: This device contains protective circuitry against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{DD}).

Notes:
1. Permanent damage can occur if maximum ratings are exceeded. Exposure to voltages or currents in excess of recommended values affects device reliability. Device modules may not operate normally while being exposed to electrical extremes.
2. Although sections of the device contain circuitry to protect against damage from high static voltages or electrical fields, take normal precautions to avoid exposure to voltages higher than maximum-rated voltages.
3. The supply voltage V_{CC} must start and restart from 0.0V; otherwise, the 360 will not come out of reset properly.Unless otherwise stated, all voltages are referenced to the reference terminal.

Table 4. Recommended Conditions Of Use
Unless otherwise stated, all voltages are referenced to the reference terminal.

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Range		+4.75		+5.25	V
V_{IL}	Logic Low Level Input Voltage Range		GND		+0.8	V
V_{IH}	Logic High Level Input Voltage Range		+2.0		V_{CC}	V
T_{case}	Operating Temperature		-55		+125	°C
V_{OH}	High Level Output Voltage		+2.4			V
f_{sys}	System Frequency	(For 25 MHz version)		25		MHz
		(For 33 MHz version)		33		MHz

Table 5. Thermal Characteristics

Symbol	Parameter		Value	Unit
θ_{JC}	Thermal Resistance - Junction to Case	240-pin Cerquad	2	°C/W
		241-pin PGA	7	
θ_{JA}	Thermal Resistance - Junction to Ambient	240-pin Cerquad	27.4	°C/W
		241-pin PGA	22.8	

$T_J = T_A + (P_D \cdot \theta_{JA})$

$P_D = (V_{DD} \cdot I_{DD}) + P_{I/O}$

Where $P_{I/O}$ is the power dissipation on pins.

Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A \div (P_D \cdot \Theta_{JA}) \quad (1)$$

where:

T_A = Ambient Temperature, °C

Θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \cdot V_{CC}$, Watts-chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins-User Determined

For most applications, $P_{I/O} < 0.3 \cdot P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving Equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273°C) + \Theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from Equation (3) by measuring P_D (at thermal equilibrium) for a know T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equations (1) and (2) iteratively for any value of T_A.

Mechanical and Environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or for Atmel standard screening.

Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum:

- Atmel logo
- Manufacturer's part number
- Class B identification
- Date-code of inspection lot
- ESD identifier if available
- Country of manufacturing

Quality Conformance Inspection

DESC/MIL-STD-883

Is in accordance with MIL-M-38535 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspections are performed on a periodical basis.

Electrical Characteristics

General Requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below:

- Static electrical characteristics for the electrical variants
- Dynamic electrical characteristics for TS68EN360
  (25 MHz, 33 MHz)

For static characteristics, test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics, test methods refer to clause "Static Characteristics" on page 14 of this specification.

Static Characteristics

GND = 0 V_{dc}, T_C = -55 to +125°C. The electrical specifications in this document are preliminary. (See numbered notes).

Characteristic	Symbol	Min.	Max.	Unit
Input High Voltage (except EXTAL)	V_{IH}	2.0	V_{CC}	V
Input Low Voltage (5V Part)	V_{IL}	GND	0.8	V
Input Low Voltage (Part Only; PA8-15, PB1, PC5, PC7, TCK)	V_{IL}	GND	0.5	V
Input Low Voltage (Part Only; All Other Pins)	V_{IL}	GND	0.8	V
EXTAL Input High Voltage	V_{IHC}	0.8*(V_{CC})	V_{CC} + 0.3	V
Undershoot	-	-	-0.8	V
Input Leakage Current (All Input Only Pins except for TMS, TDI and TRST) Vin = 0/5V	Iin	-2.5	2.5	∝A
Hi-Z (Off-State) Leakage Current (All Noncrystal Outputs and I/O Pins except TMS,TDI and TRST) Vin = 0/5V	I_{OZ}	-2.5	-2.5	∝A
Signal Low Input Current V_{IL} = 0.8V (TMS, TDI and TRST Pins Only) Signal High Input Current V_{IH} = 2.0V (TMS, TDI and TRST Pins Only)	I_L I_H	-0.5 -0.5	0.5 0.5	mA mA
Output High Voltage I_{OH} = -0.8 mA, V_{CC} = 4.75V All Noncrystal Outputs Except Open Drain Pins	V_{OH}	2.4	-	V
Output Low Voltage I_{OL} = 2.0 mA, CLKO1-2, FREEZE, ~~IPIPE0-1~~, ~~IFETCH~~, ~~BKPTO~~ I_{OL} = 3.2 mA, A31-A0, D31-D0, FC3-0, SIZ0-1, PA0, 2, 4, 6, 8-15, PB0-5, PB8-17, PC0-11, TDO, ~~PERR~~, PRTY0-3, ~~IOUT0-2~~, AVECO, AS, ~~CAS3-0~~, ~~BLCRO~~, ~~RAS0-7~~ I_{OL} = 5.3 mA, ~~DSACK0-1~~, R/~~W~~, ~~DS~~, ~~OE~~, ~~RMC~~, ~~BG~~, ~~BGACK~~, ~~BERR~~ I_{OL} = 7 mA, TXD1-4 I_{OL} = 8.9 mA, PB6, PB7, ~~HALT~~, ~~RESET~~, ~~BR~~ (Output)	V_{OL}	-	0.5 0.5 0.5 0.5 0.5	V
Input Capacitance All I/O Pins	Cin	-	20	pF
Load Capacitance (except CLKO1-2)	C_L	-	100	pF
Load Capacitance (CLKO1-2)	C_Lc		50	pF
Power	V_{CC}	4.75	5.25	V

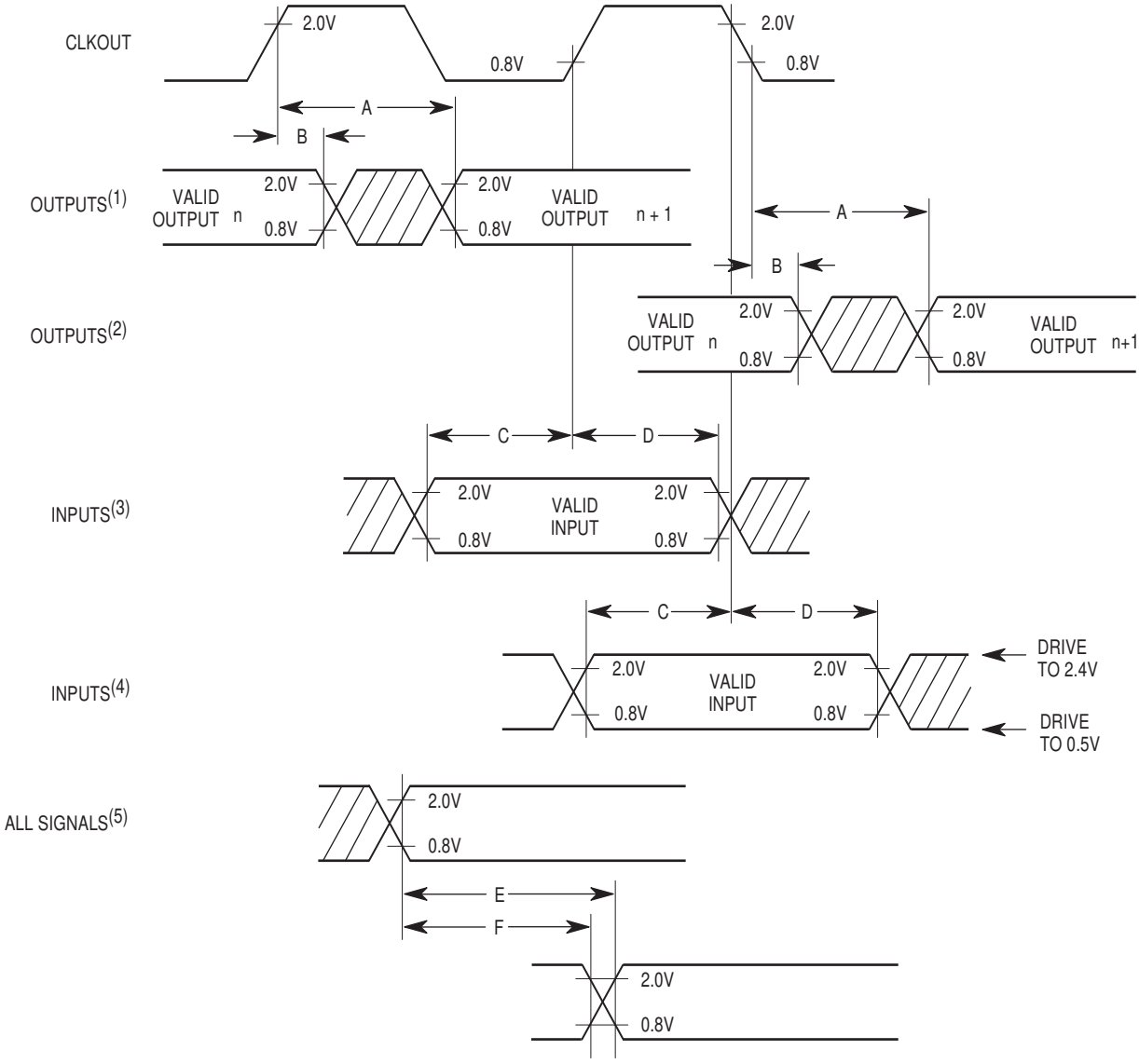
Dynamic Characteristics

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clock and possibly to one or more other signals.

The measurement of the AC specifications is defined by the waveforms shown in Figure 5. To test the parameters guaranteed by Atmel inputs must be driven to the voltage levels specified in the figure. Outputs are specified with minimum and/or maximum limits, as appropriate, and are measured as shown. Inputs are specified with minimum setup and hold times and are measured as shown. Finally, the measurement for signal-to-signal specifications are shown.

Note that the testing levels used to verifyconformance to the AC specifications do not affect the guaranteed DC operation of the device as specified in the DC electrical characteristics.

Figure 5. Drive Levels and Test Points For AC Specifications



Notes:
1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This output timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the rising edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

Legend:

a) Maximum output delay specification.

b) Minimum output hold time.

c) Minimum input setup time specification.

d) Minimum input hold time specification.

e) Signal valid to signal valid specification (maximum or minimum).

f) Signal valid to signal invalid specification (maximum or minimum).

AC Power Dissipation

Table 6. Typical Current Drain

Mode of Operation	Symbol	System Clock Frequency	BRGCLK Clock Frequency	SyncCLK Clock Frequency	Typ	Unit
Normal mode (Rev A[1] and Rev B[2])	I_{DD}	25 MHz	25 MHz	25 MHz	250	mA
Normal Mode (Rev C[3] and Newer)	I_{DD}	25 MHz	25 MHz	25 MHz	237	mA
Normal Mode	I_{DD}	33 MHz	33 MHz	33 MHz	327	mA
Low Power Mode	I_{DDSB}	Divide by 2 12.5 MHz	Divide by 16 1.56 MHz	Divide by 2 12.5 MHz	150	mA
Low Power Mode	I_{DDSB}	Divide by 4 6.25 MHz	Divide by 16 1.56 MHz	Divide by 4 6.25 MHz	85	mA
Low Power Mode	I_{DDSB}	Divide by 16 1.56 MHz	Divide by 16 1.56 MHz	Divide by 4 6.25 MHz	35	mA
Low Power Mode	I_{DDSB}	Divide by 256 97.6 kHz	Divide by 16 1.56 MHz	Divide by 4 6.25 MHz	20	mA
Low Power Mode	I_{DDSB}	Divide by 256 97.6 kHz	Divide by 64 390 kHz	Divide by 64 390 kHz	13	mA
Low Power Stop VCO Off[4]	I_{DDSP}				0.5	mA
PLL Supply Current PLL Disabled PLL Enabled	 I_{DDPD} I_{DDPE}				 TBD TBD	

Notes: 1. Rev A mask is C63T
2. Rev B masks are C69T and F35G
3. Current Rev C masks are E63C, E68C and F15W
4. EXTAL frequency is 32 kHz

All measurements were taken with only CLKO1 enabled, V_{CC} = 5.0V, V_{IL} = 0V and V_{IH} = V_{CC}

Table 7. Maximum Power Dissipation

System Frequency	V_{CC}	Max P_D	Unit	Mask
25 MHz	5.25V	1.80	W	REV A[1] and REV B[2]
25 MHz	5.25V	1.45	W	REV C[3] and Newer
25 MHz	3.6V	0.65	W	REV C[3] and Newer
33 MHz	5.25V	2.00	W	REV C[3] and Newer

Notes: 1. Rev A mask is C63T
2. Rev B masks are C69T and F35G
3. Current Rev C masks are E63C, E68C and F15W

AC Electrical Specifications Control Timing

GND = 0 Vdc, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 6).

Number	Characteristic	Symbol	25 MHz		33.34 MHz		Unit
			Min	Max	Min	Max	
	System Frequency	f_{sys}	dc(1)	25.00		33.34	MHz
	Crystal Frequency	f_{XTAL}	25	6000	25	6000	kHz
	On-Chip VCO System Frequency	f_{sys}	20	50	20	67	MHz
	Start-up Time With external clock (oscillator disabled) or after changing the multiplication factor MF	t_{pll}		2500			clks
	CLKO1-2 stability	$\square_{CLK}$	TBD	TBD			%
1	CLKO1 Period	t_{cyc}	40	-	30	-	ns
1A	EXTAL Duty Cycle, MF	t_{dcyc}	40	60	40	60	%
1C	External Clock Input Period	t_{EXTcyc}	40	-	30	-	ns
2, 3	CLKO1 Pulse Width (Measured at 1.5V)	t_{CW1}	19	-	14	-	ns
2A, 3A	CLKO2 Pulse Width (Measured at 1.5V)	t_{CW2}	9.5	-	7	-	ns
4, 5	CLKO1 Rise and Fall Times (Full drive)	t_{Crf1}	-	2	-	2	ns
4A, 5A	CLKO2 Rise and Fall Times (Full drive)	t_{Crf2}	-	2	-	1.6	ns
5B	EXTAL to CLKO1 Skew-PLL enabled (MF< 5)	t_{EXTP1}		a		a	ns
5C	EXTAL to CLKO2 Skew-PLL enabled (MF< 5)	t_{EXTP2}		a		a	ns
5D	CLKO1 to CLKO2 Skew	$Atmel_{KW}$		a		a	ns

Note: 1. Note that the minimum VCO frequency and the PLL default values put some restrictions on the minimum system frequency.

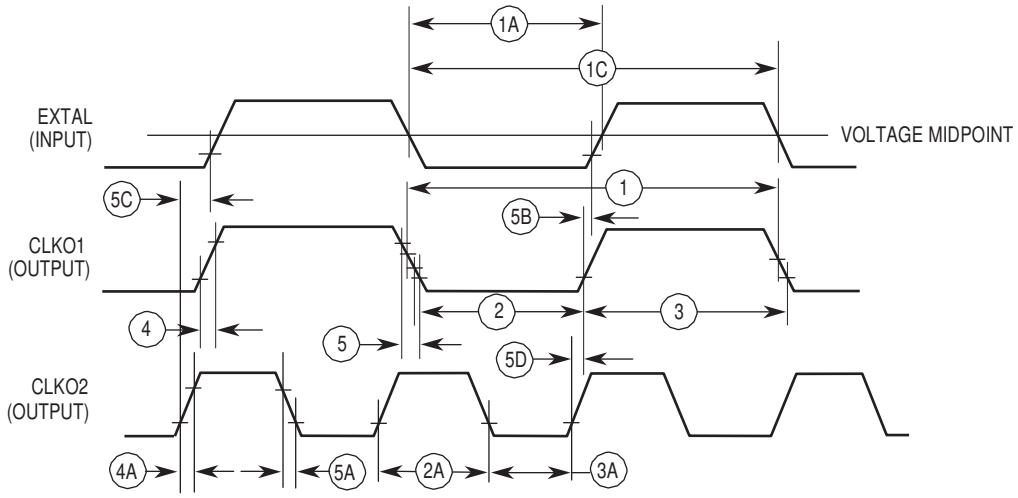
The following calculation should be used to determine the actual value for specifications 5B, 5C and 5D.

5B: 25 MHz ±(0.9 ns + 0.25 x (rise time)) (1.4 ns @ rise = 2 ns; 1.9 ns @ rise = 4 ns)
33 MHz ±(0.5 ns + 0.25 x (rise time)) (1 ns @ rise = 2 ns; 1.5 ns @ rise = 4 ns)

5C: 25/33 MHz ±(2 ns + 0.25 x (rise time)) (2.5 ns @ rise = 2 ns; 3 ns @ rise = 4 ns)

5D: 25 MHz ±(3 ns + 0.5 x (rise time)) (4 ns @ rise = 2 ns; 5 ns @ rise = 4 ns)
33 MHz ±(2.5 ns + 0.5 x (rise time)) (3.5 ns @ rise = 2 ns; 4.5 ns @ rise = 4 ns)

Figure 6. Clock Timing



External Capacitor For PLL

GND = 0 Vdc, T_C = -55 to +125°C. The electrical specifications in this document are preliminary.

Characteristic	Symbol	Min	Max	Unit
PLL External Capacitor (XFC to VCCSYN)	C_{XFC}			
MF< 5 (Recommended value MF x 400 pF)(1)		MF x 340	MF x 480	pF
MF> 4 (Recommended value MF x 540 pF)(1)		MF x 380	MF x 970	pF

Note: 1. MF - multiplication factor.

Examples:

Notes:
1. MODCK1 pin = 0, MF = 1 ⇒ C_{XFC} = 400 pF
2. MODCK1 pin = 1, crystal is 32.768 kHz (or 4.192 MHz), initial MF = 401, initial frequency = 13.14 MHz, later on MF is changed to 762 to support a frequency of 25 MHz. Minimum C_{XFC} is: 762 x 380 = 289 nF, Maximum C_{XFC} is: 401 x 970 = 390 nF. The recommended C_{XFC} for 25 MHz is: 762 x 540 = 414 nF. 289 nF < C_{XFC} < 390 nF and closer to 414 nF. The proper available value for C_{XFC} is 390 nF.
3. MODCK1 pin = 1, crystal is 32.768 kHz (or 4.192 MHz), initial MF = 401, initial frequency = 13.14 MHz, later on MF is changed to 1017 to support a frequency of 33.34 MHz. Minimum C_{XFC} is: 1017 x 380 = 386 nF, Maximum C_{XFC} is: 401 x 970 = 390 nF ⇒ 386 nF < C_{XFC} < 390 nF. The proper available value for C_{XFC} is 390 nF.
4. In order to get higher range, higher crystal frequency can be used (i.e. 50 kHz), in this case:
   Minimum C_{XFC} is: 667 x 380 = 253 nF, Maximum C_{XFC} is: 401 x 970 = 390 nF ⇒ 386 nF < C_{XFC} < 390 nF.

Bus Operation AC Timing Specifications

GND = 0 Vdc, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7 to Figure 23).

Number	Characteristic	Symbol	25 MHz		33.34 MHz		Unit
			Min	Max	Min	Max	
6	CLKO1 High to Address, FC, SIZ, RMC Valid	t_{CHAV}	0	15	0	12	ns
6A	CLKO1 High to Address Valid (GAMX = 1)	t_{CHAV}	0	20	0	15	ns
7	CLKO1 High to Address, Data, FC, SIZ, RMC High Impedance	t_{CHAZx}	0	40	0	30	ns
8	CLKO1 High to Address, Data, FC, SIZ, RMC Invalid	t_{CHAZn}	-2	-	-2	-	ns
9	CLKO1 Low to AS, DS, OE, WE, IFETCH, IPIPE, IACKx Asserted	t_{CLSA}	3	20	3	15	ns
9(10)	CLKO1 Low to CSx/RASx Asserted	t_{CLSA}	4	16	4	12	ns
9B(11)	CLKO1 High to CSx/RASx Asserted	t_{CHCA}	4	16	4	12	ns
9A(2)(10)	AS to DS or CSx/RASx or OE Asserted (Read)	t_{STSA}	-6	6	-5.625	5.625	ns
9C(2)(11)	AS to CSx/RASx Asserted	t_{STCA}	14	26	9	21	ns
11(10)	Address, FC, SIZ, RMC, valid to AS, CSx/RASx, OE, WE, (and DS Read) Asserted	t_{AVSA}	10	-	8	-	ns
11A(11)	Address, FC, SIZ, RMC, Valid to CSx/RASx Asserted	t_{AVCA}	30	-	22.5	-	ns
12	CLKO1 Low to AS, DS, OE, WE, IFETCH, IPIPE, IACKx Negated	t_{CLSN}	3	20	3	15	ns
12(16)	CLKO1 Low to CSx/RASx Negated	t_{CLSN}	4	16	4	12	ns
12A(13)(16)	CLKO1 High to CSx/RASx Negated	t_{CHCN}	4	16	4	12	ns
12B	CS negate to WE negate (CSNTQ = 1)	t_{TW}	15	-	12	-	ns
13(12)	AS, DS, CSx, OE, WE, IACKx Negated to Address, FC, SIZ Invalid (Address Hold)	t_{SNAI}	10	-	7.5	-	ns
13A(13)	CSx Negated to Address, FC, SIZ, Invalid (Address Hold)	t_{CNAI}	30	-	22.5	-	ns
14(10)(12)	AS, CSx, OE, WE (and DS Read) Width Asserted	t_{SWA}	75	-	56.25	-	ns
14C(11)(13)	CSx Width Asserted	t_{CWA}	35	-	26.25	-	ns
14A	DS Width Asserted (Write)	t_{SWAW}	35	-	26.25	-	ns
14B	AS, CSx, OE, WE, IACKx, (and DS Read) Width Asserted (Fast Termination Cycle)	t_{SWDW}	35	-	26.25	-	ns
14D(13)	CSx Width Asserted (Fast Termination Cycle)	t_{SWDW}	15	-	10	-	ns
15(3)(10)(12)	AS, DS, CSx, OE, WE Width Negated	t_{SN}	35	-	26.25	-	ns
16	CLKO1 High to AS, DS, R/W High Impedance	t_{CHSZ}	-	40	-	30	ns
17(12)	AS, DS, CSx, WE Negated to R/W High	t_{SNRN}	10	-	7.5	-	ns
17A(13)	CSx Negated to R/W High	t_{CNRN}	30	-	22.5	-	ns
18	CLKO1 High to R/W High	t_{CHRH}	0	20	0	15	ns

Bus Operation AC Timing Specifications (Continued)

GND = 0 Vdc, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7 to Figure 23).

Number	Characteristic	Symbol	25 MHz		33.34 MHz		Unit
			Min	Max	Min	Max	
20	CLKO1 High to R/$\overline{W}$ Low	t_{CHRL}	3	20	3	15	ns
21[10]	R/$\overline{W}$ High to $\overline{AS}$, $\overline{CSx}$, $\overline{OE}$ Asserted	t_{RAAA}	10	-	7.5	-	ns
21A[11]	R/$\overline{W}$ High to $\overline{CSx}$ Asserted	t_{RACA}	30	-		-	ns
22	R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write)	t_{RASA}	47	-	36	-	ns
23	CLKO1 High to Data-Out	t_{CHDO}	-	23	-	18	ns
23A	CLKO1 High to Parity Valid	t_{CHPV}	-	25	-	20	ns
23B	Parity Valid to $\overline{CAS}$ Low	t_{PVCL}	3	-	3	-	ns
24[12]	Data-Out, Parity-Out Valid to Negating Edge of $\overline{AS}$, $\overline{CSx}$, $\overline{WE}$, (Fast Termination Write)	t_{DVASN}	10	-	7.5	-	ns
25[12]	$\overline{DS}$, $\overline{CSX}$, $\overline{WE}$ Negated to Data-Out, Parity-Out Invalid (Data-Out, Parity-Out Hold)	t_{SNDOI}	10	-	7.5	-	ns
25A[13]	$\overline{CSx}$ Negated to Data-Out, Parity-Out Invalid (Data-Out, Parity-Out Hold)	t_{CNDOI}	35	-	25	-	ns
26	Data-Out, Parity-Out Valid to $\overline{DS}$ Asserted (Write)	t_{DVSA}	10	-	7.5	-	ns
27[15]	Data-In, Parity-In to CLKO1 Low (Data-Setup)	t_{DICL}	1	-	1	-	ns
27B[14]	Data-In, Parity-In Valid to CLKO1 Low (Data-Setup)	t_{DICL}	20	-	15	-	ns
27A	Late $\overline{BERR}$, $\overline{HALT}$, $\overline{BKPT}$ Asserted to CLKO1 Low (Setup Time)	t_{BELCL}	10	-	7.5	-	ns
28[18]	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DSACKx}$, $\overline{BERR}$, $\overline{HALT}$ Negated	t_{SNDN}	0	50	0	37.5	ns
29[4]	$\overline{DS}$, $\overline{CSx}$, $\overline{OE}$, Negated to Data-In Parity-In Invalid (Data-In, Parity-In Hold)	t_{SNDI}	0	-	0	-	ns
29A[4]	$\overline{DS}$, $\overline{CSx}$, $\overline{OE}$ Negated to Data-In High Impedance	t_{SHDI}	-	40	-	30	ns
30[4]	CLKO1 Low to Data-In, Parity-In Invalid (Fast Termination Hold)	t_{CLDI}	10	-	7.5	-	ns
30A[4]	CLKO1 Low to Data-In High Impedance	t_{CLDH}	-	60	-	45	ns
31[5][15]	$\overline{DSACKx}$ Asserted to Data-in, Parity-In Valid	t_{DADI}	-	32	-	24	ns
31A	$\overline{DSACKx}$ Asserted to $\overline{DSACKx}$ Valid (Skew)	t_{DADV}	-	10	-	7.5	ns
31B[5][14]	$\overline{DSACKx}$ Asserted to Data-in, Parity-In Valid	t_{DADI}	-	35	-	26	ns
32	$\overline{HALT}$ an $\overline{RESET}$ Input Transition Time	t_{HRrf}	-	140	-		ns
33	CLKO1 High to $\overline{BG}$ Asserted	t_{CLBA}	-	20	-	15	ns
34	CLKO1 High to $\overline{BG}$ Negated	t_{CLBN}	-	20	22.5	15	ns
35[6]	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted ($\overline{RMC}$ Not Asserted)	t_{BRAGA}	1	-	1	-	CLKO1
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	t_{GAGN}	1	2.5	1	2.5	CLKO1
39	$\overline{BG}$ Width Negated	t_{GH}	2	-	2	-	CLKO1
39A	$\overline{BG}$ Width Asserted	t_{GA}	1	-	1	-	CLKO1

Bus Operation AC Timing Specifications (Continued)

GND = 0 Vdc, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7 to Figure 23).

Number	Characteristic	Symbol	25 MHz		33.34 MHz		Unit
			Min	Max	Min	Max	
46	R/$\overline{W}$ Width Asserted (Write or Read)	t_{RWA}	100	-	75	-	ns
46A	R/$\overline{W}$ Width Asserted (Fast Termination Write or Read)	t_{RWAS}	75	-	56	-	ns
47A	Asynchronous Input Setup Time	t_{AIST}	5	-	4	-	ns
47B	Asynchronous Input Hold Time	t_{AIHT}	10	-	7.5	-	ns
48(5)(7)	$\overline{DSACKx}$ Asserted to $\overline{BERR}$, $\overline{HALT}$ Asserted	t_{DABA}	-	30	-	22.5	ns
53	Data-Out, Parity-Out Hold from CLKO1 High	t_{DOCH}	0	-	0	-	ns
54	CLKO1 High to Dat-Out, Parity-Out High Impedance	t_{CHDH}	-	20	-	15	ns
55	R/$\overline{W}$ Asserted to Data Bus Impedance Change	t_{RADC}	25	-	19	-	ns
56	$\overline{RESET}$ Pulse Width (Reset Instruction)	t_{HRPW}	512	-	512	-	CLKO1
56A	$\overline{RESET}$ Pulse Width (Input from External Device)	t_{RPWI}	20	-	20	-	CLKO1
57	$\overline{BERR}$ Negated to $\overline{HALT}$ Negated (Return)	t_{BNHN}	0	-	0	-	ns
58	CLKO1 High to $\overline{BERR}$, $\overline{RESETS}$, $\overline{RESETH}$ Driven Low	t_{CHBRL}	-	30		26	ns
58A	CLKO1 Low $\overline{RESETS}$ Driven Low (upon Reset Instruction execution only)	t_{CLRL}	-	30		26	ns
58B	CLKO1 High to BERR, RESETS, RESETH tri-stated	t_{CLRL}	-	20	-	15	ns
60	CLKO1 High to $\overline{BCLRO}$ Asserted	t_{CHBCA}	-	20	-	15	ns
61	CLKO1 High to $\overline{BCLRO}$ Negated	t_{CHBCN}	-	20	-	15	ns
62(9)	$\overline{BR}$ Synchronous Setup Time	t_{BRSU}	5	-	3.75	-	ns
63(9)	$\overline{BR}$ Synchronous Hold Time	t_{BRH}	10	-	7.5	-	ns
64(9)	$\overline{BGACK}$ Synchronous Setup Time	t_{BGSU}	5	-	3.75	-	ns
65(9)	$\overline{BGACK}$ Synchronous Hold Time	t_{BGH}	10	-	7.5	-	ns
66	$\overline{BR}$ Low to CLKO1 Rising Edge (040 comp. mode)	t_{BRCH}	5	-	5	-	ns
70	CLKO1 Low to Data Bus Driven (Show Cycle)	t_{SCLDD}	0	30	0	22.5	ns
71	Data Setup Time to CLKO1 Low (Show Cycle)	t_{SCLDS}	10	-	7.5	-	ns
72	Data Hold from CLKO1 Low (Show Cycle)	t_{SCLDH}	6	-	3.75	-	ns
73	$\overline{BKPT}$ Input Setup Time	t_{BKST}	10	-	7.5	-	ns
74	$\overline{BKPT}$ Input Hold Time	t_{BKHT}	6	-	3.75	-	ns
75	$\overline{RESETH}$ Low to Config2-0, MOD1-0, B16M Valid	t_{MST}	-	500	-	500	CLKO1
76	Config2-0	t_{MSH}	0	-	0	-	ns
77	MOD1-0 Hold Time, B16M Hold Time	t_{MSH}	10	-	10	-	CLKO1
80	DSI Input Setup Time	t_{DSISU}	10	-	7.5	-	ns

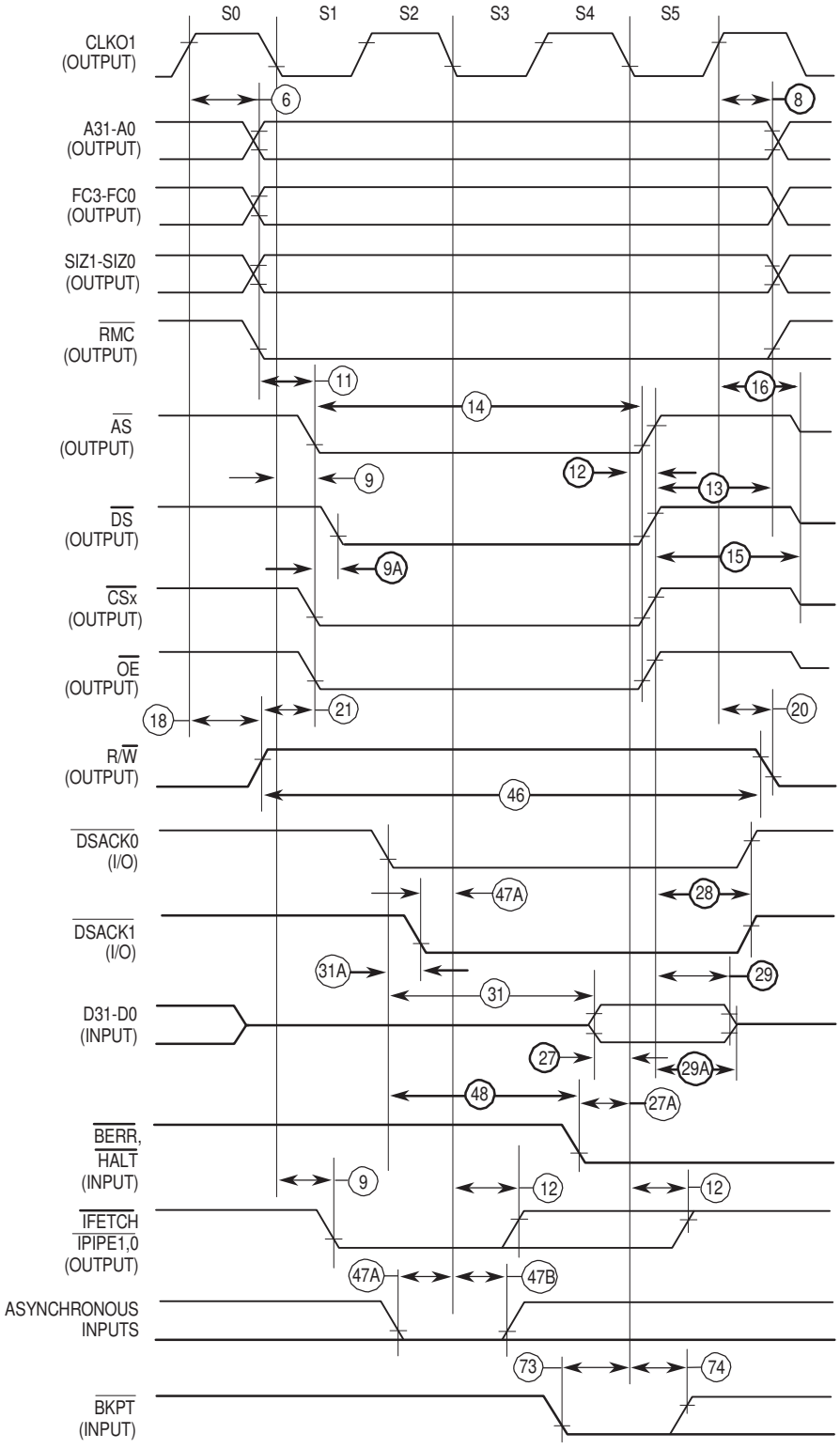
Bus Operation AC Timing Specifications (Continued)

GND = 0 Vdc, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7 to Figure 23).

Number	Characteristic	Symbol	25 MHz		33.34 MHz		Unit
			Min	Max	Min	Max	
81	DSI Input Hold Time	t_{DSIH}	6	-	3.75	-	ns
82	DSCLC Setup Time	t_{DSCSU}	10	-	7.5	-	ns
83	DSCLC Hold Time	t_{DSCH}	6	-	3.75	-	ns
84	DSO Delay Time	t_{DSOD}	-	tcyc+20	-	tcyc+20	ns
85	DSCLK Cycle	t_{DSCCYC}	2	-	2	-	CLKO1
86	CLKO1 High to Freeze Asserted	t_{FRZA}	0	35	0	26.25	ns
87	CLKO1 High to Freeze Negated	t_{FRZN}	0	35	0	26.25	ns
88	CLKO1 High to $\overline{IFETCH}$ High Impedance	t_{IFZ}	0	35	0	26.25	ns
89	CLKO1 High to $\overline{IFETCH}$ Valid	t_{IF}	0	35	0	26.25	ns
90	CLKO1 High to $\overline{PERR}$ Asserted	t_{CHPA}	0	20	0	15	ns
91	CLKO1 High to $\overline{PERR}$ Negated	t_{CHPN}	0	20	0	15	ns
92	V_{CC} Ramp-Up Time At Power-On Reset	t_{RMIN}	5	-	5	-	ns

Notes:
1. All AC timing is shown with respect to 0.8V and 2.0V levels unless otherwise noted.
2. This number can be reduced to 5 ns if strobes have equal loads.
3. If multiple chip selects are used, the $\overline{CSx}$ width negated (#15) applies to the time from the negation of a heavily loaded chip select to the assertion of a lightly loaded chip select.
4. Hold times are specified with respect to $\overline{DS}$ or $\overline{CSx}$ on asynchronous reads and with respect to CLKO1 on fast termination reads. The user is free to use either hold time for fast termination reads.
5. If the asynchronous setup (#17) requirements are satisfied, the $\overline{DSACKx}$ low to data setup time (#31) and $\overline{DSACKx}$ low to $\overline{BERR}$ low setup time (#48) can be ignored. The data must only satisfy the data-in to CLKO1 low setup time (#27) for the following clock cycle: $\overline{BERR}$ must only satisfy the late $\overline{BERR}$ low to CLKO1 low setup time (#27A) for the following clock cycle.
6. To ensure coherency during every operand transfer, $\overline{BG}$ will not be asserted in response to $\overline{BR}$ until after cycles of the current operand transfer are complete and $\overline{RMC}$ is negated.
7. In the absence of $\overline{DSACKx}$, $\overline{BERR}$ is an asynchronous input using the asynchronous setup time (#47).
8. During interrupt acknowledge cycles, the processor may insert up to two wait states between states S0 and S1.
9. Specs are for Synchronous Arbitration only. ASTM = 1.
10. $\overline{CSx}$ specs are for TRLX = 0.
11. $\overline{CSx}$ specs are for TRLX = 1.
12. $\overline{CSx}$ specs are for CSNTQ = 0.
13. $\overline{CSx}$ specs are for CSNTQ = 1; or $\overline{RASx}$ specs for DRAM accesses.
14. Specs are read cycles with parity check and PBEE = 1.
15. Specs are read cycles with parity check and PBEE = 0, PAREN = 1.
16. $\overline{RASx}$ specs are for page miss case.
17. Specifications only apply to $\overline{CSx}$/$\overline{RASx}$ pins.
18. Specification applies to non fast termination cycles. In fast termination cycles, the $\overline{BERR}$ signal must be negated by 20 ns after negation of $\overline{AS}$, $\overline{DS}$.

Figure 7. Read Cycle



Note: All timing is shown with respect to 0.8V and 2.0V levels.

Figure 8. Fast Termination Read Cycle (Parity Check PAREN = 1, PBEE = 0)

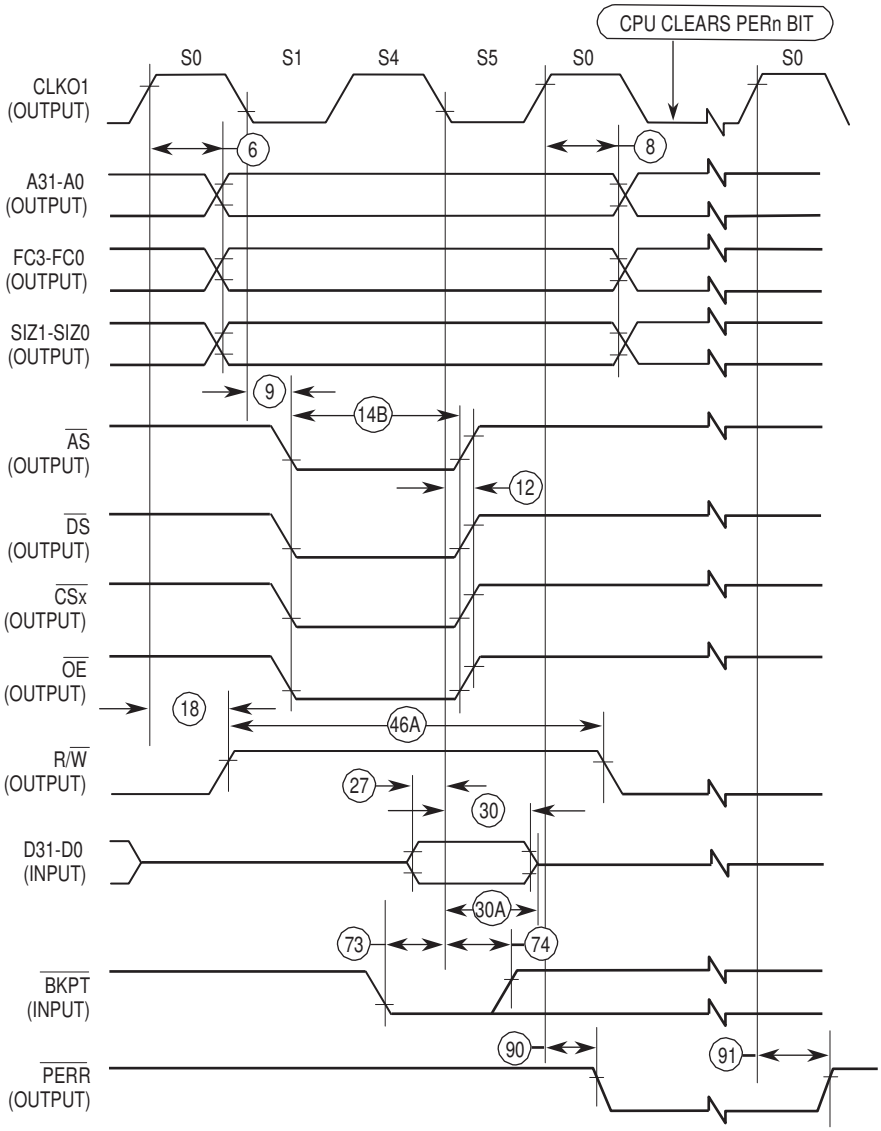
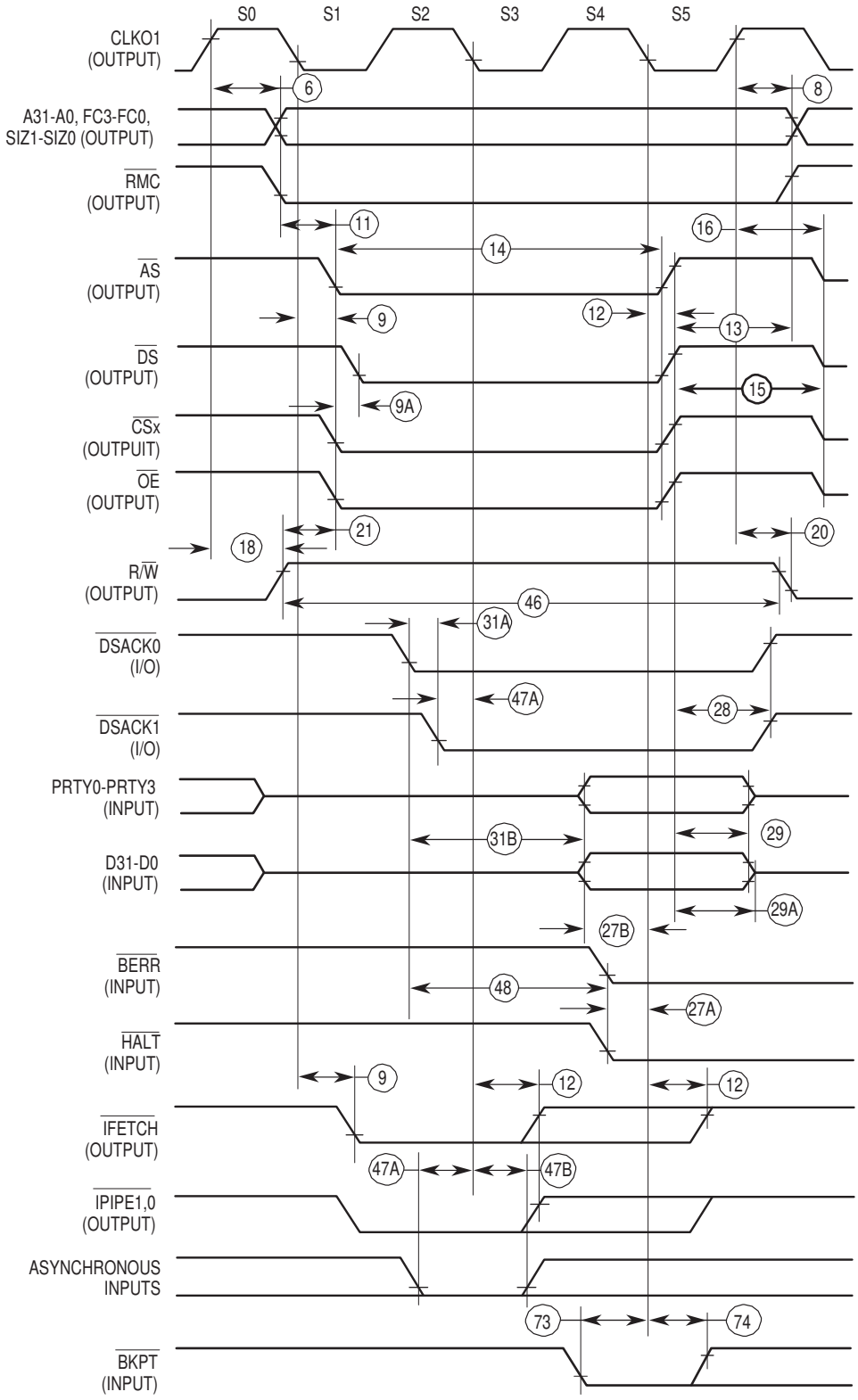


Figure 9. Read Cycle (With Parity Check, PBEE = 1)



Note: All timing is shown with respect to 0.8V and 2.0V levels.