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## Features

- 80C52 Compatible
  - 8051 Pin and Instruction Compatible
  - Four 8-bit I/O Ports
  - Three 16-bit Timer/Counters
  - 256 Bytes Scratchpad RAM
- High-speed Architecture
- 40 MHz at 5V, 30 MHz at 3V
- X2 Speed Improvement Capability (6 Clocks/Machine Cycle)
  - 30 MHz at 5V, 20 MHz at 3V (Equivalent to 60 MHz at 5V, 40 MHz at 3V)
- Dual Data Pointer
- On-chip ROM/EPROM (8Kbytes)
- Programmable Clock Out and Up/Down Timer/Counter 2
- Asynchronous Port Reset
- Interrupt Structure with
  - 6 Interrupt Sources
  - 4 Level Priority Interrupt System
- Full Duplex Enhanced UART
  - Framing Error Detection
  - Automatic Address Recognition
- Low EMI (Inhibit ALE)
- Power Control Modes
  - Idle Mode
  - Power-down Mode
  - Power-off Flag
- Once Mode (On-chip Emulation)
- Power Supply: 4.5 - 5.5V, 2.7 - 5.5V
- Temperature Ranges: Commercial (0 to 70°C) and Industrial (-40 to 85°C)
- Packages: PDIL40, PLCC44, VQFP44 1.4, PQFP44 (13.9 footprint)

## Description

TS80C52X2 is high performance CMOS ROM, OTP, EPROM and ROMless versions of the 80C51 CMOS single chip 8-bit microcontroller.

The TS80C52X2 retains all features of the 80C51 with extended ROM/EPROM capacity (8 Kbytes), 256 bytes of internal RAM, a 6-source, 4-level interrupt system, an on-chip oscillator and three timer/counters.

In addition, the TS80C52X2 has a dual data pointer, a more versatile serial channel that facilitates multiprocessor communication (EUART) and an X2 speed improvement mechanism.

The fully static design of the TS80C52X2 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The TS80C52X2 has 2 software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the timers, the serial port and the interrupt system are still operating. In the power-down mode the RAM is saved and all other functions are inoperative.



**8-bit  
Microcontroller  
8 Kbytes  
ROM/OTP,  
ROMless**

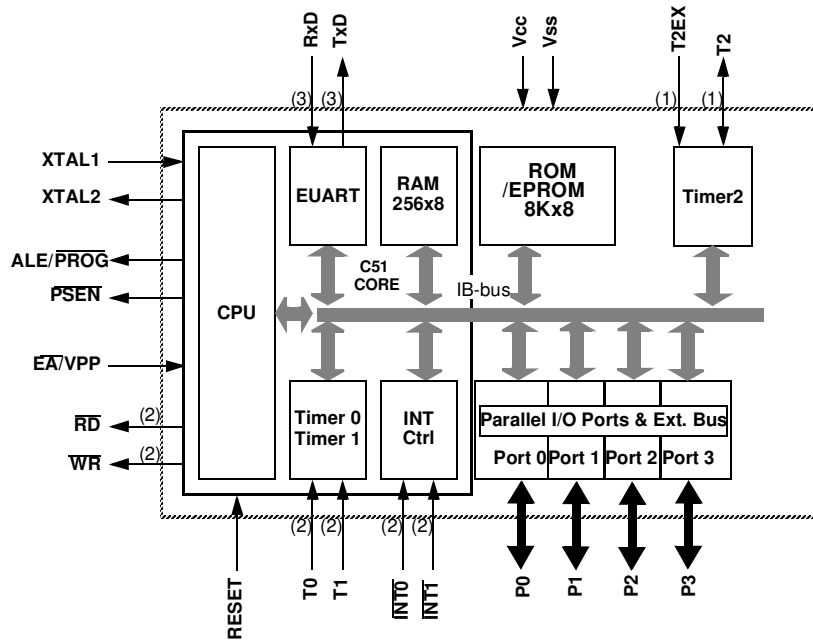
**TS80C32X2  
TS87C52X2  
TS80C52X2  
AT80C32X2  
AT80C52X2  
AT87C52X2**



**Table 1. Memory Size**

	ROM (bytes)	EPROM (bytes)	TOTAL RAM (bytes)
TS80C32X2	0	0	256
TS80C52X2	8k	0	256
TS87C52X2	0	8k	256

## Block Diagram



- Notes: 1. Alternate function of Port 1  
2. Alternate function of Port 3

## SFR Mapping

The Special Function Registers (SFRs) of the TS80C52X2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR1
- I/O port registers: P0, P1, P2, P3
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- Power and clock control registers: PCON
- Interrupt system registers: IE, IP, IPH
- Others: AUXR, CKCON

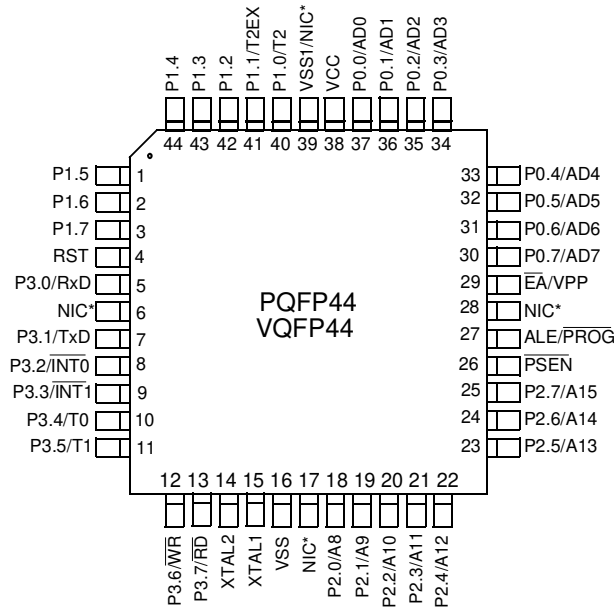
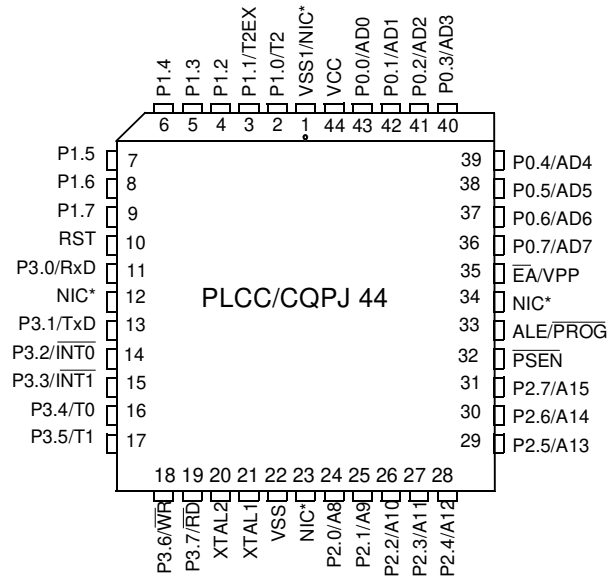
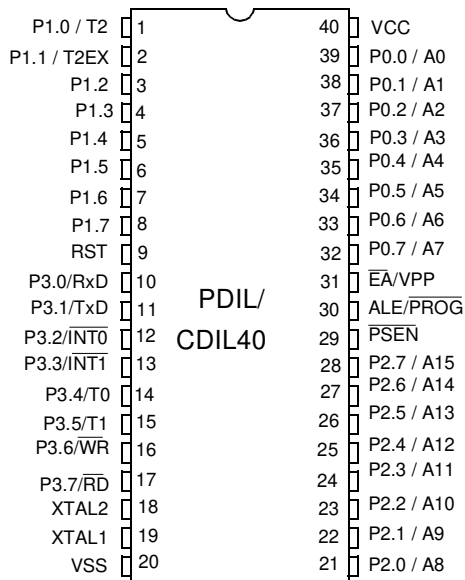
**Table 2.** All SFRs with their address and their reset value

	Bit	Non Bit							
	Addressable	Addressable							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h									FFh
F0h	B 0000 0000								F7h
E8h									EFh
E0h	ACC 0000 0000								E7h
D8h									DFh
D0h	PSW 0000 0000								D7h
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh
C0h									C7h
B8h	IP XX00 0000	SADEN 0000 0000							BFh
B0h	P3 1111 1111							IPH XX00 0000	B7h
A8h	IE 0X00 0000	SADDR 0000 0000							AFh
A0h	P2 1111 1111		AUXR1 XXXX XXX0						A7h
98h	SCON 0000 0000	SBUF XXXX XXXX							9Fh
90h	P1 1111 1111								97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XXXXXXXX0	CKCON XXXX XXX0	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Reserved 



# Pin Configuration



\*NIC: No Internal Connection

Mnemonic	Pin Number			Type	Name and Function
	DIL	LCC	VQFP 1.4		
V <sub>SS</sub>	20	22	16	I	<b>Ground:</b> 0V reference
V <sub>SS1</sub>		1	39	I	Optional Ground: <b>Contact the Sales Office for ground connection.</b>
V <sub>CC</sub>	40	44	38	I	<b>Power Supply:</b> This is the power supply voltage for normal, idle and power-down operation
P0.0-P0.7	39-32	43-36	37-30	I/O	<b>Port 0:</b> Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to V <sub>CC</sub> or V <sub>SS</sub> in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification during which P0 outputs the code bytes.
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	<b>Port 1:</b> Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during memory programming and verification.  Alternate functions for Port 1 include:
	1	2	40	I/O	<b>T2 (P1.0):</b> Timer/Counter 2 external count input/Clockout
	2	3	41	I	<b>T2EX (P1.1):</b> Timer/Counter 2 Reload/Capture/Direction Control
P2.0-P2.7	21-28	24-31	18-25	I/O	<b>Port 2:</b> Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX atDPTR). In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX atRi), port 2 emits the contents of the P2 SFR. Some Port 2 pins receive the high order address bits during EPROM programming and verification: P2.0 to P2.4
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	<b>Port 3:</b> Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also serves the special features of the 80C51 family, as listed below.
	10	11	5	I	<b>RXD (P3.0):</b> Serial input port
	11	13	7	O	<b>TXD (P3.1):</b> Serial output port
	12	14	8	I	<b>INT0 (P3.2):</b> External interrupt 0

Mnemonic	Pin Number			Type	Name and Function
	DIL	LCC	VQFP 1.4		
	13	15	9	I	<b>INT1 (P3.3):</b> External interrupt 1
	14	16	10	I	<b>T0 (P3.4):</b> Timer 0 external input
	15	17	11	I	<b>T1 (P3.5):</b> Timer 1 external input
	16	18	12	O	<b>WR (P3.6):</b> External data memory write strobe
	17	19	13	O	<b>RD (P3.7):</b> External data memory read strobe
Reset	9	10	4	I	<b>Reset:</b> A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to $V_{SS}$ permits a power-on reset using only an external capacitor to $V_{CC}$ .
ALE/ $\overline{\text{PROG}}$	30	33	27	O (I)	<b>Address Latch Enable/Program Pulse:</b> Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ( $\overline{\text{PROG}}$ ) during EPROM programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches.
PSEN	29	32	26	O	<b>Program Store Enable:</b> The read strobe to external program memory. When executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.
$\overline{\text{EA}}/V_{PP}$	31	35	29	I	<b>External Access Enable/Programming Supply Voltage:</b> $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFH (RB) or 7FFFH (RC), or FFFFH (RD). If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH (RB) or 7FFFH (RC). $\overline{\text{EA}}$ must be held low for ROMless devices. This pin also receives the 12.75V programming supply voltage ( $V_{PP}$ ) during EPROM programming. If security level 1 is programmed, $\overline{\text{EA}}$ will be internally latched on Reset.
XTAL1	19	21	15	I	<b>Crystal 1:</b> Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	<b>Crystal 2:</b> Output from the inverting oscillator amplifier



## TS80C52X2 Enhanced Features

In comparison to the original 80C52, the TS80C52X2 implements some new features, which are:

- The X2 option
- The Dual Data Pointer
- The 4 level interrupt priority system
- The power-off flag
- The ONCE mode
- The ALE disabling
- Some enhanced features are also located in the UART and the Timer 2

## X2 Feature

The TS80C52X2 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power
- Save power consumption while keeping same CPU power (oscillator power saving)
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes
- Increase CPU power by 2 while keeping same crystal frequency

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

## Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 1. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 2 shows the mode switching waveforms.

**Figure 1.** Clock Generation Diagram

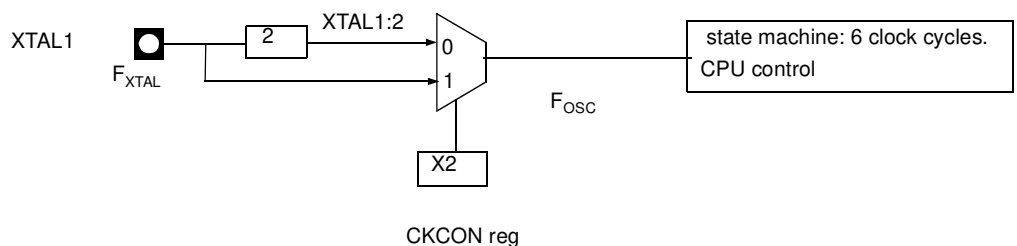
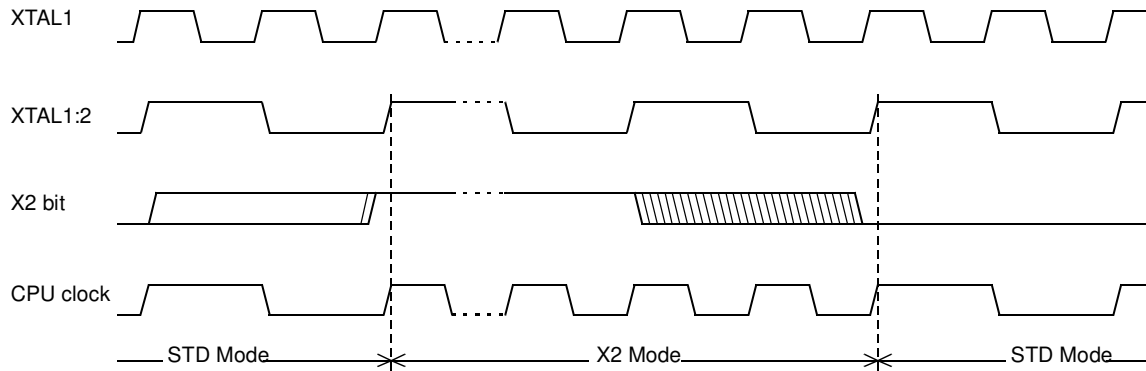


Figure 2. Mode Switching Waveforms



The X2 bit in the CKCON register (See Table 3.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

Note: In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.

Table 3. CKCON Register  
CKCON - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	X2

Bit Number	Bit Mnemonic	Description
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
3	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
2	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
1	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
0	X2	<b>CPU and peripheral clock bit</b> Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$ ). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$ ).

Reset Value = XXXX XXX0b

Not bit addressable

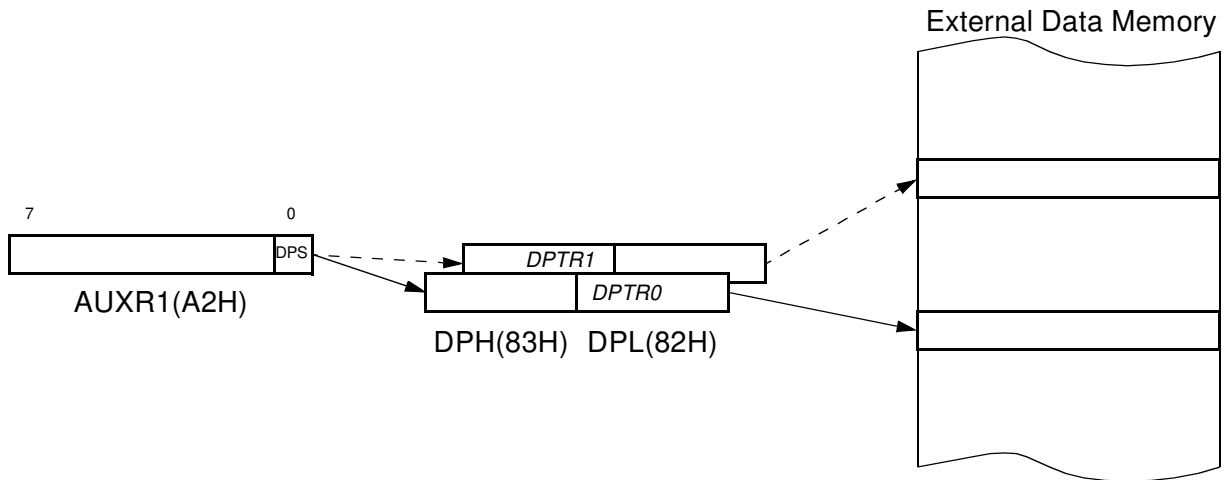
For further details on the X2 feature, please refer to ANM072 available on the web (<http://www.atmel.com>)

## Dual Data Pointer Register (Ddptr)

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 (See Table 5.) that allows the program code to switch between them (Refer to Figure 3).

**Figure 3.** Use of Dual Pointer



**Table 4.** AUXR1: Auxiliary Register 1

7	6	5	4	3	2	1	0
-	-	-	-	GF3	0	-	DPS
Bit Number	Bit Mnemonic	Description					
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
4	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
3	GF3	This bit is a general purpose user flag					
2	0	<b>Reserved</b> Always stuck at 0					
1	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
0	DPS	<b>Data Pointer Selection</b> Clear to select DPTR0. Set to select DPTR1.					

Reset Value = XXXX XXX0

Not bit addressable

## Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a 'source' pointer and the other one as a "destination" pointer.

### ASSEMBLY LANGUAGE

```

; Block move using dual data pointers
; Destroys DPTR0, DPTR1, A and PSW
; note: DPS exits opposite of entry state
; unless an extra INC AUXR1 is added
;
00A2  AUXR1 EQU 0A2H
;
0000 909000MOV DPTR,#SOURCE ; address of SOURCE
0003 05A2 INC AUXR1 ; switch data pointers
0005 90A000 MOV DPTR,#DEST ; address of DEST
0008  LOOP:
0008 05A2 INC AUXR1 ; switch data pointers
000A E0 MOVX A,atDPTR ; get a byte from SOURCE
000B A3 INC DPTR ; increment SOURCE address
000C 05A2 INC AUXR1 ; switch data pointers
000E F0 MOVX atDPTR,A ; write the byte to DEST
000F A3 INC DPTR ; increment DEST address
0010 70F6JNZ LOOP ; check for 0 terminator
0012 05A2 INC AUXR1 ; (optional) restore DPS

```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.

## Timer 2

The timer 2 in the TS80C52X2 is compatible with the timer 2 in the 80C52.

It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 5) and T2MOD register (See Table 6). Timer 2 operation is similar to Timer 0 and Timer 1.  $C/\overline{T}2$  selects  $F_{OSC}/12$  (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and CP/RL2 (T2CON), as described in the Atmel 8-bit Microcontroller Hardware description.

Refer to the Atmel 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C52X2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

### Auto-reload Mode

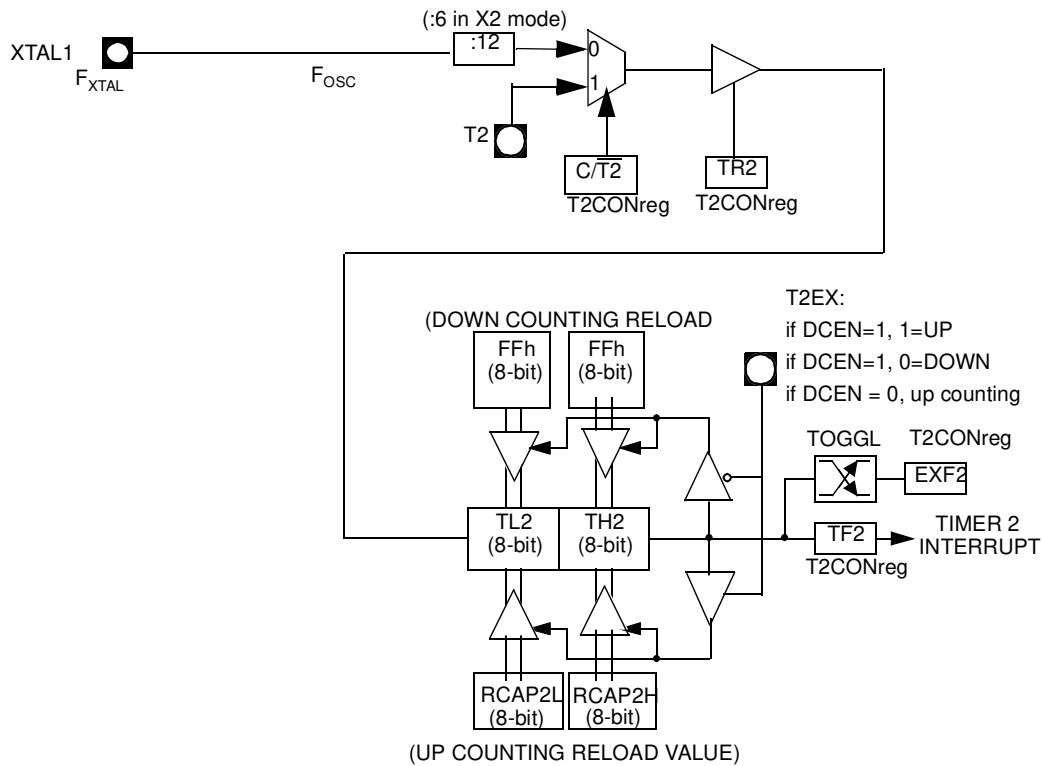
The Auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 4. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution.

Figure 4. Auto-reload Mode Up/Down Counter (DCEN = 1)



**Programmable Clock-output**

In the clock-out mode, timer 2 operates as a 50%-duty-cycle, programmable clock generator (See Figure 5) . The input clock increments TL2 at frequency  $F_{osc}/2$ . The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers :

$$Clock - OutFrequency = \frac{F_{osc}}{4 \times (65536 - RCAP2H/RCAP2L)}$$

For a 16 MHz system clock, timer 2 has a programmable frequency range of 61 Hz ( $F_{osc}/2^{16}$ ) to 4 MHz ( $F_{osc}/4$ ). The generated clock signal is brought out to T2 pin (P1.0).

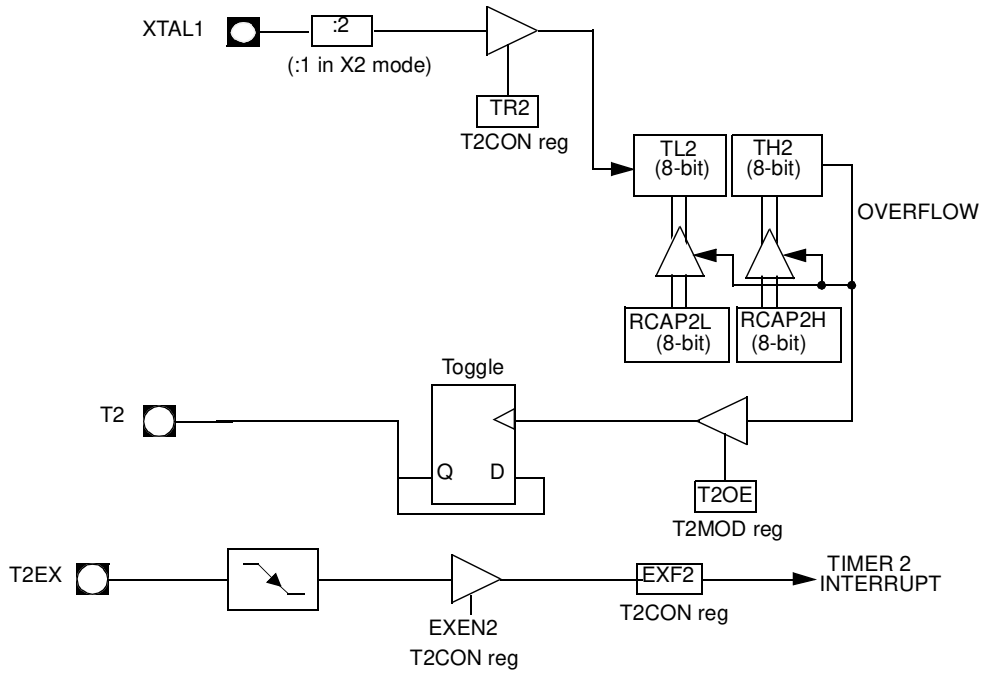
Timer 2 is programmed for the clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear  $C/\overline{T2}$  bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.
- Enter a 16-bit initial value in timer registers TH2/TL2. It can be the same as the reload value or a different one depending on the application.
- To start the timer, set TR2 run control bit in T2CON register.

It is possible to use timer 2 as a baud rate generator and a clock generator simultaneously. For this configuration, the baud rates and clock frequencies are not independent since both functions use the values in the RCAP2H and RCAP2L registers.



**Figure 5.** Clock-Out Mode  $C/\overline{T2} = 0$



**Table 5. T2CON Register**  
T2CON - Timer 2 Control Register (C8h)

7	6	5	4	3	2	1	0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#
Bit Number	Bit Mnemonic	Description					
7	TF2	<b>Timer 2 overflow Flag</b> Must be cleared by software. Set by hardware on timer 2 overflow, if RCLK = 0 and TCLK = 0.					
6	EXF2	<b>Timer 2 External Flag</b> Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. When set, causes the CPU to vector to timer 2 interrupt routine when timer 2 interrupt is enabled. Must be cleared by software. EXF2 doesn't cause an interrupt in Up/down counter mode (DCEN = 1)					
5	RCLK	<b>Receive Clock bit</b> Clear to use timer 1 overflow as receive clock for serial port in mode 1 or 3. Set to use timer 2 overflow as receive clock for serial port in mode 1 or 3.					
4	TCLK	<b>Transmit Clock bit</b> Clear to use timer 1 overflow as transmit clock for serial port in mode 1 or 3. Set to use timer 2 overflow as transmit clock for serial port in mode 1 or 3.					
3	EXEN2	<b>Timer 2 External Enable bit</b> Clear to ignore events on T2EX pin for timer 2 operation. Set to cause a capture or reload when a negative transition on T2EX pin is detected, if timer 2 is not used to clock the serial port.					
2	TR2	<b>Timer 2 Run control bit</b> Clear to turn off timer 2. Set to turn on timer 2.					
1	C/T2#	<b>Timer/Counter 2 select bit</b> Clear for timer operation (input from internal clock system: F <sub>OSC</sub> ). Set for counter operation (input from T2 input pin, falling edge trigger). Must be 0 for clock out mode.					
0	CP/RL2#	<b>Timer 2 Capture/Reload bit</b> If RCLK=1 or TCLK=1, CP/RL2# is ignored and timer is forced to Auto-reload on timer 2 overflow. Clear to Auto-reload on timer 2 overflows or negative transitions on T2EX pin if EXEN2=1. Set to capture on negative transitions on T2EX pin if EXEN2=1.					

Reset Value = 0000 0000b

Bit addressable

**Table 6.** T2MOD Register  
T2MOD - Timer 2 Mode Control Register (C9h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	DCEN
Bit Number	Bit Mnemonic	Description					
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
4	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
3	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
2	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
1	T2OE	<b>Timer 2 Output Enable bit</b> Clear to program P1.0/T2 as clock input or I/O port. Set to program P1.0/T2 as clock output.					
0	DCEN	<b>Down Counter Enable bit</b> Clear to disable timer 2 as up/down counter. Set to enable timer 2 as up/down counter.					

Reset Value = XXXX XX00b  
Not bit addressable

**TS80C52X2 Serial I/O Port**

The serial I/O port in the TS80C52X2 is compatible with the serial I/O port in the 80C52. It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

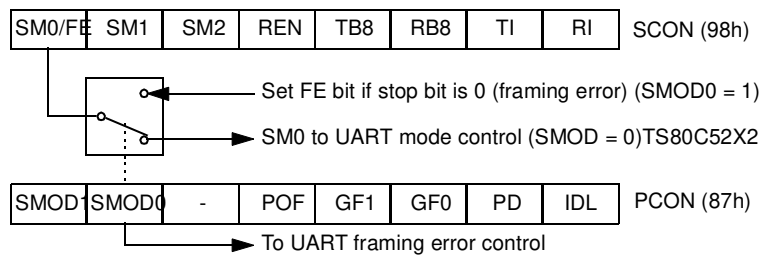
Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

**Framing Error Detection**

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 6).

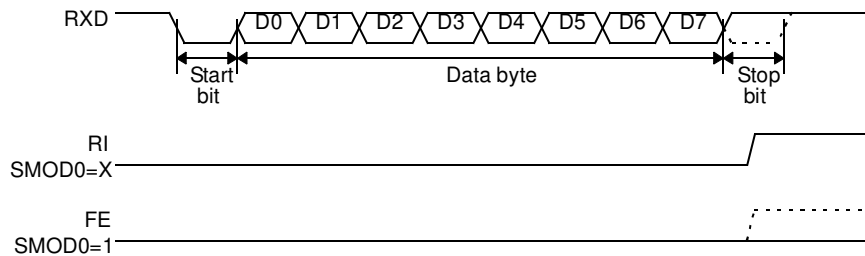
**Figure 6.** Framing Error Block Diagram



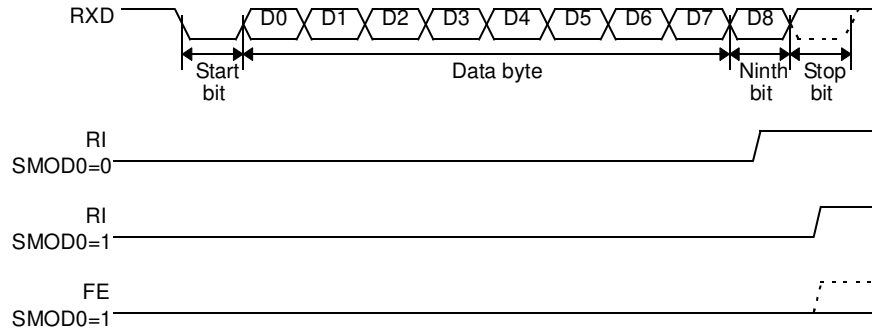
When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 9.) bit is set.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 7. and Figure 8.).

**Figure 7.** UART Timings in Mode 1



**Figure 8.** UART Timings in Modes 2 and 3



### Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

Note: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

### Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed.

To address a device by its individual address, the SADEN mask byte must be 1111 1111b.

For example:

```
SADDR0101 0110b
SADEN1111 1100b
Given0101 01XXb
```

The following is an example of how to use given addresses to address different slaves:

```
Slave A:SADDR1111 0001b
SADEN1111 1010b
Given1111 0X0Xb
```

```
Slave B:SADDR1111 0011b
SADEN1111 1001b
Given1111 0XX1b
```

```
Slave C:SADDR1111 0010b
SADEN1111 1101b
Given1111 00X1b
```

The SADEN byte is selected so that each slave may be addressed separately.

For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g.

1111 0000b).

For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. 1111 0011b).

To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

**Broadcast Address**

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

```
SADDR 0101 0110b
SADEN 1111 1100b
Broadcast =SADDR OR SADEN1111 111Xb
```

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

```
Slave A:SADDR1111 0001b
      SADEN1111 1010b
Broadcast1111 1X11b,
```

```
Slave B:SADDR1111 0011b
      SADEN1111 1001b
Broadcast1111 1X11B,
```

```
Slave C:SADDR=1111 0010b
      SADEN1111 1101b
Broadcast1111 1111b
```

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send an address FBh.

**Reset Addresses**

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX XXXXb (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

**Table 7. SADEN Register**  
SADEN - Slave Address Mask Register (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b  
Not bit addressable

**Table 8. SADDR Register**  
SADDR - Slave Address Register (A9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b  
Not bit addressable





**Table 9.** SCON Register  
SCON - Serial Control Register (98h)

7	6	5	4	3	2	1	0																									
FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI																									
Bit Number	Bit Mnemonic	Description																														
7	FE	<b>Framing Error bit (SMOD0=1)</b> Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit																														
	SM0	<b>Serial port Mode bit 0</b> Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit																														
6	SM1	<b>Serial port Mode bit 1</b> <table border="1"> <thead> <tr> <th>SM0</th> <th>SM1</th> <th>Mode</th> <th>Description</th> <th>Baud Rate</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Shift Register</td> <td><math>F_{XTAL}/12</math> (/6 in X2 mode)</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>8-bit UART</td> <td>Variable</td> </tr> <tr> <td>1</td> <td>0</td> <td>2</td> <td>9-bit UART</td> <td><math>F_{XTAL}/64</math> or <math>F_{XTAL}/32</math> (/32, /16 in X2 mode)</td> </tr> <tr> <td>1</td> <td>1</td> <td>3</td> <td>9-bit UART</td> <td>Variable</td> </tr> </tbody> </table>						SM0	SM1	Mode	Description	Baud Rate	0	0	0	Shift Register	$F_{XTAL}/12$ (/6 in X2 mode)	0	1	1	8-bit UART	Variable	1	0	2	9-bit UART	$F_{XTAL}/64$ or $F_{XTAL}/32$ (/32, /16 in X2 mode)	1	1	3	9-bit UART	Variable
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1	1	3	9-bit UART	Variable																												
5	SM2	<b>Serial port Mode 2 bit / Multiprocessor Communication Enable bit</b> Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.																														
4	REN	<b>Reception Enable bit</b> Clear to disable serial reception. Set to enable serial reception.																														
3	TB8	Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3. Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.																														
2	RB8	<b>Receiver Bit 8 / Ninth bit received in modes 2 and 3</b> Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.																														
1	TI	<b>Transmit Interrupt flag</b> Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.																														
0	RI	<b>Receive Interrupt flag</b> Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 7. and Figure 8. in the other modes.																														

Reset Value = 0000 0000b

Bit addressable

**Table 10.** PCON Register  
PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
Bit Number	Bit Mnemonic	Description					
7	SMOD1	<b>Serial port Mode bit 1</b> Set to select double baud rate in mode 1, 2 or 3.					
6	SMOD0	<b>Serial port Mode bit 0</b> Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.					
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
4	POF	<b>Power-off Flag</b> Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.					
3	GF1	<b>General purpose Flag</b> Cleared by user for general purpose usage. Set by user for general purpose usage.					
2	GF0	<b>General purpose Flag</b> Cleared by user for general purpose usage. Set by user for general purpose usage.					
1	PD	<b>Power-down mode bit</b> Cleared by hardware when reset occurs. Set to enter power-down mode.					
0	IDL	<b>Idle mode bit</b> Clear by hardware when interrupt or reset occurs. Set to enter idle mode.					

Reset Value = 00X1 0000b

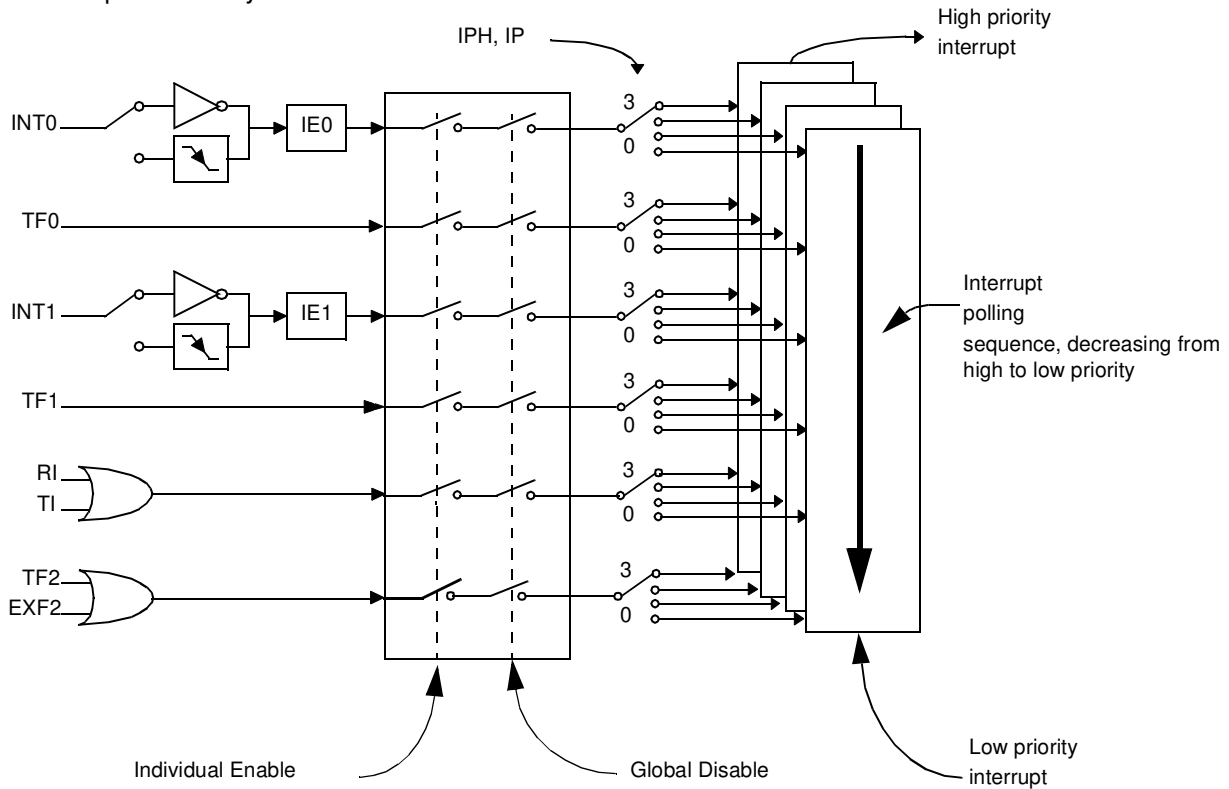
Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.

## Interrupt System

The TS80C52X2 has a total of 6 interrupt vectors: two external interrupts ( $\overline{INT0}$  and  $\overline{INT1}$ ), three timer interrupts (timers 0, 1 and 2) and the serial port interrupt. These interrupts are shown in Figure 9.

**Figure 9.** Interrupt Control System



Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 12.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 13.) and in the Interrupt Priority High register (See Table 14.). shows the bit values and priority levels associated with each combination.

**Table 11.** Priority Level Bit Values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level

are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

**Table 12.** IE Register  
IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	-	ET2	ES	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	<b>Enable All interrupt bit</b> Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	ET2	<b>Timer 2 overflow interrupt Enable bit</b> Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.
4	ES	<b>Serial port Enable bit</b> Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	<b>Timer 1 overflow interrupt Enable bit</b> Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	<b>External interrupt 1 Enable bit</b> Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	<b>Timer 0 overflow interrupt Enable bit</b> Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	<b>External interrupt 0 Enable bit</b> Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0X00 0000b

Bit addressable

**Table 13.** IP Register  
IP - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0
-	-	PT2	PS	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Description
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	PT2	<b>Timer 2 overflow interrupt Priority bit</b> Refer to PT2H for priority level.
4	PS	<b>Serial port Priority bit</b> Refer to PSH for priority level.
3	PT1	<b>Timer 1 overflow interrupt Priority bit</b> Refer to PT1H for priority level.
2	PX1	<b>External interrupt 1 Priority bit</b> Refer to PX1H for priority level.
1	PT0	<b>Timer 0 overflow interrupt Priority bit</b> Refer to PT0H for priority level.
0	PX0	<b>External interrupt 0 Priority bit</b> Refer to PX0H for priority level.

Reset Value = XX00 0000b  
Bit addressable

**Table 14.** IPH Register  
IPH - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0															
-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H															
Bit Number	Bit Mnemonic	Description																				
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.																				
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.																				
5	PT2H	<b>Timer 2 overflow interrupt Priority High bit</b> <table border="1"> <thead> <tr> <th>PT2H</th> <th>PT2</th> <th>Priority Level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Lowest</td> </tr> <tr> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Highest</td> </tr> </tbody> </table>						PT2H	PT2	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PT2H	PT2	Priority Level																				
0	0	Lowest																				
0	1																					
1	0																					
1	1	Highest																				
4	PSH	<b>Serial port Priority High bit</b> <table border="1"> <thead> <tr> <th>PSH</th> <th>PS</th> <th>Priority Level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Lowest</td> </tr> <tr> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Highest</td> </tr> </tbody> </table>						PSH	PS	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
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1	0																					
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PT1H	PT1	Priority Level																				
0	0	Lowest																				
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PX1H	PX1	Priority Level																				
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0	0	Lowest																				
0	1																					
1	0																					
1	1	Highest																				

Reset Value = XX00 0000b  
Not bit addressable

