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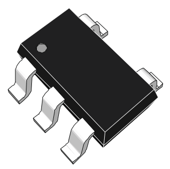
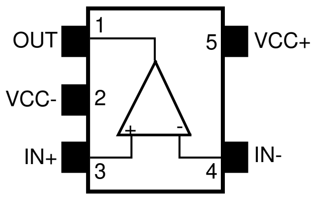
TSB611

Low-power, rail-to-rail output, 36 V operational amplifier

Datasheet - production data



SOT23-5



Features

- Low offset voltage: 1 mV max
- Low power consumption: 125 µA max. at 36 V
- Wide supply voltage: 2.7 to 36 V
- Gain bandwidth product: 560 kHz typ
- Unity gain stable
- Rail-to-rail output
- Input common mode voltage includes ground
- High tolerance to ESD: 4 kV HBM
- Extended temperature range: -40 °C to 125 °C
- Automotive qualification

Applications

- Industrial
- Power supplies
- Automotive

Description

The TSB611 single operational amplifier (op amp) offers an extended supply voltage operating range and rail-to-rail output. It also offers an excellent speed/power consumption ratio with 560 kHz gain bandwidth product while consuming less than 125 µA at 36V supply voltage.

The TSB611 operates over a wide temperature range from -40 °C to 125°C making this device ideal for industrial and automotive applications.

Thanks to its small package size, the TSB611 can be used in applications where space on the board is limited. It can thus reduce the overall cost of the PCB.

Contents

1 Absolute maximum ratings and operating conditions

Table 1: Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{cc}	Supply voltage [(1)]	40	V
V_{id}	Differential input voltage [(2)]	$\pm V_{cc}$	
V_{in}	Input voltage	$(V_{cc-}) - 0.2$ to $(V_{cc+}) + 0.2$	
I_{in}	Input current [(3)]	10	mA
T_{stg}	Storage temperature	-65 to 150	°C
R_{thja}	Thermal resistance junction to ambient [(4)(5)]	250	°C/W
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model [(6)]	4000	V
	MM: machine model [(7)]	200	
	CDM: charged device model [(8)]	1500	
	Latch-up immunity	200	mA

Notes:

(1) All voltage values, except differential voltage are with respect to network ground terminal.

(2) Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.

(3) Input current must be limited by a resistor in series with the inputs.

(4) R_{th} are typical values.

(5) Short-circuits can cause excessive heating and destructive dissipation.

(6) According to JEDEC standard JESD22-A114F.

(7) According to JEDEC standard JESD22-A115A.

(8) According to ANSI/ESD STM5.3.1.

Table 2: Operating conditions

Symbol	Parameter	Value	Unit
V_{cc}	Supply voltage	2.7 to 36	V
V_{icm}	Common mode input voltage range	$(V_{cc-}) - 0.1$ to $(V_{cc+}) - 1$	
T_{oper}	Operating free air temperature range	-40 to 125	°C

2 Electrical characteristics

Table 3: Electrical characteristics at Vcc+ = 2.7 V with Vcc- = 0 V, Vicm = Vcc/2, Tamb = 25 °C, and RL = 10 kΩ connected to Vcc/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage		-1		1	mV
		-40 °C < T< 125 °C	-1.6		1.6	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T< 125 °C		1.8	6	μV/°C
I_{io}	Input offset current			1	5	nA
		-40 °C < T< 125 °C			10	
I_{ib}	Input bias current			5	10	
		-40 °C < T< 125 °C			15	
CMR	Common mode rejection ratio: 20 log ($\Delta V_{icm}/\Delta V_{io}$)	V_{icm} = 0 V to V_{cc+} -1 V, $V_{out} = V_{cc}/2$	90	115		dB
		-40 °C < T< 125 °C	85			
A_{vd}	Large signal voltage gain	V_{out} = 0.5 V to (V_{cc+} - 0.5 V)	98	102		
		-40 °C < T< 125 °C	94			
V_{OH}	High level output voltage (voltage drop from V_{cc+})			13	25	mV
		-40 °C < T< 125 °C			30	
V_{OL}	Low level output voltage			26	30	
		-40 °C < T< 125 °C			35	
I_{out}	I_{sink}	$V_{out} = V_{cc}$	13	20		mA
		-40 °C < T< 125 °C	10			
	I_{source}	V_{out} = 0 V	20	28		
		-40 °C < T< 125 °C	7			
I_{CC}	Supply current (per channel)	No load, $V_{out} = V_{cc}/2$		92	110	μA
		-40 °C < T< 125 °C			125	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF		480		kHz
F_u	Unity gain frequency	R_L = 10 kΩ, C_L = 100 pF		430		
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		60		Degrees
G_m	Gain margin	R_L = 10 kΩ, C_L = 100 pF		18		dB
SR+	Positive slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V	0.13	0.18		V/μs
SR-	Negative slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V	0.10	0.14		
e_n	Equivalent input noise voltage	f = 1 kHz		37		nV/√Hz
		f = 10 kHz		32		
THD+N	Total harmonic distortion + noise	f_{in} = 1 kHz, Gain = 1, R_L = 100 kΩ, V_{icm} = (V_{cc} - 1 V)/2, BW = 22 kHz, V_{out} = 1 V_{pp}		0.005		%

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{rec}	Overload recovery time			2		µs

Table 4: Electrical characteristics at Vcc+ = 12 V with Vcc- = 0 V, Vicm = Vcc/2, Tamb = 25 °C, and RL = 10 kΩ connected to Vcc/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage		-1		1	mV
		-40 °C < T< 125 °C	-1.6		1.6	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T< 125 °C		1.6	6	µV/°C
I_{io}	Input offset current			1	5	nA
		-40 °C < T< 125 °C			15	
I_{ib}	Input bias current			5	10	
		-40 °C < T< 125 °C			15	
CMR	Common mode rejection ratio: 20 log ($\Delta V_{icm}/\Delta V_{io}$)	V_{icm} = 0 V to V_{cc+} - 1 V, V_{out} = $V_{cc}/2$	95	126		dB
		-40 °C < T< 12 5°C	90			
SVR	Supply voltage rejection ratio: 20 log ($\Delta V_{cc}/\Delta V_{io}$)	V_{cc} = 2.8 to 12 V	95	124		
		-40 °C < T< 125 °C	90			
A_{vd}	Large signal voltage gain	V_{out} = 0.5 V to (V_{cc+} - 0.5 V)	105	115		
		-40 °C < T< 125 °C	100			
V_{OH}	High level output voltage drop from V_{cc+}			37	60	mV
		-40 °C < T< 125 °C			65	
V_{OL}	Low level output voltage			56	65	
		-40 °C < T< 125 °C			75	
I_{out}	I_{sink}	V_{out} = V_{cc}	24	35		mA
		-40 °C < T< 125 °C	10			
	I_{source}	V_{out} = 0 V	28	40		
		-40 °C < T< 125 °C	10			
I_{CC}	Supply current (per channel)	No load, V_{out} = $V_{cc}/2$		97	115	µA
		-40 °C < T< 125 °C			130	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF		510		kHz
F_u	Unity gain frequency	R_L = 10 kΩ, C_L = 100 pF		460		
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		60		Degrees
G_m	Gain margin	R_L = 10 kΩ, C_L = 100 pF		18		dB
SR+	Positive slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V	0.13	0.19		V/µs
SR-	Negative slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V	0.11	0.15		
e_n	Equivalent input noise voltage	f = 1 kHz		31		nV/√Hz
		f = 10 kHz		30		
THD+N	Total harmonic distortion + noise	f_{in} = 1 kHz, Gain = 1, R_L = 100 kΩ, V_{icm} = (V_{cc} - 1 V)/2, BW = 22 kHz, V_{out} = 2 V_{pp}		0.004		%

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{rec}	Overload recovery time			2		µs

Table 5: Electrical characteristics at Vcc+ = 36 V with Vcc- = 0 V, Vicm = Vcc/2, Tamb = 25 °C, and RL = 10 kΩ connected to Vcc/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage		-1		1	mV
		-40 °C < T< 125 °C	-1.6		1.6	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T< 125 °C		1.3	6	μV/°C
I_{io}	Input offset current			1	5	nA
		-40 °C < T< 125 °C			20	
I_{ib}	Input bias current			5	10	
		-40 °C < T< 125 °C			20	
CMR	Common mode rejection ratio: 20 log ($\Delta V_{icm}/\Delta V_{io}$)	V_{icm} = 0 V to V_{cc+} - 1 V, $V_{out} = V_{cc}/2$	105	130		dB
		-40 °C < T< 125 °C	100			
SVR	Supply voltage rejection ratio 20 log ($\Delta V_{cc}/\Delta V_{io}$)	V_{cc} = 12 to 36 V	100	124		
		-40 °C < T< 125 °C	95			
A_{vd}	Large signal voltage gain	V_{out} = 0.5 V to (V_{cc+} - 0.5 V)	110	120		
		-40 °C < T< 125 °C	105			
V_{OH}	High level output voltage drop from V_{CC+}			80	110	mV
		-40 °C < T< 125 °C			150	
V_{OL}	Low level output voltage			90	110	
		-40 °C < T< 125 °C			150	
I_{out}	I_{sink}	$V_{out} = V_{cc}$	40	60		mA
		-40 °C < T< 125 °C	10			
	I_{source}	V_{out} = 0 V	40	70		
		-40 °C < T< 125 °C	20			
I_{CC}	Supply current (per channel)	No load, $V_{out} = V_{cc}/2$		103	125	μA
		-40 °C < T< 125 °C			140	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF		560		kHz
F_u	Unity gain frequency	R_L = 10 kΩ, C_L = 100 pF		500		
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		58		Degrees
G_m	Gain margin	R_L = 10 kΩ, C_L = 100 pF		18		dB
SR+	Positive slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V	0.15	0.20		V/μs
SR-	Negative slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V	0.12	0.16		
e_n	Equivalent input noise voltage	f = 1 kHz		29		nV/√Hz
		f = 10 kHz		28		
THD+N	Total harmonic distortion + noise	f_{in} = 1 kHz, Gain = 1, R_L = 100 kΩ, V_{icm} = (V_{cc} - 1 V)/2, BW = 22 kHz, V_{out} = 2 V_{pp}		0.004		%

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{rec}	Overload recovery time	R_L = 10 kΩ, C_L = 100 pF, Gain = 1		2		µs

Figure 1: Supply current vs. supply voltage at Vicm = VCC/2

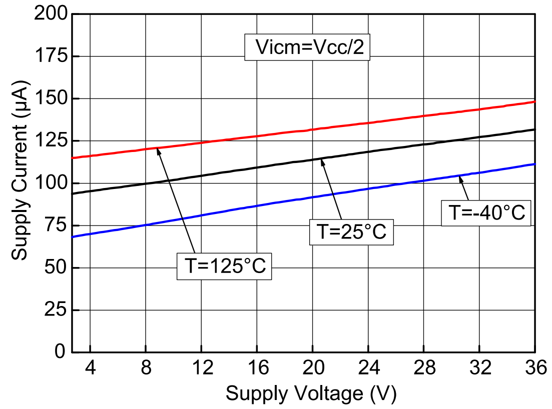


Figure 2: Input offset voltage distribution at VCC = 2.7 V

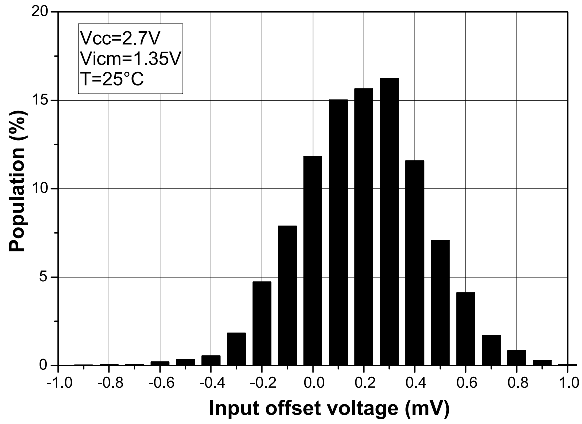


Figure 3: Input offset voltage distribution at VCC = 12 V

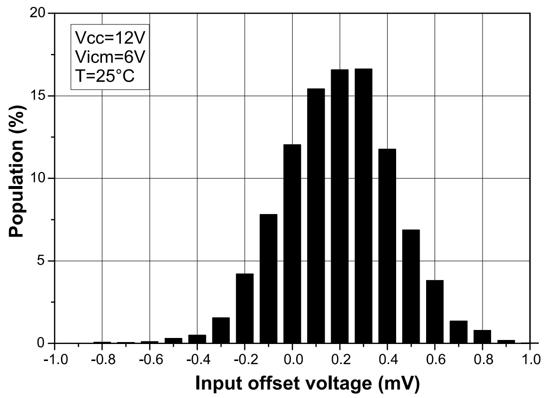


Figure 4: Input offset voltage distribution at VCC = 36 V

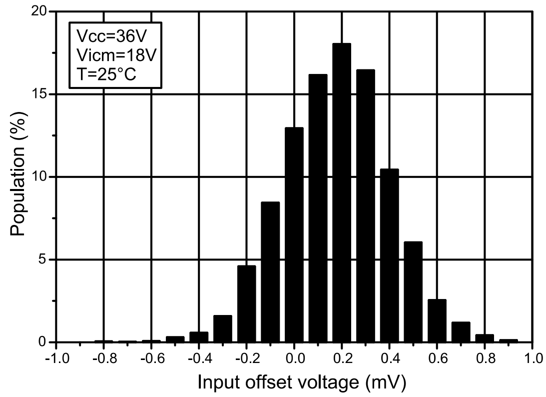


Figure 5: Input offset voltage vs. Temperature at VCC = 36 V

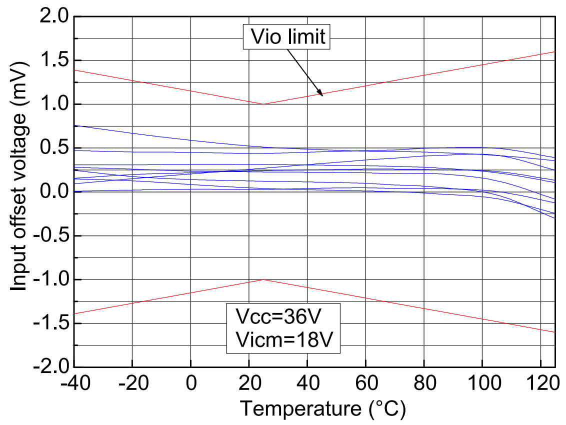


Figure 6: Input offset voltage temperature variation distribution at VCC = 36 V

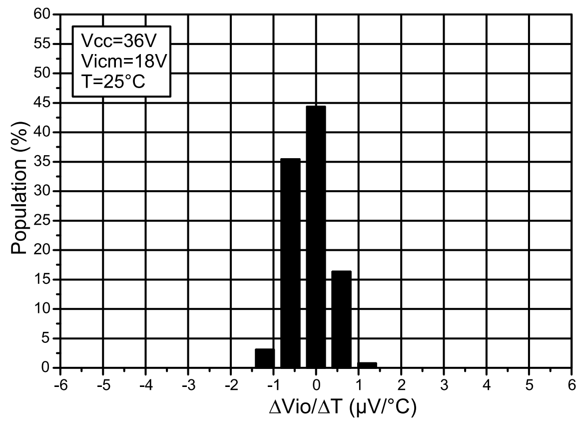


Figure 7: Input offset voltage vs. supply voltage

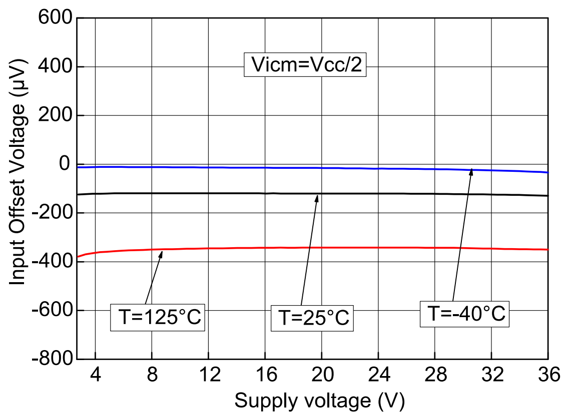


Figure 8: Input offset voltage vs. common-mode voltage at VCC = 2.7 V

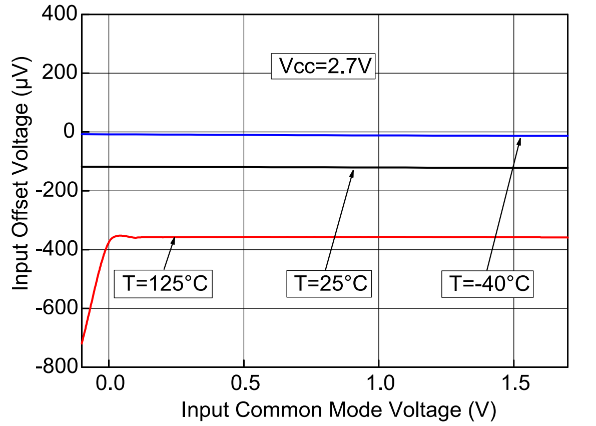


Figure 9: Input offset voltage vs. common-mode voltage at VCC = 36 V

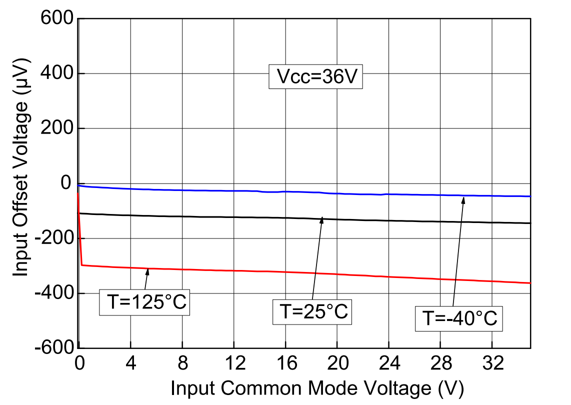


Figure 10: Input bias current vs. common mode voltage at VCC = 4 V

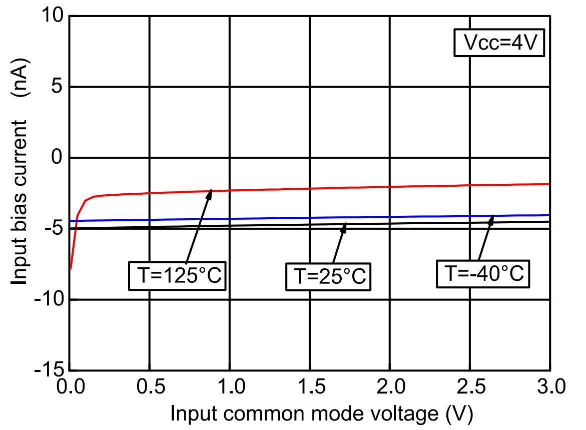


Figure 11: Input bias current vs. common mode voltage at VCC = 36 V

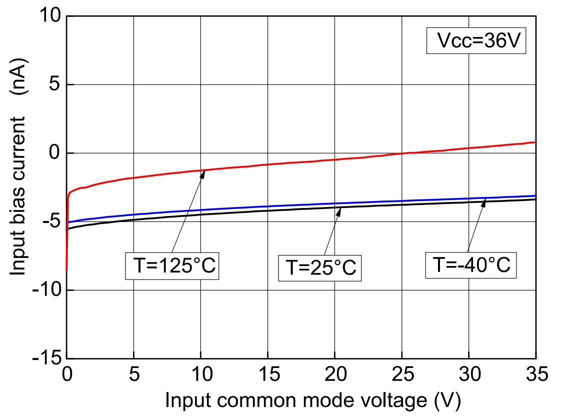


Figure 12: Output current vs. output voltage at VCC = 2.7 V

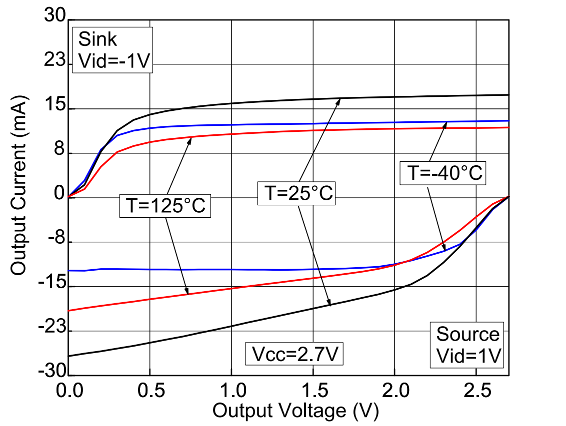


Figure 13: Output current vs. output voltage at VCC = 36 V

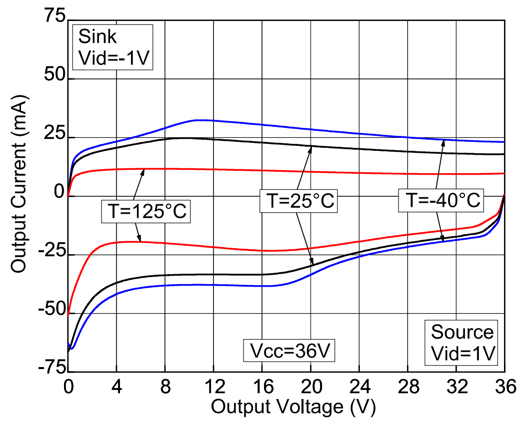


Figure 14: Output voltage (Voh) vs. supply voltage

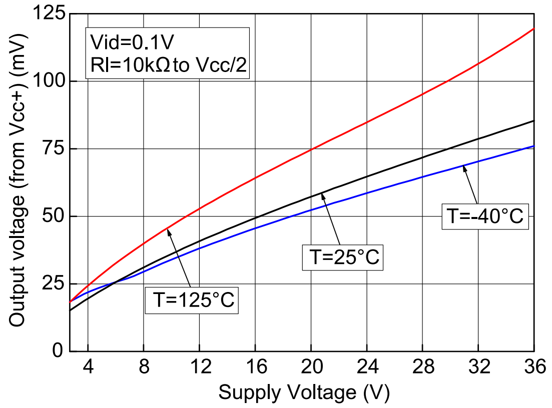


Figure 15: Output voltage (Vol) vs. supply voltage

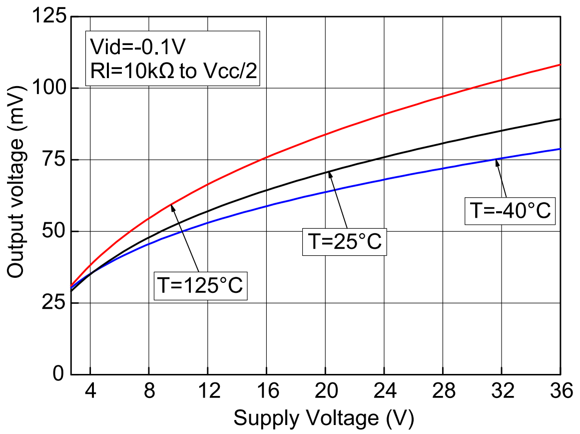


Figure 16: Amplifier behavior close to negative rail at VCC = 5 V

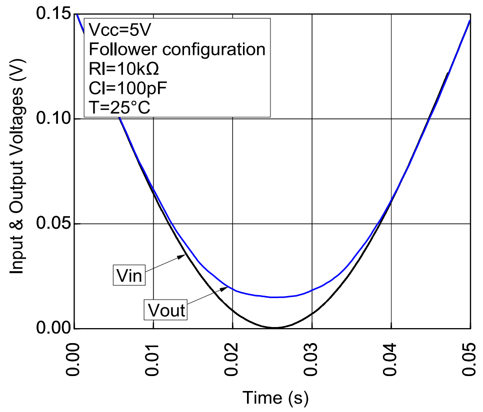


Figure 17: Amplifier behavior close to positive rail at VCC = 5 V

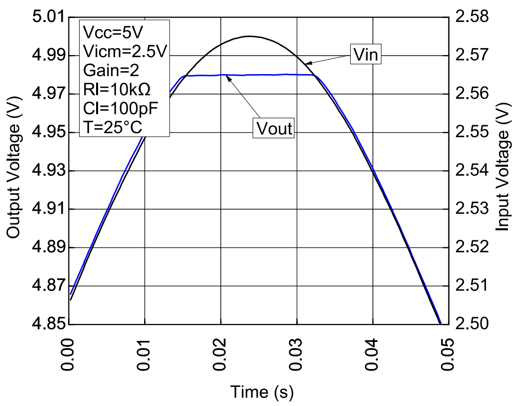


Figure 18: Slew rate vs. supply voltage

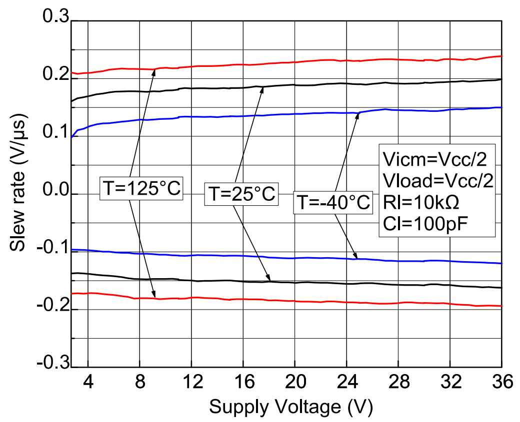


Figure 19: Negative slew rate behavior vs. temperature at VCC = 36 V

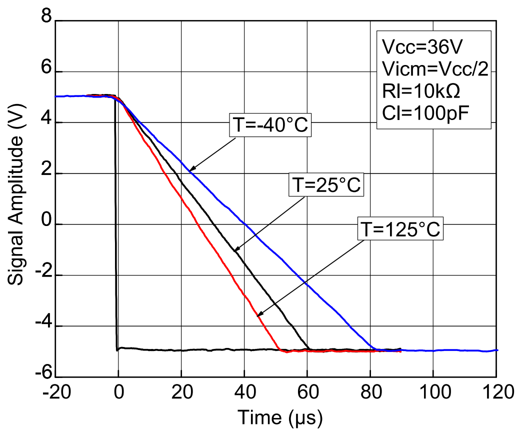


Figure 20: Positive slew rate behavior vs. temperature at VCC = 36 V

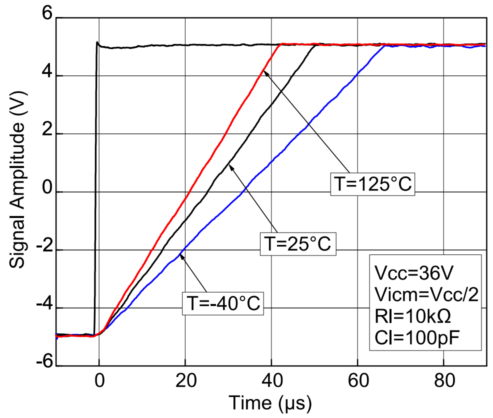


Figure 21: Small step response vs. time at VCC = 36 V

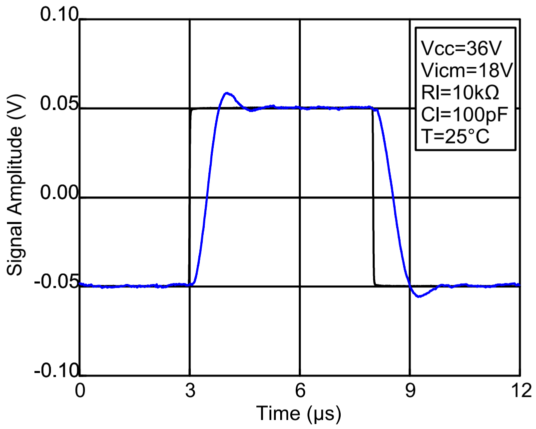


Figure 22: Output desaturation vs. time

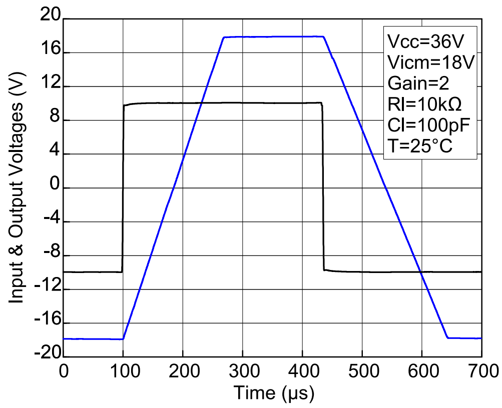


Figure 23: Gain and phase vs. frequency at VCC = 2.7 V

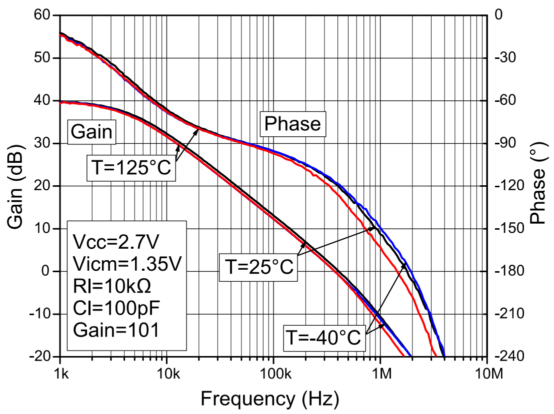


Figure 24: Gain and phase vs. frequency at VCC = 36 V

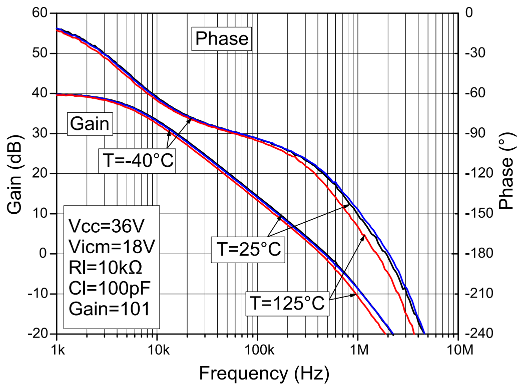


Figure 25: Phase margin vs. output current at VCC = 2.7 V and 36 V

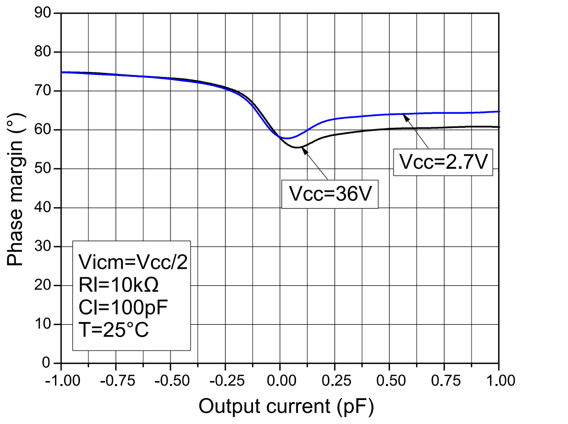


Figure 26: Phase margin vs. capacitive load at VCC = 2.7 V and 36 V

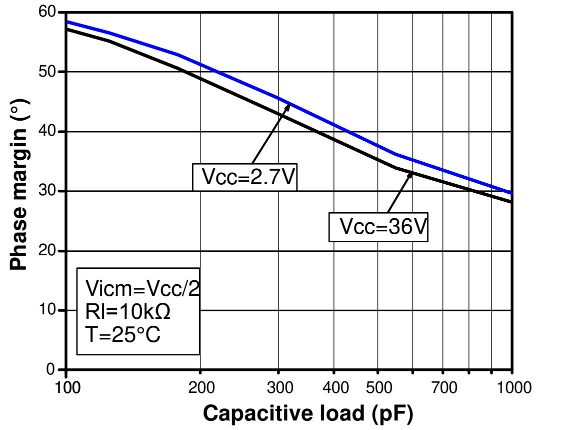


Figure 27: Overshoot vs. capacitive load at VCC = 2.7 V and 36 V

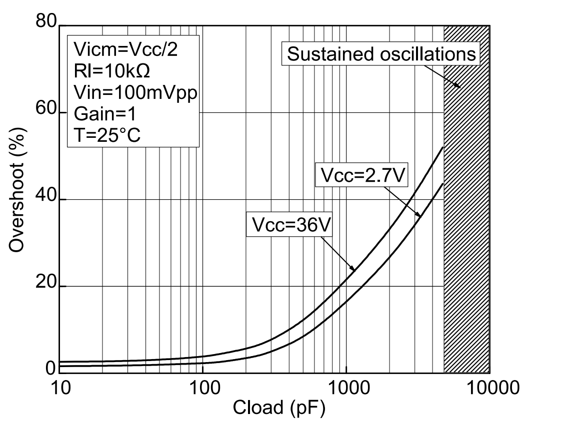


Figure 28: Noise vs. frequency at VCC = 36 V

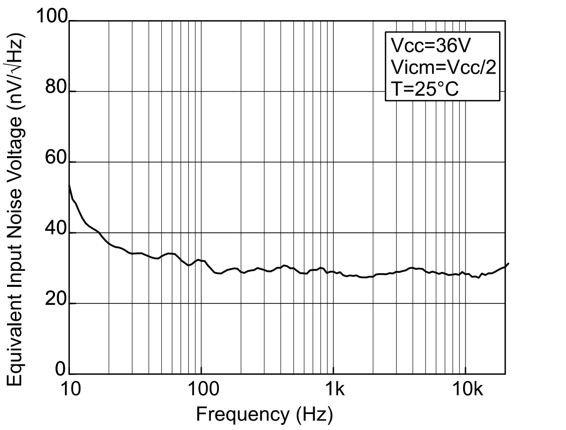


Figure 29: Noise vs. time at VCC = 36 V

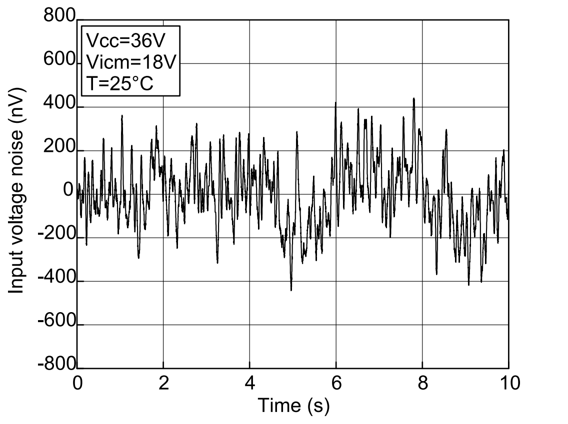


Figure 30: THD+N vs. frequency

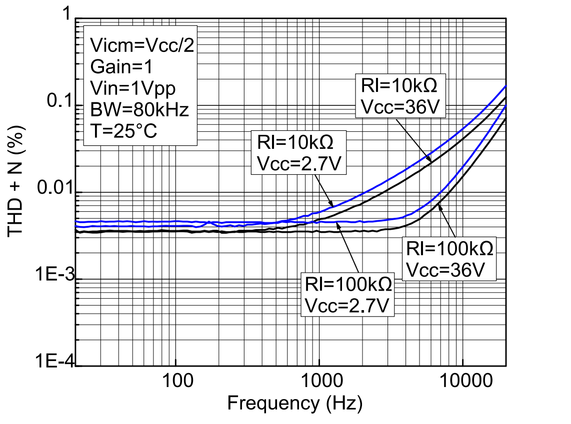


Figure 31: THD+N vs. output voltage

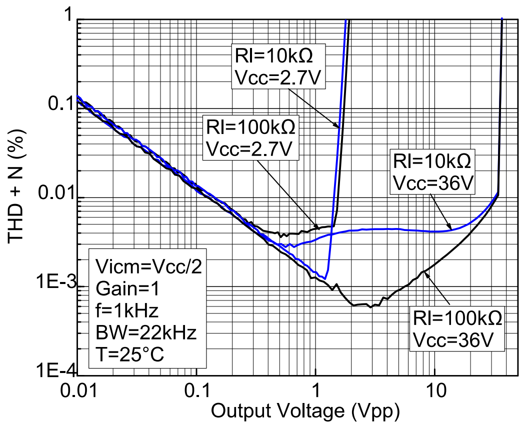


Figure 32: PSRR vs. frequency at VCC = 36 V

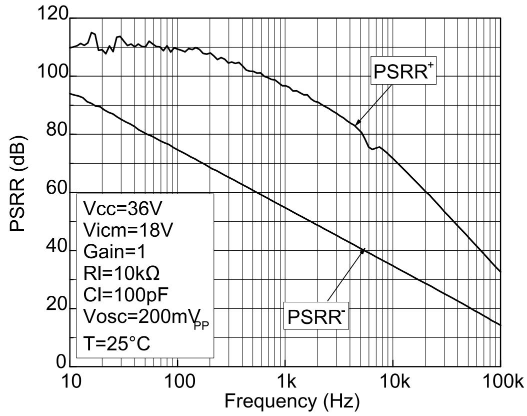


Figure 33: Output impedance vs. frequency at VCC = 2.7 V and 36 V

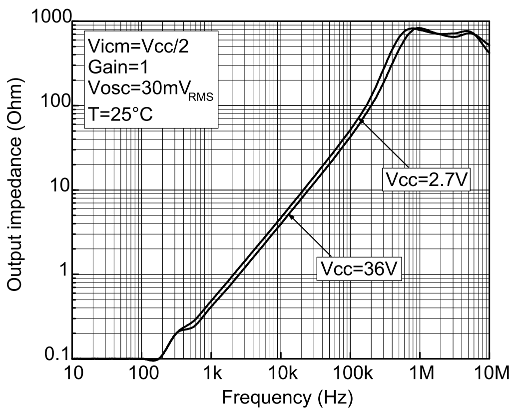
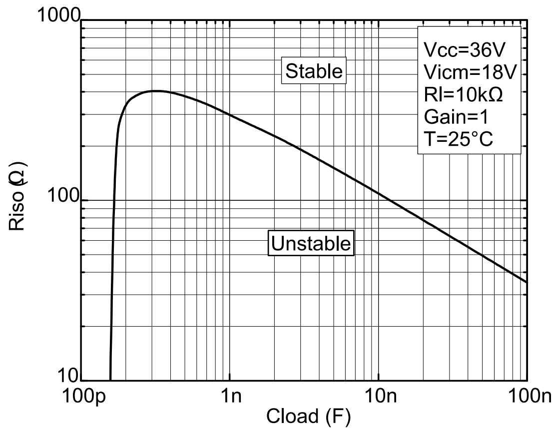


Figure 34: Output series resistor recommended for stability vs. capacitive load



3 Application information

3.1 Operating voltages

The TSB611 operational amplifier can operate from 2.7 V to 36 V. The parameters are fully specified at 2.7 V, 12 V, and 36 V power supplies. However, parameters are very stable in the full V_{cc} range. Additionally, main specifications are guaranteed in the extended temperature range from -40 to 125 °C.

3.2 Input common-mode range

The TSB611 has an input common-mode range that includes ground. The input common-mode range is extended from (V_{CC-}) - 0.1 V to (V_{CC+}) - 1 V.

3.3 Rail-to-rail output

The operational amplifier's output levels can go close to the rails: 100 mV maximum below the positive rail and 110 mV maximum above the negative rail when connected to a 10 kΩ resistive load to $V_{CC}/2$ for a power supply voltage of 36 V.

3.4 Input offset voltage drift over temperature

The maximum input voltage drift variation over temperature is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift over temperature is computed using *Equation 1*.

Equation 1

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) - V_{io}(25\,°C)}{T - 25\,°C}\right|$$

Where T = -40 °C and 125 °C.

The datasheet maximum value is guaranteed by measurements on a representative sample size ensuring a C_{pk} (process capability index) greater than 2.

3.5 Long term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using *Equation 2*.

Equation 2

$$A_{FV} = e^{\beta \cdot (V_S - V_U)}$$

Where:

A_{FV} is the voltage acceleration factor

β is the voltage acceleration constant in 1/V, constant technology parameter (β = 1)

V_S is the stress voltage used for the accelerated test

V_U is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined in *Equation 3*.

Equation 3

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S}\right)}$$

Where:

A_{FT} is the temperature acceleration factor

E_a is the activation energy of the technology based on the failure rate

k is the Boltzmann constant (8.6173 x 10^{-5} eV.K^{-1})

T_U is the temperature of the die when V_U is used (K)

T_S is the temperature of the die under temperature stress (K)

The final acceleration factor, A_F, is the multiplication of the voltage acceleration factor and the temperature acceleration factor (*Equation 4*).

Equation 4

$$A_F = A_{FT} \times A_{FV}$$

A_F is calculated using the temperature and voltage defined in the mission profile of the product. The A_F value can then be used in *Equation 5* to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

Equation 5

$$\text{Months} = A_F \times 1000\ \text{h} \times 12\ \text{months} / (24\ \text{h} \times 365.25\ \text{days})$$

To evaluate the op amp reliability, a follower stress condition is used where V_{CC} is defined as a function of the maximum operating voltage and the absolute maximum rating (as recommended by JEDEC rules).

The V_{io} drift (in µV) of the product after 1000 h of stress is tracked with parameters at different measurement conditions (see *Equation 6*).

Equation 6

$$V_{CC} = \text{max}V_{op} \text{ with } V_{icm} = V_{CC}/2$$

The long term drift parameter (ΔV_{io}), estimating the reliability performance of the product, is obtained using the ratio of the V_{io} (input offset voltage value) drift over the square root of the calculated number of months (*Equation 7*).

Equation 7

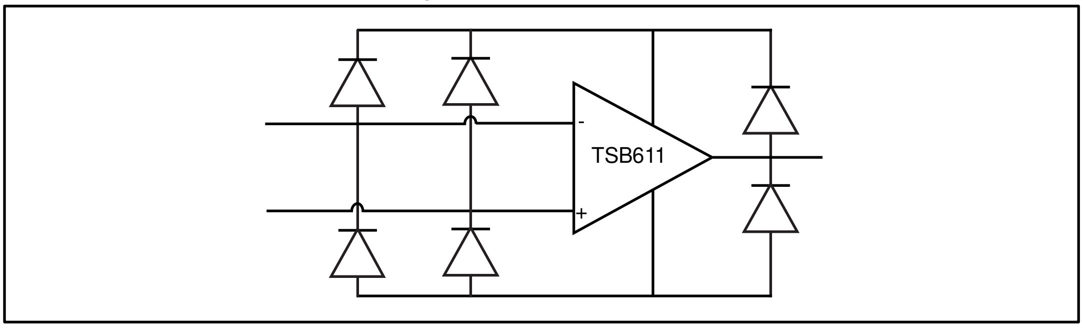
$$\Delta V_{io} = \frac{V_{io}drift}{\sqrt{(months)}}$$

Where V_{io} drift is the measured drift value in the specified test conditions after 1000 h stress duration.

3.6 ESD structure of TSB611

The TSB611 is protected against electrostatic discharge (ESD) with dedicated diodes (see *Figure 35*). These diodes must be considered at application level especially when signals applied on the input pins go beyond the power supply rails (V_{CC+} or V_{CC-}). Current through the diodes must be limited to a maximum of 10 mA as stated in *Table 1*. A serial resistor or a Schottky diode can be used on the inputs to improve protection but the 10 mA limit of input current must be strictly observed.

Figure 35: ESD structure



3.7 Initialization time

The TSB611 has a good power supply rejection ratio (PSRR), but as with all devices, it is recommended to use a 22 nF bypass capacitor as close as possible to the power supply pins. It prevents the noise present on the power supply impacting the signal conditioning. In addition, this bypass capacitor enhances the initialization time (see *Figure 36* and *Figure 37*).

Figure 36: Startup behavior without bypass capacitor

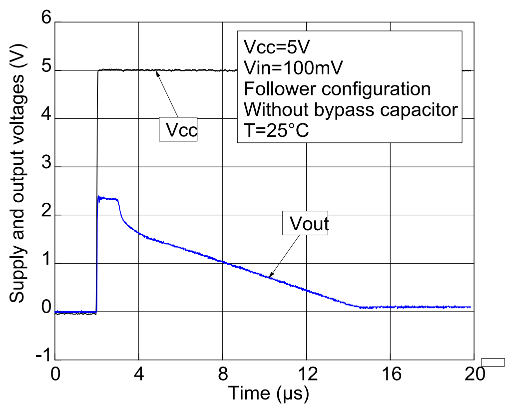
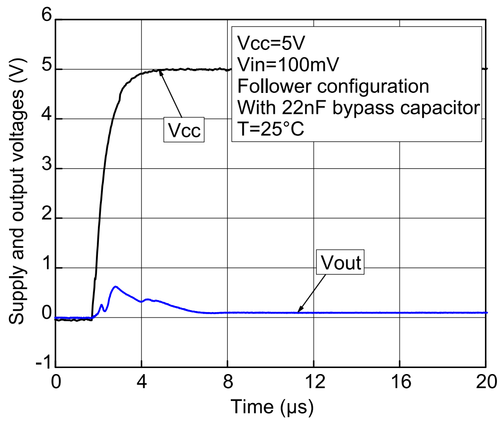


Figure 37: Startup behavior with a 22 nF bypass capacitor



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 SOT23-5 package information

Figure 38: SOT23-5 package outline

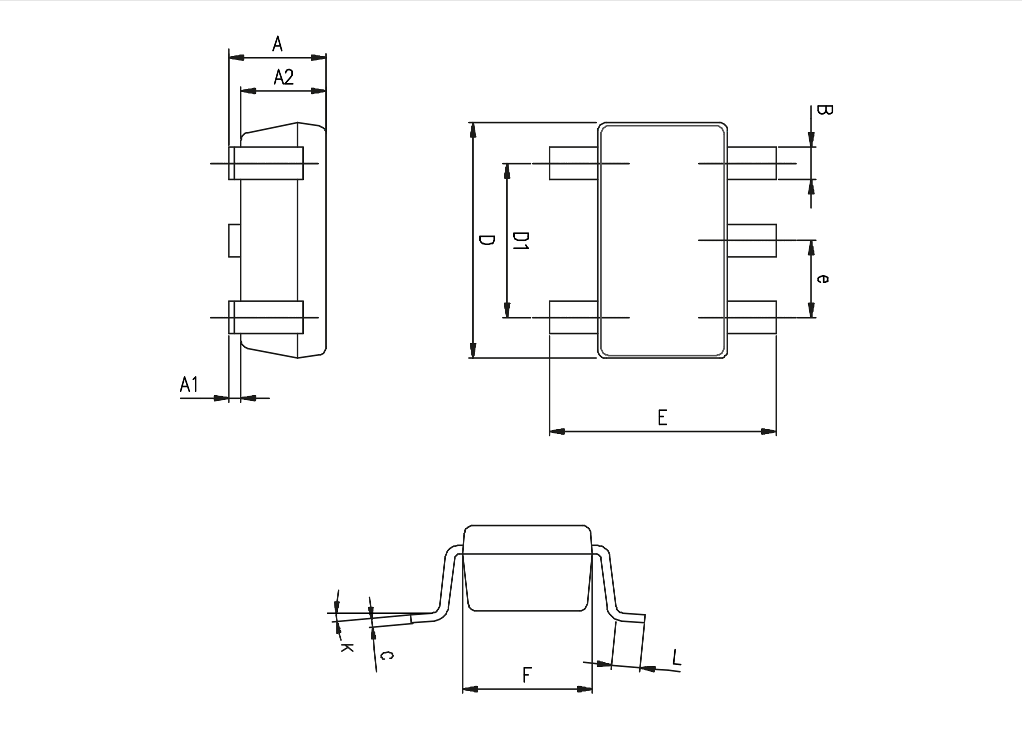


Table 6: SOT23-5 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0 degrees		10 degrees	0 degrees		10 degrees

5 Ordering information

Table 7: Order codes

Order code	Temperature range	Package	Packing	Marking
TSB611ILT	-40 °C to 125 °C	SOT23-5	Tape and reel	K191
TSB611IYLT [(1)]				K194

Notes:

[(1)]Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent on going.

6 Revision history

Table 8: Document revision history

Date	Revision	Changes
17-Aug-2015	1	Initial release