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Tsi384™
Evaluation Board User Manual

60E1000_MA001_08

September 2009

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Contents

About this Document

This document describes how to test the key features of the Tsi384 using the Tsi384 evaluation board. It can be used in conjunction with the Tsi384 Evaluation Board Schematics.

Related Information

- *Tsi384 User Manual*
- *Tsi384 Evaluation Board Schematics*
- *PCI Express Base Specification (Revision 1.1)*
- *PCI Express CEM Specification (Revision 1.1)*
- *PCI Express-to-PCI/PCI-X Bridge Specification (Revision 1.0)*
- *PCI-X Addendum to PCI Local Bus Specification (Revision 1.0a)*

Acronyms

Term	Definition
PCIe	PCI Express
PCI/X	PCI or PCI-X bus mode
SerDes	Serial/De-serializer

Revision History

60E1000_MA001_08, Formal, September 2009

This document was rebranded as IDT. It does not include any technical changes.

60E1000_MA001_07, Formal, May 2008

The following changes were made to this version:

- Completed various changes in response to the Tsi384 evaluation board's removal of support for an external arbiter (see "Arbitration").
- Updated the document to support Revision 1.0, Assembly number E1000_AS001_05 of the Tsi384 evaluation board. This assembly version includes the hardware changes listed in the following table.

Evaluation Board Changes – Assembly E1000_AS001_03

Item	Previous Usage/Definition	New Usage/Definition
U11/Tsi384 Bridge	Tsi384-133CLVZ	Tsi384-133ILVZ2
PCI_LOCKn pull-up	None	Add 4.7K +/-1K size 0603 resistor between pin B39 (LOCK#) and pin B41 (3.3V) on J2
3.3Vaux on J2	No connection	Short pin A14 (3.3Vaux) to pin A21 (3.3V) by wiring
3.3Vaux on J36 and J37	No connection	Short pin A14 (3.3Vaux) to pin A21 (3.3V) by wiring
JTAG signals pull-up	2K pull-up on R288, R293, R294, R295	Change to 10K instead
PCI reset	C231 was 1uF (0603) (0603ZD105KAT2A)	Changed to 10uF (0603) MFR P/N: ECJ-1VB0J106M

60E1000_MA001_06, Formal, January 2008

Corrected the descriptions of the S7 and S8 switches. Previously, these descriptions were reversed.

60E1000_MA001_05, Formal, October 2007

Added PCI pull-up resistor values to Table 3.

60E1000_MA001_04, Formal, May 2007

This document supports the Revision 1.0, Assembly number E1000_AS001_03 version of the Tsi384 evaluation board. This assembly version includes the hardware changes listed in the following table.

Evaluation Board Changes – Assembly E1000_AS001_03

Reference Designator	Description
Removals	
R13	Removed
Reworks	
Add 10 K Ohm pull-down to PCI_RST#	

60E1000_MA001_03, Formal, April 2007

This is the general release version of the document. There are no technical differences between this document and the previous version.

60E1000_MA001_02, Formal, March 2007

This document includes "Bill of Materials" for the Tsi384 evaluation board. It supports the Revision 1.0, Assembly number E1000_AS001_02 version of the Tsi384 evaluation board. This assembly version includes the hardware changes listed in the following table.

Evaluation Board Changes – Assembly E1000_AS001_02

Reference Designator	Description
Changes	
R88	Change to .015ohm
R242,R272,R6	Change to 1Kohm
C182,C183,C193, C189,C207,C202	Change to 2.2uF
R148	Populate
R150	Populate
C77,C45	Install
C235	Change to 300nF
R208	130 Ohm
R215	220 Ohm
R220	441 Ohm
R139	2260 Ohm
R144	220 Ohm
R196	441 Ohm
Removals	
R141	Remove
Reworks	
Add 1kohm resistor pull-up to LOCK#	

60E1000_MA001_01, Formal, March 2007

This is the first version of the *Tsi384 Evaluation Board User Manual*. This document supports the Revision 1.0, Assembly number E1000_AS001_01 version of the Tsi384 evaluation board.

1. Board Design

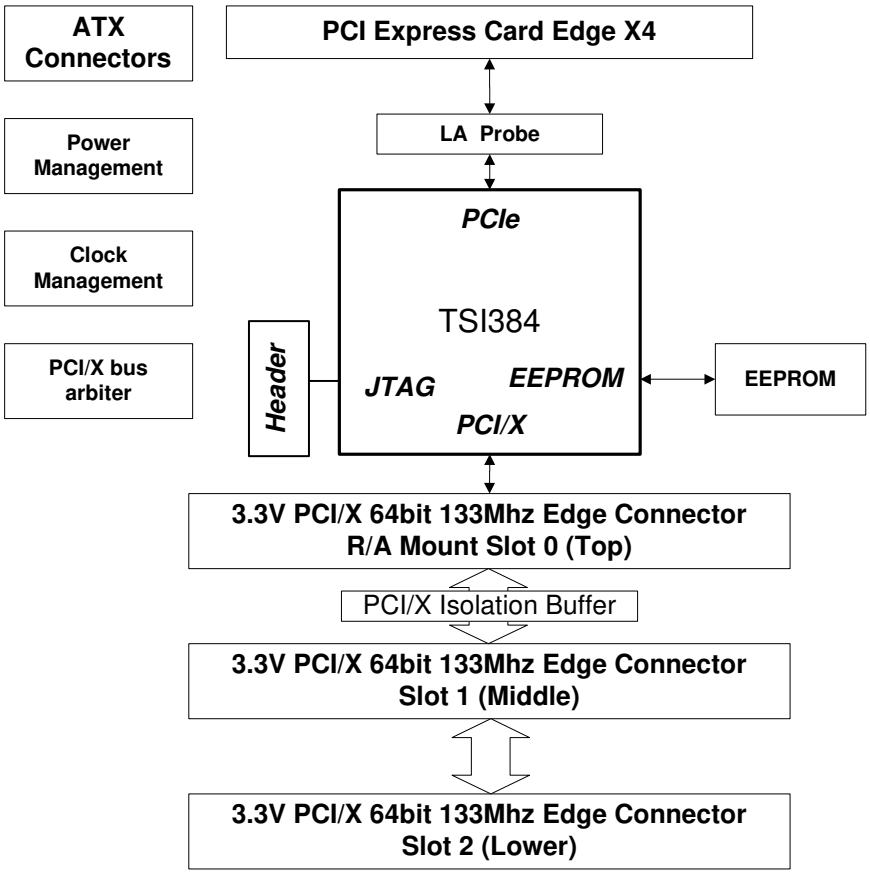
Topics discussed include the following:

1.1 Overview

The key features of the Tsi384 evaluation board include the following:

- Single x4 lane, 2.5 Gbps PCIe 1.1 compatible riser card (extended height form factor)
- Three PCI/X slots
- 32-/64-bit PCI/X bus, 25–133 MHz operation
- PCI/X power support through system or external supply
- PCIe compliance/debugging test points

Figure 1: Evaluation Board Block Diagram



1.2 PCI/X Interface

1.2.1 Overview

The PCI/X Interface is implemented on the board with three slots, in which one is an R/A mounted connector on the top of the board. All PCI/X connectors are compliant with the PCI/X 2.0b specification. Appropriate clearance is provided such that up to three PCI/X cards can be inserted for testing while the board is in an open-chassis standard ATX case.

The PCI/X Interface supports the configurations listed in Table 1.

Table 1: PCI/X Interface — Supported Configurations

Protocol	Operating Speed (MHz)	Number of Slots Supported
PCI	25, 33, 50, 66	3
PCI-X	50, 66	3
PCI-X	100	2
PCI-X	133	1

The support for PCI-X 133 MHz operation is possible with the use of an isolation buffer. The R/A connector located on the top of board is available in this maximum frequency. The PCI bus is routed forward and returned to the other slots to expand the bus for multi-slot support.

1.2.2 IDSEL Signals

IDSEL signals are connected in the following order:

- Slot 0 – R/A connector top slot: 2K ohms to AD16 (Device 0)
- Slot 1 – Vertical middle slot: 2K ohms to AD19 (Device 3)
- Slot 2 – Vertical lower slot: 2K ohms to AD18 (Device 2)

The 2K ohm resistor value is consistent with the ability of the Tsi384 to drive the AD lines 2 clock cycles prior in PCI mode, and 4 clock cycles prior in PCI-X mode. The PCI/X Interface is unterminated with the exception of the clock signals.

1.2.3 Interrupt Signals

The PCI interrupt signals are connected to the slots as shown in Table 2.

Table 2: PCI Interrupt Routing

Tsi384	Slot 0	Slot 1	Slot 2
A	A	D	C
B	B	A	D
C	C	B	A
D	D	C	B

1.2.4 PCI Pull-up Signals

The following signals have a pull-up resistor on the PCI bus.

Table 3: PCI Pull-up Signals

Signal	Description	Resistor Value
PCI_CBE#[4:7]	Byte enables for upper 32-bit AD lines	8.2K
PCI_REQ#[0:3]	Bus request	8.2K
PCI_GNT#[0:3]	Bus grant	8.2K
PCI_FRAME#	Control signal	8.2K
PCI_IRDY#, PCI_TRDY#	Control signal	8.2K
PCI_STOP#	Control signal	8.2K
PCI_SERR#	System error	8.2K
PCI_PERR#	Parity error	8.2K
PCI_PAR	Parity of lower 32-bit lines and CBE bus	8.2K
PCI_PAR64	Parity of upper 32-bit AD lines and CBE bus	8.2K
PCI_DEVSEL#	Device select line	8.2K
PCI_INT#[A:D]	Interrupt line	2.4K
PCI_PME#	PCI Power Management Event occurred	8.2K

1.2.5 Arbitration

The Tsi384 evaluation board has provisions to implement an external arbiter; however, the current PCB assembly does not have the external arbiter implemented. Therefore, the only valid mode of operation is internal arbiter enabled.

1.3 PCIe Interface

The Tsi384 evaluation board implements a four-line PCIe interface. It is designed to connect onto a PCIe system with a standard x4 finger connector. The system must provide the REFCLK and PERSTN signals. The PCIe interface has the following design elements:

- Supports Hot insertion and removal
- Mid-bus logic analyzer pads for PCIe RXD/TXD signal probing
- AC coupling on the TXD lanes
- JTAG TDI - TDO loopback for chain continuity

1.4 Power Management

1.4.1 Power Regulation

The evaluation board's power regulation is implemented as follows:

- Digital 3.3V power supply available from DC/DC regulator or ATX supply
- Digital 1.2V switching regulator
- PCIe supplies filtered using EMI ferrite networks

To support PCI/X cards, the following additional power resources are included:

- 12V to 5V DC/DC converter
- 12V to 3.3V DC/DC converter
- External power connectors – ATX 20-pin connector for supplying all power from an ATX power supply

1.4.2 Power Requirements

The power requirements and implementation for the Tsi384 is as follows.

Table 4: Tsi384 Power Requirements

Supply Name	Symbol	Supplied Source
Device Core	1.2V_384	DC/DC switching regulator w/Enable pin
PCIe 1.2V Core	1.2V_A_384	Passive Filter
PCI 3.3v supply	3.3V_384	Power switch w optional Ferrite filter to reduce EMI/noise from PCI environment
PCIe 3.3v supply	3.3V_A_384	Passive Filter

The target power draw of the Tsi384 is a maximum of 2 Watts, all supplies combined. The supplies to the Tsi384 are controlled during ramp up using enable pins on regulators and switches.

1.4.2.1 PCIe

The PCIe CEM Specification 1.1 defines power limits on PCIe slots according to the number of lanes available on the card. Power rules regarding x4 PCIe slots are a maximum of 25W slot. Current limits are included in Table 5.

Table 5: PCIe Connector Current Limits

Rail	Current
3.3V	3A
12V	2.1A

In both cases (x4 or x16), the usage of the 12V supply provides access to the full 25W/75W available from the system to the board. The PCIe pinout design includes more 12V power pins as it allows more power-per-pin capability. The evaluation board regulates all power from the 12V system rail; however, 3.3V from the system remains unused.

1.4.2.2 PCI/X

The PCISIG defines the power rules regarding PCI/X cards as a maximum of 25 Watts per card (All power rails combined power draw). The individual current limits on voltage rails are included in Table 6.

Table 6: PCI/X Connector current limits

Rail	Current
3.3v	7.6a
5v	5a
-12v	100ma
12v	500ma

It is not possible “within spec” to provide the full power required to the PCI/X without violating the specification while drawing power from only a x4 PCIe system. Up to 23W not including regulator efficiency losses can be made available. The evaluation board provides the power requirements in one of two ways depending on the application:

- PCIe system power
- ATX System connector

The following conditions summarize the power available for a single PCI/X card without external supply. An efficiency of 85% is taken into account for switching regulators. These limits can be exceeded in cases where the system can provide more than the suggested limit, which is usually only implemented in hot swap systems.

Table 7: PCI/X Connector Current Limit with No External Supply

Rail	Supplying Topology	Current (Maximum)
3.3V	12V to 3.3V regulator	6A
12V	12V directly	500mA
-12V	N/A	N/A
5V	12V to 5V regulator	4A

For additional slots, or in cases where the system cannot supply enough power, a separate ATX power connector is used to power the card. The evaluation board senses the presence of this supply, and disables the slave PCIe slot power. For the case of a separate external ATX supply, all three slots are provided with the required power.

1.4.3 Power Sequencing

On power-up, the card power sequencing is as follows:

1. 1.2V powered on
2. PCI/X I/O slot power and pull-ups, and Tsi384 3.3V

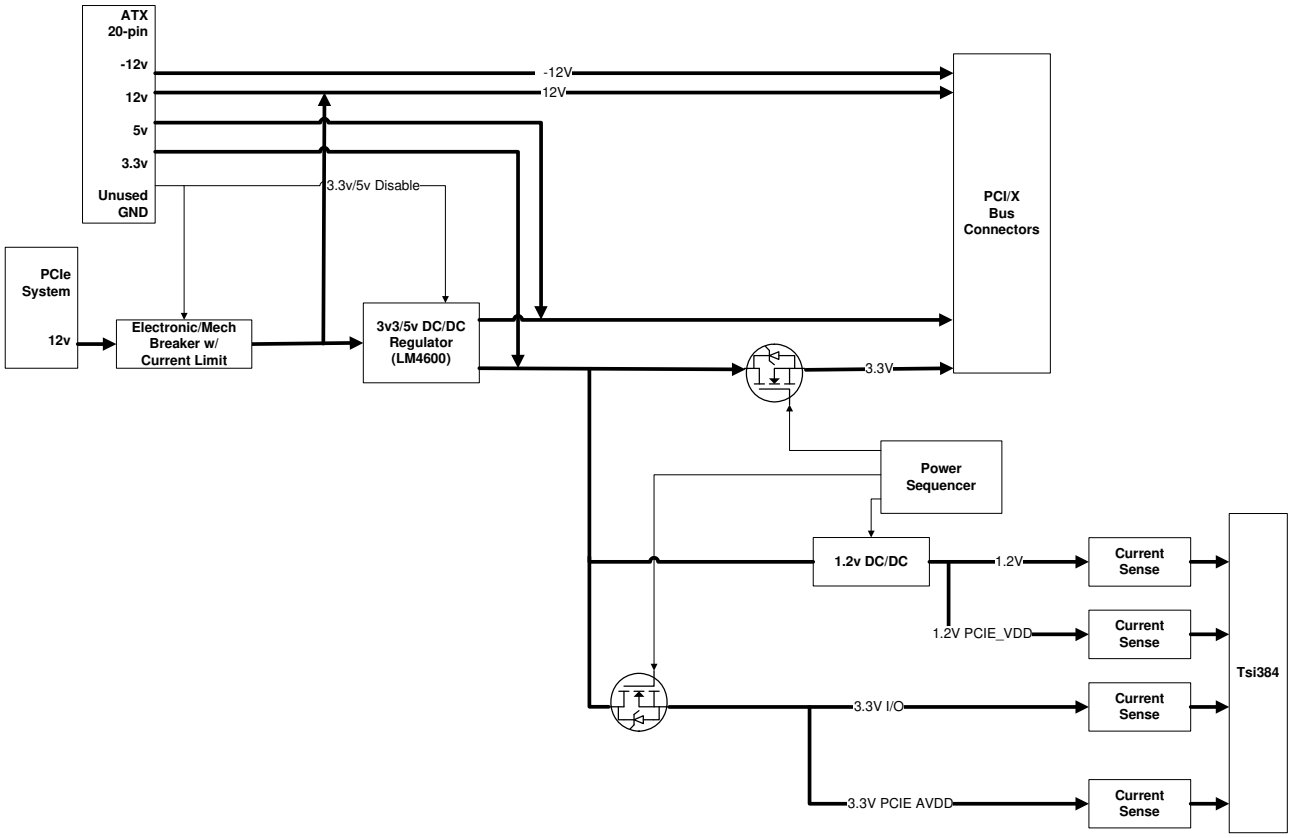
12V/-12V/5V PCI are not sequence controlled.

1.4.4 System Power Design

Figure 2 illustrates the power distribution for the riser card. The following list is a functional summary of the power design:

1. Sequencing control over the following rails:
   - 3.3V PCI
   - 3.3V Tsi384 I/O/PCIe A_{VDD}
   - 1.2V Tsi384 Core/PCIe V_{DD}
2. ATX 20-pin connector override, which disables all power draw from the PCIe system
3. Current sensing of Tsi384 supplies

Figure 2: System Power Distribution



1.5 Clock Management

The Tsi384 requires up to two input clocks to operate:

- 25–133MHz clock for PCI/X
- 100-MHz reference clock for PCIe

The PCI/X and PCIe input clocks are briefly discussed.

1.5.1 PCI/X

The evaluation board supports master and slave clocking for PCI/X.

- Master – When in master mode, the Tsi384 generates the required PCI/X clock for all slots.
- Slave – When in slave mode, an on-board selectable 25–133 MHz clock generator is used as follows:

— Low skew distribution buffer to all slots and Tsi384

— External clock input for any optional testing

To multiplex the sources of two clocks, passive resistor muxes are located at the endpoints of the clock nets. For more information, see the *Tsi384 Evaluation Board Schematic (60E1000_SC002)*.

1.5.1.1 PCIe

For PCIe clocking, a 100-MHz differential HCSL clock source is required. The clock source is available in two forms:

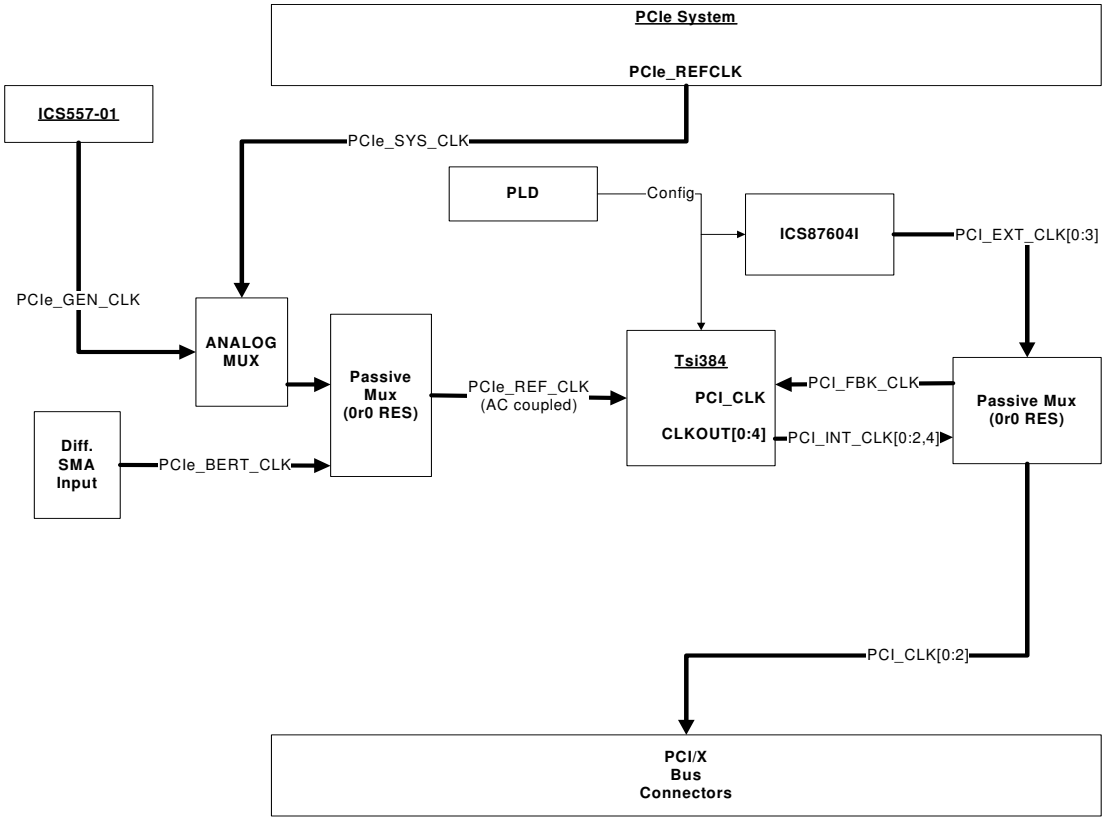
- Edge connector clock source – This clock source synchronizes the system SerDes with the Tsi384.
- On-board 100-MHz reference – This clock source can separate the clock domains between the bridge and the root complex.

The two PCIe clock sources are multiplexed with an analog multiplexer to select between the system clock or on-board clock (see Figure 3).

1.5.2 System Clock Distribution

Figure 3 shows the distribution of the system clock on the Tsi384 evaluation board.

Figure 3: System Clock Distribution



1.6 Other Interfaces

1.6.1 JTAG Interface

To support debug and testing of device, JTAG access to the Tsi384 is available using a standard JTAG header for Wiggler connection.

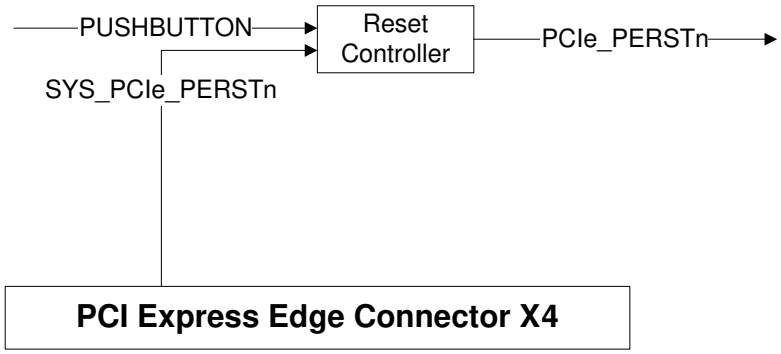
1.6.2 EEPROM Interface

A single EEPROM device socket is available for programming registers during startup. The socket is in an 8-pin DIP format.

1.7 Hardware Reset

Figure 4 illustrates the reset options of the Tsi384 evaluation board.

Figure 4: Board Reset



Three levels of reset are available:

- Cold reset – This reset is applied during power up. System (card edge) PCIe_PERSTn is muxed with the board's reset controller.
- Warm reset – This reset is activated by a push-button reset on the board.
- Hot reset – This reset is activated by the in-band message sent by the root complex. No supporting hardware is necessary.

For more information on cold, warm, and hot reset levels, see the "Resets, Clocking, and Initialization Options" chapter in the *Tsi384 User Manual*.

1.8 Logic Analyzer Connectivity

The serial buses have Midbus pads (TMS818 probe) for visibility of SerDes lines using a pre-processor. Each probing pad provides access to the RX and TX segments of a x4 link.

To access the PCI/X bus, a Nexus PCI/X interposer card can be used with Tektronix mictor cables. The card can be plugged into any PCI edge slot, or in-line with the device under test.

2. Configurable Options

Topics discussed include the following:

2.1 Switches

2.1.1 DIP Switches

Switches S1 to S6 combine four, small slide switches identified with numbers 1 to 4 (see Table 8 for individual switch definition).

Figure 5: DIP Switch Package/Individual Switch Position

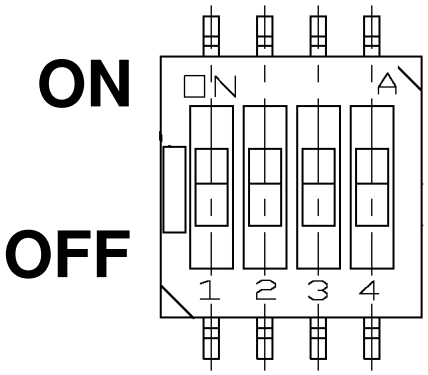
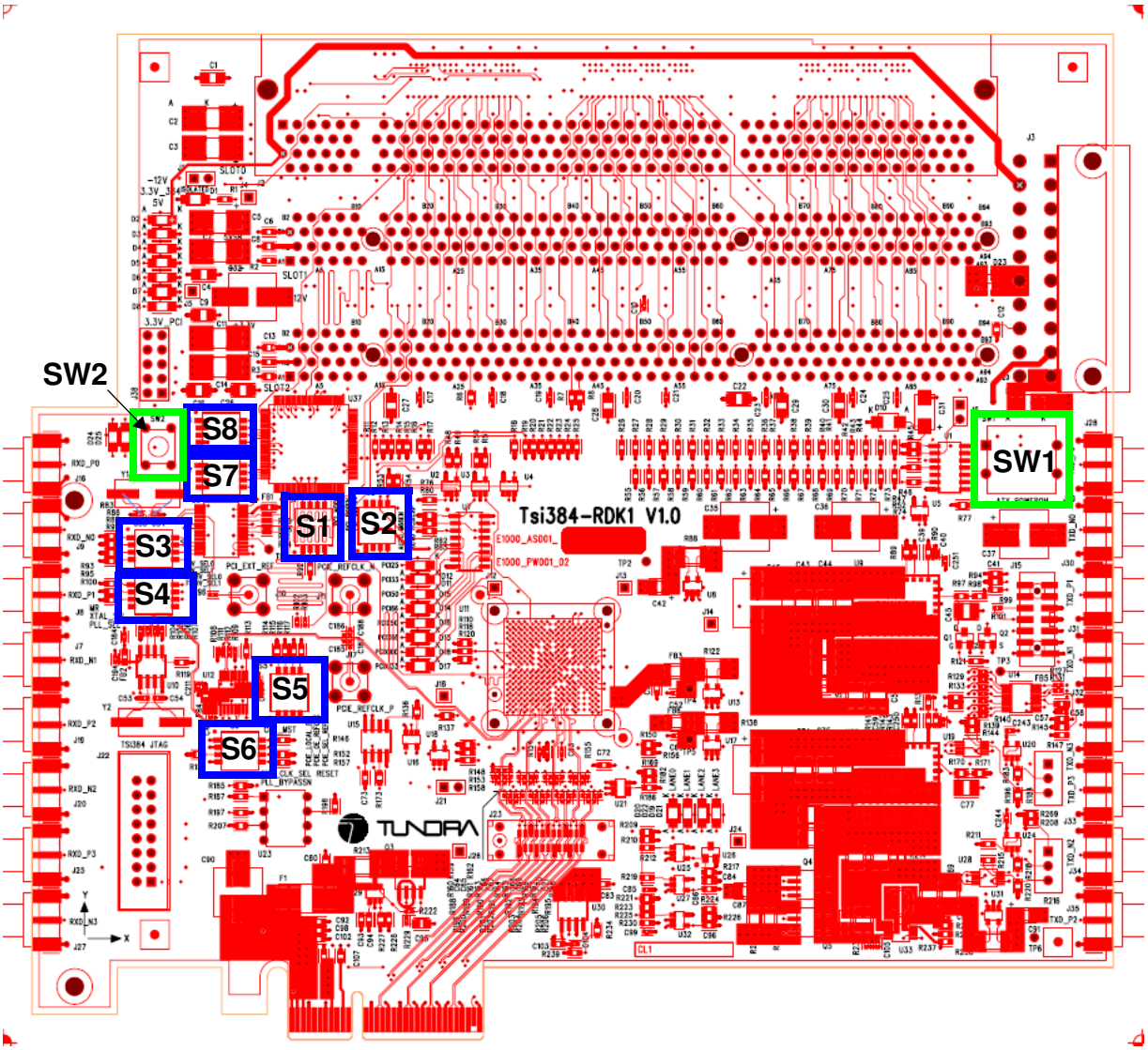


Figure 6: Switch Locations



Switch S1 is used to manually set PCI/X bus modes.

Table 8: S1 Settings

Switch Number	Description	Default Setting	On/Off Setting
1	PCIXCAP setting	OFF	ON = Forces Tsi384's PCIXCAP input to ground OFF = Tsi384's PCIXCAP input has a weak pull up to 3.3V
2	PCIXCAP setting	OFF	ON = Tsi384's PCIXCAP input has a weak pull down to ground OFF = Tsi384's PCIXCAP input has a weak pull up to 3.3V
3	M66EN setting	OFF	ON = Forces Tsi384's M66EN input to ground OFF = Tsi384's M66EN input has a weak pull up to 3.3V
4	PCI_SEL100 setting	ON	ON = Forces Tsi384's PCI_SEL100 input to ground OFF = Tsi384's PCI_SEL100 input has a weak pull up to 3.3V

Table 9: Bus Mode Setting for S1 (Assumes S2.3 and S2.4 are OFF)

Switch Setting (Switch 1 - 2 - 3 - 4)	Signal Setting	Bus Mode
OFF - OFF - x - OFF	PCIXCAP = High M666EN = x PCI_SEL100 = High	PCIX 100 MHz
OFF - OFF - x - ON	PCIXCAP = High M666EN = x PCI_SEL100 = Low	PCIX 133 MHz
OFF - ON - x - OFF	PCIXCAP = pull-down M666EN = x PCI_SEL100 = High	PCIX 50 MHz
OFF - ON - x - ON	PCIXCAP = pull-down M666EN = x PCI_SEL100 = Low	PCIX 66 MHz
ON - x - OFF - OFF	PCIXCAP = Low M666EN = High PCI_SEL100 = High	PCI 50 MHz
ON - x - OFF - ON	PCIXCAP = Low M666EN = High PCI_SEL100 = Low	PCI 66 MHz

Table 9: Bus Mode Setting for S1 (Assumes S2.3 and S2.4 are OFF) *(Continued)*

Switch Setting (Switch 1 - 2 - 3 - 4)	Signal Setting	Bus Mode
ON - x - ON - OFF	PCIXCAP = Low M666EN = Low PCI_SEL100 = High	PCI 25 MHz
ON - x - ON - ON	PCIXCAP = Low M666EN = Low PCI_SEL100 = Low	PCI 33 MHz

Switch S2 is used to connect PCI bus mode signal to the Tsi384.

Table 10: S2 Settings

Switch Number	Description	Default Setting	On/Off Setting
1	No function	-	-
2	No function	-	-
3	Bus M66EN connection	ON	ON = Connect the PCI M66EN signal to the Tsi384 OFF = Disconnect the PCI M66EN from the Tsi384
4	Bus PCIXCAP connection	ON	ON = Connect the PCI PCIXCAP signal to the Tsi384 OFF = Disconnect the PCI PCIXCAP from the Tsi384

Note that S1 and S2 operate together. When the S2 switches are ON, the S1 setting applies to the whole bus. For example, when PCIXCAP is connected to the Tsi384 (S2.4 ON), and PCIXCAP is forced to ground (S1.1 ON), the whole bus will see PCIXCAP low.

Switches S3 and S4 are used to set the PCI/X bus external clock frequency. By default the PCI/X bus clock source is the Tsi384. The external clock can only be connected to the PCI/X bus by replacing resistors on the board. When an external clock source is used, an on-board PLL is used to set the proper bus clock frequency. Table 11 contains the clock frequency settings for S3.

Table 11: S3 Settings

Switch Number	Description	Default Setting	On/Off Setting
1	DIV_SEL0	OFF	[FBDIV_SEL1, FBDIV_SEL0, DIV_SEL1, DIV_SEL0] ON = 1 OFF = 0 0,0,0,0 = x 4 0,0,0,1 = x 3 0,0,1,0 = x 2 0,0,1,1 = x 1 0,1,0,0 = x 5.33 0,1,0,1 = x 4 0,1,1,0 = x 2.667 0,1,1,1 = x 1.33 1,0,0,0 = x 6.667 1,0,0,1= x 5 1,0,1,0= x 3.33 1,0,1,1= x 1.67 1,1,0,0= x 8 1,1,0,1= x 6 1,1,1,0= x 4 1,1,1,1= x 2
2	DIV_SEL1	OFF	
3	FBDIV_ SEL0	OFF	
4	FBDIV_ SEL1	OFF	

Switch S4 controls the external clock PLL.

Table 12: S4 Settings

Switch Number	Description	Default Setting	On/Off Setting
1	PLL Reset	ON	ON = PLL in reset. PLL clock outputs are low. OFF = PLL is active and clock outputs are enabled.
2	XTAL select	OFF	ON = Clock source for PLL is reference clock from connector J10 OFF = Clock source for PLL is a 25-MHz oscillator.
3	PLL select	OFF	ON = PLL is bypassed. OFF = PLL is enabled. External clock source is multiplied as per S3 setting
4	No function	-	-

Switch S5 controls the PCIe clock multiplexer and the on-board PCIe reference clock PLL.

Table 13: S5 Settings

Switch Number	Description	Default Setting	On/Off Setting
1	No Function	-	-
2	PCIe on-board PLL enable	ON	ON = On-board PCIe reference clock PLL disabled. OFF = On-board PCIe reference clock PLL enabled.
3	PCIe clock multiplexer enable	OFF	ON = On-board PCIe clock multiplexer disabled. OFF = On-board PCIe clock multiplexer enabled.
4	PCIe clock source select	OFF	ON = On-board PCIe reference clock is used. OFF = System PCIe reference clock is used.

Switch S6 configures Tsi384's power-up options.

Table 14: S6 Settings

Switch Number	Description	Default Setting	On/Off Setting
1	Clock Master option	OFF	ON = Tsi384 is clock slave on the PCI/X bus OFF = Tsi384 is clock master on the PCI/X bus (clock master mode)
2	Internal arbiter option	OFF	ON = Internal arbiter is disabled OFF = Internal arbiter is enabled
3	PCI-X clock selection	ON	ON = When in clock master mode, the Tsi384 uses the clock on PCI_CLK compensated through the PLL to time the PCI-X Interface. OFF = When in clock master mode, the Tsi384 uses the internal clock generated from REFCLK to time the PCI-X Interface.
4	PCI-X PLL bypass	OFF	ON = PLL is bypassed. OFF = PLL is enabled.

These switches are not used.

Table 15: S7 and S8 Settings

Switch Number	Description	Default Setting	On/Off Setting
1	No function	-	-
2	No function	-	-
3	No function	-	-
4	No function	-	-

2.1.2 Push Button

SW1 is used to turn the ATX power supply ON. This switch is used only when the evaluation board is powered up with a stand-alone ATX power supply.

SW2 is used to reset the evaluation board. When pushing the reset button, the board is reset the same way a PCIe system reset would reset the board.