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IDT® Tsi572
Serial RapidIO Switch

Hardware Manual

May 18, 2012

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Contents

About this Document

This section discusses general document information about the Tsi572. The following topics are described:

Scope

The *Tsi572 Hardware Manual* discusses electrical, physical, and board layout information for the Tsi572. It is intended for hardware engineers who are designing system interconnect applications with these devices.

Document Conventions

This document uses a variety of conventions to establish consistency and to help you quickly locate information of interest. These conventions are briefly discussed in the following sections.

Non-differential Signal Notation

Non-differential signals are either active-low or active-high. An active-low signal has an active state of logic 0 (or the lower voltage level), and is denoted by a lowercase "b". An active-high signal has an active state of logic 1 (or the higher voltage level), and is not denoted by a special character. The following table illustrates the non-differential signal naming convention.

State	Single-line signal	Multi-line signal
Active low	NAME_b	NAMEn[3]
Active high	NAME	NAME[3]

Differential Signal Notation

Differential signals consist of pairs of complement positive and negative signals that are measured at the same time to determine a signal's active or inactive state (they are denoted by "_p" and "_n", respectively). The following table illustrates the differential signal naming convention.

State	Single-line signal	Multi-line signal
Inactive	NAME_p = 0 NAME_n = 1	NAME_p[3] = 0 NAME_n[3] =1
Active	NAME_p = 1 NAME_n = 0	NAME_p[3] is 1 NAME_n[3] is 0

Symbols

This symbol indicates a basic design concept or information considered helpful.

This symbol indicates important configuration information or suggestions.

This symbol indicates procedures or operating levels that may result in misuse or damage to the device.

Revision History

May 18, 2012, Formal

- Updated the first paragraph in "Power Sequencing" on page 33
- Changed the SP_IO_SPEED setting in Table 21 for 125 MHz / 1.25 Baud rate to 1,1

November 18, 2010, Formal

- Added a note to Table 13

August 2009, Formal

This is the current release of the *Serial RapidIO Switch.* There have been no technical changes to the document; the formatting has been updated to reflect IDT.

June 2009, Formal

Changes have been implemented throughout the document.

July 2008, Advance

The changes to this documents includes adding industrial variants of the device to “Ordering Information” on page 87.

June 2008, Advance

This was the first version of the *Serial RapidIO Switch*.

1. Signals and Package

This chapter describes the packaging (mechanical) features for the Tsi572. It includes the following information:

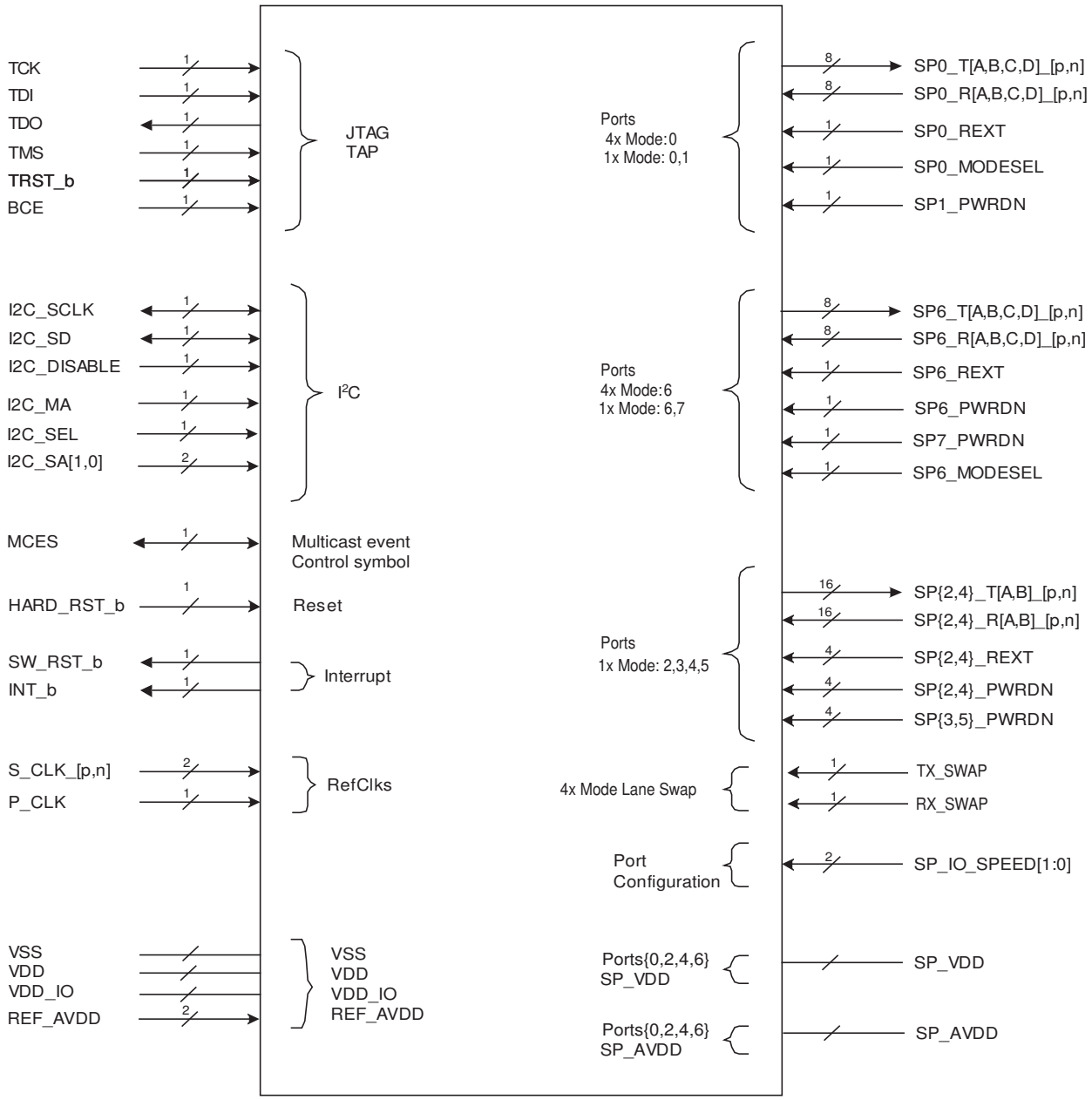
1.1 Pinlist

The pinlist and ballmap information for the Tsi572 are available by visiting www.idt.com. For more information, see the following documents:

- *Tsi572 Pinlist*
- *Tsi572 Ballmap*

1.2 Signals

Figure 1: Signal Grouping



1.2.1 Conventions

The following conventions are used in the signal description table:

- Signals with the suffix "_p" are the positive half of a differential pair.
- Signals with the suffix "_n" are the negative half of a differential pair.
- Signals with the suffix "_b" are active low.

Signals are classified according to the types defined in Table 1.

Table 1: Signal Types

Pin Type	Definition
I	Input
O	Output
I/O	Input/Output
OD	Open Drain
SRIO	Differential driver/receiver defined by *RapidIO Interconnect Specification (Revision 1.3)*
PU	Pulled Up internal to the Tsi572
PD	Pulled Down internal to the Tsi572
LVTTL	CMOS I/O with LVTTL thresholds
Hyst	Hysteresis
Core Power	Core supply
Core Ground	Ground for core logic
I/O Power	I/O supply
N/C	No connect These signals must be left unconnected.

1.2.2 Endian Ordering

This document follows the bit-numbering convention adopted by *RapidIO Interconnect Specification (Revision 1.3)*, where [0:7] is used to represent an 8 bit bus with bit 0 as the most-significant bit.

1.2.3 Port Numbering

The following table shows the mapping between port numbers and the physical ports. These port numbers are used within the destination ID lookup tables for ingress RapidIO ports and in numerous register configuration fields.

Table 2: Port Numbering

Port Number	RapidIO Port	Mode
0	Serial Port 0 (SP0)	1x or 4x
1	Serial Port 1 (SP1)	1x
2	Serial Port 2 (SP2)	1x
3	Serial Port 3 (SP3)	1x
4	Serial Port 4 (SP4)	1x
5	Serial Port 5 (SP5)	1x
6	Serial Port 6 (SP6)	1x or 4x
7	Serial Port 7 (SP7)	1x

1.2.4 Signal Grouping

The following table lists the signals by group and their recommended termination.

Table 3: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
Signal Port Numbering **n = 0, 2, 4, 6**			
Serial Port Transmit			
SP{n}_TA_p	O, SRIO	Port n Lane A Differential Non-inverting Transmit Data output (4x mode) Port n Lane A Differential Non-inverting Transmit Data output (1x mode)	No termination required.
SP{n}_TA_n	O, SRIO	Port n Lane A Differential Inverting Transmit Data output (4x mode) Port n Lane A Differential Inverting Transmit Data output (1x mode)	No termination required.
SP{n}_TB_p	O, SRIO	Port n Lane B Differential Non-inverting Transmit Data output (4x mode) Port n+1 Lane B Differential Non-inverting Transmit Data output (1x mode)	No termination required.
SP{n}_TB_n	O, SRIO	Port n Lane B Differential Inverting Transmit Data output (4x mode) Port n+1 Lane B Differential Inverting Transmit Data output (1x mode)	No termination required.
SP[0,6]_TC_p	O, SRIO	Port n Lane C Differential Non-inverting Transmit Data output (4x mode)	No termination required.
SP[0,6]_TC_n	O, SRIO	Port n Lane C Differential Inverting Transmit Data output(4x mode)	No termination required.
SP[0,6]_TD_p	O, SRIO	Port n Lane D Differential Non-inverting Transmit Data output (4x mode)	No termination required.
SP[0,6]__TD_	O, SRIO	Port n Lane D Differential Inverting Transmit Data output (4x mode)	No termination required.

Table 3: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
Serial Port Receive			
SP{n}_RA_p	I, SRIO	Port n Lane A Differential Non-inverting Receive Data input (4x node) Port n Lane A Differential Non-inverting Receive Data input (1x mode)	DC blocking capacitor of 0.1uF in series
SP{n}_RA_n	I, SRIO	Port n Lane A Differential Inverting Receive Data input (4x mode) Port n Lane A Differential Inverting Receive Data input (1x mode)	DC blocking capacitor of 0.1uF in series
SP{n}_RB_p	I, SRIO	Port n Lane B Differential Non-inverting Receive Data input (4x mode) Port n+1 Lane B Differential Non-inverting Receive Data input (1x mode)	DC blocking capacitor of 0.1uF in series
SP{n}_RB_n	I, SRIO	Port n Lane B Differential Inverting Receive Data input (4x mode) Port n+1 Lane B Differential Inverting Receive Data input (1x mode)	DC blocking capacitor of 0.1uF in series
SP[0,6]_RC_p	I, SRIO	Port n Lane C Differential Non-inverting Receive Data input(4x mode)	DC blocking capacitor of 0.1uF in series
SP[0,6]_RC_n	I, SRIO	Port n Lane C Differential Inverting Receive Data input (4x mode)	DC blocking capacitor of 0.1uF in series
SP[0,6]_RD_p	I, SRIO	Port n Lane D Differential Non-inverting Receive Data input(4x mode)	DC blocking capacitor of 0.1uF in series
SP[0,6]_RD_n	I, SRIO	Port n Lane D Differential Inverting Receive Data input (4x mode)	DC blocking capacitor of 0.1uF in series

Table 3: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
Serial Port Configuration			
SP{n}_REXT	Analog	Used to connect a resistor to VSS to provide a reference current for the driver and equalization circuits.	Must be connected to VSS with a 191-ohm (1%) resistor.
SP{n}_MODESEL	I/O, LVTTL, PD	Selects the serial port operating mode for ports 0and 6 0 = Port 0 or 6 operating in 4x mode 1 = Ports n and n+1 operating in 1x mode Note: Output capability of this pin is only used in test mode. Must remain stable for 10 P_CLK cycles after HW_RST_b is de-asserted in order to be sampled correctly. This signal is ignored after reset.	Pin must be tied off according to the required configuration. Either a 10K pull up to VDD_IO or a 10K pull-down to VSS_IO. Internal pull-down may be used for logic 0.
SP{n}_PWRDN	I/O, LVTTL, PU	Port n Transmit and Receive Power Down control This signal controls the state of Port n *and Port n+1* The PWRDN controls the state of all four lanes (A/B/C/D) of SERDES Macro. 0 = Port n Powered Up. Port n+1 controlled by SP{n+1}_PWRDN. 1 = Port n Powered Down. Port n+1 Powered Down. Override SP{n}_PWRDN using PWDN_x1 field in “SRIO MAC x Clock Selection Register” in the *Tsi572 User Manual*. Output capability of this pin is only used in test mode. Must remain stable for 10 P_CLK cycles after HW_RST_B is de-asserted in order to be sampled correctly. This signal is ignored after reset.	Pin must be tied off according to the required configuration. Either a 10K pull up to VDD_IO or a 10K pull-down to VSS_IO. Internal pull-up may be used for logic 1.

Table 3: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
SP{n+1}_PWRDN	I/O, LVTTL, PU	Port n+1 Transmit and Receive Power Down control This signal controls the state of Port n+1. Note that Port n+1 is never used when 4x mode is selected for a Serial Rapid IO MAC, and it must be powered down. 0 = Port n+1 Powered Up 1 = Port n+1 Powered Down Override SP{n+1}_PWRDN using PWDN_x4 field SRIO MAC x Clock Selection Register. Output capability of this pin is only used in test mode. Must remain stable for 10 P_CLK cycles after HW_RST_B is de-asserted in order to be sampled correctly. This signal is ignored after reset.	Pin must be tied off according to the required configuration. Either a 10K pull up to VDD_IO or a 10K pull-down to VSS_IO. Internal pull-up may be used for logic 1.

Table 3: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
Serial Port Speed Select			
SP_IO_SPEED[1]	I/O, LVTTL, PU	Serial Port Transmit and Receive operating frequency select, bit 1. When combined with SP_IO_SPEED[0], this pin selects the default serial port frequency for all ports. 00 = 1.25 Gbit/s 01 = 2.5 Gbit/s 10 = 3.125 Gbit/s (default) 11 = Illegal Selects the speed at which the ports operates when reset is removed. This could be at either HARD_RST_b being de-asserted or by the completion of a self-reset. These signals must remain stable for 10 P_CLK cycles after HW_RST_b is de-asserted in order to be sampled correctly. These signals are ignored after reset and software is able to over-ride the port frequency setting in the SRIO MAC x Digital Loopback and Clock Selection register. The SP_IO_SPEED[1:0] setting is equal to the IO_SPEED field in SRIO MAC x Clock Selection Register. Output capability of this pin is only used in test mode.	Pin must be tied off according to the required configuration. Either a 10K pull-up to VDD_IO or a 10K pull-down to VSS_IO. Internal pull-down may be used for logic 0.
SP_IO_SPEED[0]	I/O, LVTTL, PD	See SP_IO_SPEED[1]	Pin must be tied off according to the required configuration. Either a 10K pull-up to VDD_IO or a 10K pull-down to VSS_IO. Internal pull-up may be used for logic 1.

Table 3: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
Serial Port Lane Ordering Select			
SP_RX_SWAP	I, LVTTL, PD	Configures the order of 4x receive lanes on serial ports [0,6] 0 = A, B, C, D 1 = D, C, B, A This signal is ignored in 1X mode. Must remain stable for 10 P_CLK cycles after HARD_RST_b is de-asserted in order to be sampled correctly. This signal is ignored after reset. Note: Ports that require the use of lane swapping for ease of routing will only function as 4x mode ports. The re-configuration of a swapped port to dual 1x mode operation results in the inability to connect to a 1x mode link partner.	No termination required. Internal pull-down can be used for logic 0. Pull up to VDD_IO through 10K if external pull-up is desired. Pull down to VSS_IO through a 10K resistor if an external pull-down is desired.
SP_TX_SWAP	I, LVTTL, PD	Configures the order of 4x transmit lanes on serial ports [0,6]. 0 = A, B, C, D 1 = D, C, B, A Must remain stable for 10 P_CLK cycles after HARD_RST_b is de-asserted in order to be sampled correctly. This signal is ignored after reset. Note: Ports that require the use of lane swapping for ease of routing only function as 4x mode ports. The re-configuration of a swapped port to dual 1x mode operation results in the inability to connect to a 1x mode link partner.	No termination required. Internal pull-down can be used for logic 0. Pull up to VDD_IO through 10K if external pull-up is desired. Pull down to VSS_IO through 10K resistor if an external pull-down is desired.
Clock and Reset			
P_CLK	I, LVTTL	This clock is used for the register bus clock. The nominal frequency of this input clock is 100 MHz. For more information on programming the P_CLK operating frequency, refer to “P_CLK Programming” on page 75.	No termination required.

Table 3: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
S_CLK_p	I, CML	Differential non-inverting reference clock. The clock is used for following purposes: SERDES reference clock, serial port system clock, ISF clock and test clock. The maximum frequency of this input clock is 156.25 MHz. The clock frequency is defined in "Reference Clock, S_CLK_p/n" on page 35. For more information on the S_CLK operating frequency, refer to "Line Rate Support" on page 71.	AC coupling capacitor of 0.1uF required.
S_CLK_n	I, CML	Differential inverting reference clock. The clock is used for following purposes: SerDes reference clock, serial port system clock, ISF clock and test clock. The maximum frequency of this input clock is 156.25 MHz. The clock frequency is defined in "Reference Clock, S_CLK_p/n" on page 35. For more information on the S_CLK operating frequency, refer to "Line Rate Support" on page 71.	AC coupling capacitor of 0.1uF required.
HARD_RST_b	I LVTTL, Hyst, PU	Schmidt-triggered hard reset. Asynchronous active low reset for the entire device. The Tsi572 does not contain a voltage detector to generate internal reset.	Connect to a power-up reset source. Refer to "Reset Requirements" on page 64
Interrupts			
INT_b	O, OD, LVTTL, 2mA	Interrupt signal (open drain output)	External pull-up required. Pull up to VDD_IO through a 10K resistor.

Table 3: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
SW_RST_b	O, OD, LVTTL, 2mA	Software reset (open drain output): This signal is asserted when a RapidIO port receives a valid reset request on a RapidIO link. If self-reset is not selected, this pin remains asserted until the reset request is cleared from the status registers. If self-reset is selected, this pin remains asserted until the self reset is complete. If the Tsi572 is reset from the HARD_RST_b pin, this pin is de-asserted and remains de-asserted after HARD_RST_b is released. For more information, refer to “Resets” in the Tsi572 User’s Manual.	External pull-up required. Pull up to VDD_IO through a 10K resistor.
Multicast			
MCES	I/O, LVTTL, PD	Multicast Event Symbol pin. As an input, an edge (rising or falling) will trigger a Multicast Event Control Symbol will be sent to all ports; As an output, this pin will toggle its value every time an Multicast Event Control Symbol is received by any port which is enabled for Multicast even control symbols. Must remain stable for 10 P_CLK cycles *before and after* a transition.	No termination required. This pin must not be driven by an external source until all power supply rails are stable.
I^2C			
I2C_SCLK	I/O, OD, LVTTL, PU 8mA	I^2C input/output clock, up to 100 kHz. If an EEPROM is present on the I^2C bus, this clock signal must be connected to the clock input of the serial EEPROM on the I^2C bus. If an EEPROM is not present, the recommended terminations should be used.	No termination required. Internal pull-up may be used for logic 1. Pull up to VDD_IO through a minimum 470 ohms resistor if higher edge rate is required.
I2C_SD	I/O, OD, LVTTL, PU 8mA	I^2C input and output data bus (bidirectional open drain)	No termination required. Internal pull-up may be used for logic 1. Pull up to VDD_IO through a minimum 470 ohms resistor if higher edge rate required.

Table 3: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
I2C_DISABLE	I, LVTTL, PD	Disable I^2C register loading after reset. When asserted, the Tsi572 does not attempt to load register values from I^2C. 0 = Enable I^2C register loading 1 = Disable I^2C register loading Must remain stable for 10 P_CLK cycles after HARD_RST_b is de-asserted in order to be sampled correctly. Note: This signal does not control the slave accessibility of the interface. This signal is ignored after reset.	No termination required. Pull up to VDD_IO through a 10K resistor if I^2C loading is not required.
I2C_MA	I, CMOS, PU	I^2C Multibyte Address. When driven high, I^2C module will expect multi-byte peripheral addressing; otherwise, when driven low, single-byte peripheral address is assumed. Must remain stable for 10 P_CLK cycles after HW_RST_b is de-asserted in order to be sampled correctly. This signal is ignored after reset.	No termination required. Internal pull-up may be used for logic 1. Pull up to VDD_IO through 10K resistor if an external pull-up is desired. Pull down to VSS_IO to change the logic state.
I2C_SA[1,0]	I, CMOS, PU	I^2C Slave Address pins. The values on these two pins represent the values for the lower 2 bits of the 7-bit address of Tsi572 when acting as an I^2C slave (see I^2C Slave Configuration register). The values at these pins can be overridden by software after reset.	No termination required. Internal pull-up may be used for logic 1. Pull up to VDD_IO through 10K resistor if an external pull-up is desired. Pull down to VSS_IO to change the logic state.

Table 3: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
I2C_SEL	I, CMOS, PU	I^2C Pin Select. Together with the I2C_SA[1,0] pins, Tsi572 will determine the lower 2 bits of the 7-bit address of the EEPROM address it boots from. When asserted, the I2C_SA[1,0] values will also be used as the lower 2 bits of the EEPROM address. When de-asserted, the I2C_SA[1,0] pins will be ignored and the lower 2 bits of the EEPROM address are default to 00. The values of the lower 2 bits of the EEPROM address can be over-ridden by software after reset.	No termination required. Internal pull-up may be used for logic 1. Pull up to VDD_IO through 10K resistor if an external pull-up is desired. Pull down to VSS_IO to change the logic state.
JTAG TAP Controller			
TCK	I, LVTTL, PD	IEEE 1149.1 Test Access Port Clock input	Pull up to VDD_IO through 10K resistor if not used.
TDI	I, LVTTL, PU	IEEE 1149.1 Test Access Port Serial Data Input	Pull up to VDD_IO through a 10K resistor if the signal is not used or a if higher edge rate is required.
TDO	O, LVTTL, 2mA	IEEE 1149.1 Test Access Port Serial Data Output	No connect if JTAG is not used. Pull up to VDD_IO through a 10K resistor if used.
TMS	I, LVTTL, PU	IEEE 1149.1 Test Access Port Test Mode Select	Pull up to VDD_IO through a 10K resistor if not used.
TRST_b	I, LVTTL, PU	IEEE 1149.1 Test Access Port TAP Reset Input This input must be asserted during the assertion of HARD-RST_b. Afterwards, it may be left in either state. Combine the HARD_RST_b and TRST_b signals with an AND gate and use the output to drive the TRST_b pin.	Tie to VSS_IO through a 10K resistor if not used.

Table 3: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
BCE	I, LVTTL, PU	Boundary Scan compatibility enabled pin. This input is used to aid 1149.6 testing. This signal also enables system level diagnostic capability using features built into the SerDes. For more information on this functionality, refer to the Serial RapidIO Signal Analyzer documentation. This signal must be tied to VDD_IO during normal operation of the device, and during JTAG accesses of the device registers	This signal should have the capability to be pulled-up or pulled-low. • The default setting is to be pulled-up. • Pulling the signal low enables the signal analyzer functionality on the SerDes • A 10K resistor to VDD_IO should be used.
Power Supplies			
SP_AVDD	-	Port n and n+1: 3.3V supply for bias generator circuitry. This is required to be a low-noise supply.	Refer to ““Decoupling Requirements” on page 57”
REF_AVDD	-	Analog 1.2V for Reference Clock (S_CLK_p/n). Clock distribution network power supply.	Refer to ““Decoupling Requirements” on page 57”
Common Supply			
VDD_IO	-	Common 3.3V supply for LVTTL I/O	Refer to ““Decoupling Requirements” on page 57”
VSS	-	Common ground supply for digital logic	Refer to ““Decoupling Requirements” on page 57”
VDD	-	Common 1.2V supply for digital logic	Refer to ““Decoupling Requirements” on page 57”
SP_VDD	-	1.2V supply for CDR, Tx/Rx, and digital logic for all RapidIO ports	Refer to ““Decoupling Requirements” on page 57”

a. Signals for unused serial ports do not require termination and can be left as N/Cs.

1.3 Package Characteristics

The Tsi572's package characteristics are summarized in the following table. The following figures show the top, side, and bottom views of the Tsi572 package.

Table 4: Package Characteristics

Feature	Description
Package Type	Heat Slug Ball Grid Array (HSBGA)
Package Body Size	21 mm x 21 mm
JEDEC Specification	95-1 Section 14
Pitch	1.00 mm
Ball pad size	500 um
Soldermask opening	400 um
Moisture Sensitivity Level	3

Figure 2: Package Diagram — Top View

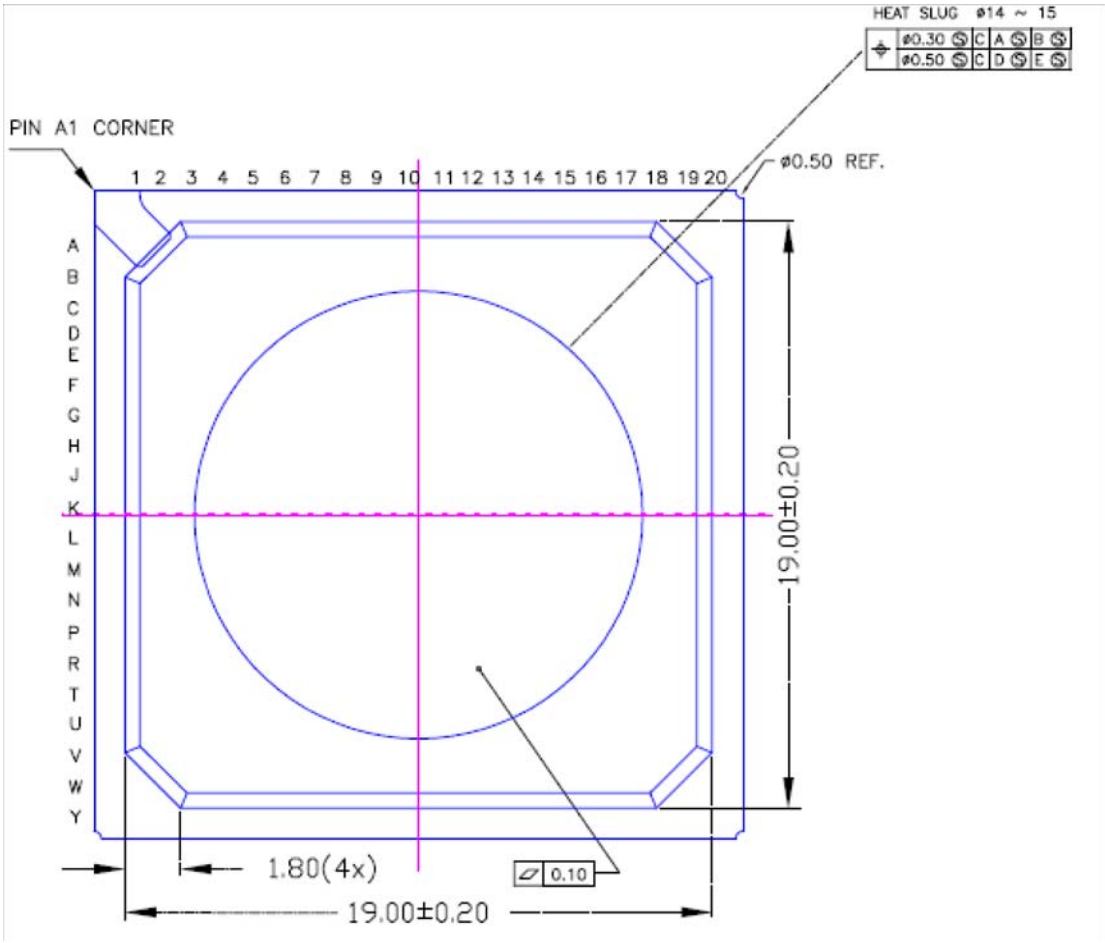


Figure 3: Package Diagram — Side View