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IDT® Tsi577
Serial RapidIO Switch

Hardware Manual

May 18, 2012

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Contents

About this Document

This section discusses general document information about the *Serial RapidIO Switch*. The following topics are described:

Scope

The *Tsi577 Hardware Manual* discusses electrical, physical, and board layout information for the Tsi577. It is intended for hardware engineers who are designing system interconnect applications with these devices.

Document Conventions

This document uses a variety of conventions to establish consistency and to help you quickly locate information of interest. These conventions are briefly discussed in the following sections.

Non-differential Signal Notation

Non-differential signals are either active-low or active-high. An active-low signal has an active state of logic 0 (or the lower voltage level), and is denoted by a lowercase "b". An active-high signal has an active state of logic 1 (or the higher voltage level), and is not denoted by a special character. The following table illustrates the non-differential signal naming convention.

State	Single-line signal	Multi-line signal
Active low	NAME_b	NAMEn[3]
Active high	NAME	NAME[3]

Differential Signal Notation

Differential signals consist of pairs of complement positive and negative signals that are measured at the same time to determine a signal's active or inactive state (they are denoted by "_p" and "_n", respectively). The following table illustrates the differential signal naming convention.

State	Single-line signal	Multi-line signal
Inactive	NAME_p = 0 NAME_n = 1	NAME_p[3] = 0 NAME_n[3] =1
Active	NAME_p = 1 NAME_n = 0	NAME_p[3] is 1 NAME_n[3] is 0

Symbols

This symbol indicates a basic design concept or information considered helpful.

This symbol indicates important configuration information or suggestions.

This symbol indicates procedures or operating levels that may result in misuse or damage to the device.

Revision History

May 18, 2012, Formal

- Updated the first paragraph in “Power Sequencing” on page 35
- Added Figure 38 (Analyzer Probe Footprint)

November 18, 2010, Formal

Added a note to Table 13

August 2009, Formal

There have been no technical changes to this document. The formatting has been updated to reflect IDT.

June 2009, Formal

There have been changes throughout the document.

September 2008, Advance

- Updated Table 8 on page 32 with new Tsi577 operating conditions

August 2008, Advance

- Updated Table 5 on page 29 with new Tsi577 thermal characteristics
- Updated Table 6 on page 29 with new simulated junction to ambient characteristics

August 2008, Advance

Although changes occurred throughout this document, the majority of changes were in “Signals and Package” on page 11.

June 2008, Advance

This was the first version of this document.

Bibliography

1	*RapidIO Interconnect Specification (Revision 1.3)*	This specification explains RapidIO's logical layer, common transport layer, and physical layer protocol and packet formats. It also describes overall inter-operability requirements for the RapidIO protocol. For more information, see www.rapidio.org.
2	Enhancements to the RapidIO AC Specification	This document contains the AC specifications for the RapidIO physical layer.
3	ANSI/TIA/EIA-644-1995, Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, March 1996.	This documents the LVDS electrical characteristics.
4	I^2C Specification	This specification defines the standard I2C bus interface, including specifications for all the enhancements. For more information, see www.semiconductors.philips.com document number: 9398 393 40011
5	High-Speed Digital System Design	Hall,Stephen H.,Garret W. Hall & James A. McCall, ©2000 John Wiley & Sons inc. ISBN 0-471-36090-2
6	*High-Speed Digital Design*	Johnson, Howard, Martin Graham ©1993 Prentice-Hall inc. ISBN 0-13-395724-1
7	*High Performance Printed Circuit Boards*	Harper, Charles A. ©1999 McGraw-Hill ISBN 0-07-026713-8
8	Transmission Line *RAPIDESIGNER*©	Application Note 905 ©1996 National Semiconductor Corp. Lit # 100905-002 & 633201-001
9	*High Speed PCB Design*	Ritchey, Lee W., James C. Blankenhorn ©1993 SMT Plus Inc., and Ritch Tech
10	Design Guidelines for Electronic Packaging *Utilizing High Speed Techniques*	The Institute for Interconnecting and Packaging Electronic Circuits ©1999 IPC Document # IPC-D-317A

11	*High Speed Signal Propagation*	Johnson, Howard, Martin Graham ©2003 Prentice-Hall inc. ISBN 0-13-084408-X
12	*High Speed Digital Design and PCB Layout*	Hanson, Robert J. ©AmeriCom Test & SMT Technology Inc.
13	*1-10 GBps Serial Interconnect Requirements*	Solving High Speed Serial Design Challenges ©2004Xilinx
14	*10GBps Serial Backplanes Using Virtex-II Pro X*	Solving High Speed Serial Design Challenges ©2004Xilinx
15	*Designing Controlled-impedance Vias*	Thomas Neu, EDN magazine, October 2 2003
16	*Computer Circuits Electrical Design, First Edition,*	Ron K. Poon Prentice-Hall, Inc., 1995

1. Signals and Package

This chapter describes the packaging (mechanical) features for the Tsi577. It includes the following information:

1.1 Signals

The following conventions are used in the signal description table:

- Signals with the suffix "_p" are the positive half of a differential pair.
- Signals with the suffix "_n" are the negative half of a differential pair.
- Signals with the suffix "_b" are active low.

Signals are classified according to the types defined in Table 1.

Table 1: Signal Types

Pin Type	Definition
I	Input
O	Output
I/O	Input/Output
OD	Open Drain
SRIO	Differential driver/receiver defined by *RapidIO Interconnect Specification (Revision 1.3)*
PU	Pulled Up internal to the Tsi577
PD	Pulled Down internal to the Tsi577
LVTTL	CMOS I/O with LVTTL thresholds
CML	Current Mode Logic - Defined by *RapidIO Interconnect Specification (Revision 1.3)*

Table 1: Signal Types (Continued)

Pin Type	Definition
Hyst	Hysteresis
Core Power	Core supply
Core Ground	Ground for core logic
I/O Power	I/O supply
N/C	No connect These signals must be left unconnected.

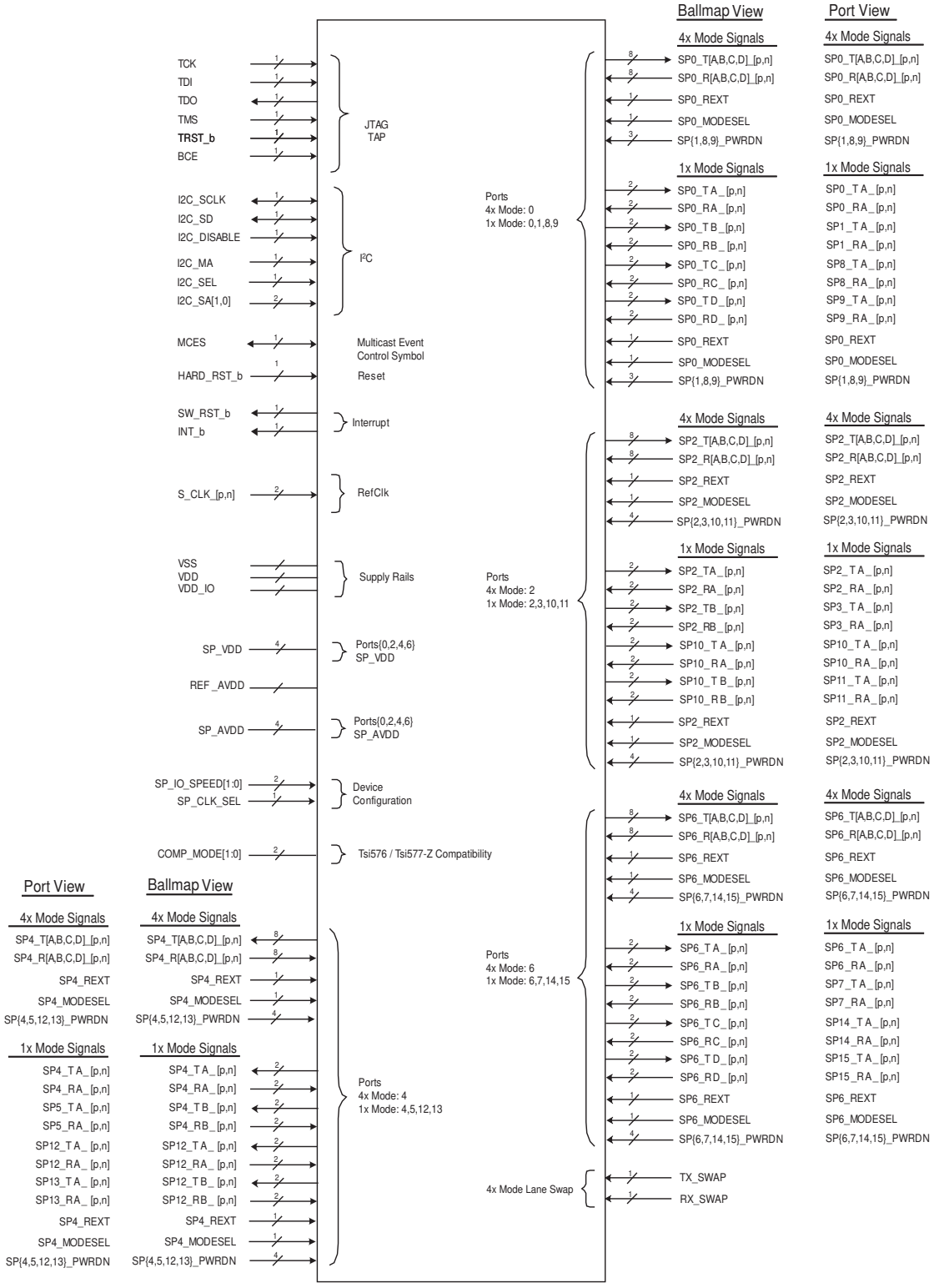
1.1.1 Endian Ordering

This document follows the bit-numbering convention adopted by *RapidIO Interconnect Specification (Revision 1.3)*, where [0:7] is used to represent an 8 bit bus with bit 0 as the most-significant bit.

1.1.2 Signal Grouping

Figure 1 shows two views of the signals: the ball map view and the port view. The ball map view shows the pins as they are named in the Tsi577 ball map. The port view shows the signals on the same balls that are configuration dependent.

Figure 1: Signal Groupings



The signals shown in Table 2 are described using the port view information (4x mode) in Figure 1. The ball map view in the figure is to show compatibility with the Tsi576 and Tsi577-Z devices.

Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
PORT n = 1x/4x Mode Serial RapidIO **PORT m = 1x Mode Serial RapidIO** **n = 0, 2, 4, 6** **m = n+1, n+8, n+9 for each value of n**			
Serial Port Transmit			
SP{n}_TA_p	O, SRIO	Port n Lane A Differential Non-inverting Transmit Data output (4x mode) Port n Differential Non-inverting Transmit Data output (1x mode)	No termination required.
SP{n}_TA_n	O, SRIO	Port n Lane A Differential Inverting Transmit Data output (4x mode) Port n Differential Inverting Transmit Data output (1x mode)	No termination required.
SP{n}_TB_p	O, SRIO	Port n Lane B Differential Non-inverting Transmit Data output (4x mode) Port m (=n+1) Differential Non-inverting Transmit Data output (1x mode)	No termination required.
SP{n}_TB_n	O, SRIO	Port n Lane B Differential Inverting Transmit Data output (4x mode) Port m (=n+1) Differential Inverting Transmit Data output (1x mode)	No termination required.
SP{n}_TC_p	O, SRIO	Port n Lane C Differential Non-inverting Transmit Data output (4x mode) Port m (=n+8) Differential Non-inverting Transmit Data output (1x mode)	No termination required.
SP{n}_TC_n	O, SRIO	Port n Lane C Differential Inverting Transmit Data output (4x mode) Port m (=n+8) Differential Inverting Transmit Data output (1x mode)	No termination required.
SP{n}_TD_p	O, SRIO	Port n Lane D Differential Non-inverting Transmit Data output (4x mode) Port m (=n+9) Differential Non-inverting Transmit Data output (1x mode)	No termination required.

Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
SP{n}_TD_n	O, SRIO	Port n Lane D Differential Inverting Transmit Data output (4x mode) Port m (=n+9) Differential Inverting Transmit Data output (1x mode)	No termination required.
Serial Port Receive			
SP{n}_RA_p	I, SRIO	Port n Lane A Differential Non-inverting Receive Data input (4x node) Port n Differential Non-inverting Receive Data input (1x mode)	DC blocking capacitor of 0.1uF in series
SP{n}_RA_n	I, SRIO	Port n Lane A Differential Inverting Receive Data input (4x mode) Port n Differential Inverting Receive Data input (1x mode)	DC blocking capacitor of 0.1uF in series
SP{n}_RB_p	I, SRIO	Port n Lane B Differential Non-inverting Receive Data input (4x mode) Port m (=n+1) Differential Non-inverting Receive Data input (1x mode)	DC blocking capacitor of 0.1uF in series
SP{n}_RB_n	I, SRIO	Port n Lane B Differential Inverting Receive Data input (4x mode) Port m (=n+1) Differential Inverting Receive Data input (1x mode)	DC blocking capacitor of 0.1uF in series
SP{n}_RC_p	I, SRIO	Port n Lane C Differential Non-inverting Receive Data input (4x mode) Port m (=n+8) Differential Non-inverting Receive Data input (1x mode)	DC blocking capacitor of 0.1uF in series
SP{n}_RC_n	I, SRIO	Port n Lane C Differential Inverting Receive Data input (4x mode) Port m (=n+8) Differential Inverting Receive Data input (1x mode)	DC blocking capacitor of 0.1uF in series
SP{n}_RD_p	I, SRIO	Port n Lane D Differential Non-inverting Receive Data input (4x mode) Port m (=n+9) Differential Non-inverting Receive Data input (1x mode)	DC blocking capacitor of 0.1uF in series
SP{n}_RD_n	I, SRIO	Port n Lane D Differential Inverting Receive Data input (4x mode) Port m (=n+9) Differential Inverting Receive Data input (1x mode)	DC blocking capacitor of 0.1uF in series

Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
Serial Port Configuration			
SP{n}_REXT	I	Used to connect a resistor to VSS to provide a reference current for the driver and equalization circuits.	Series resistor of 191Ω (1%) connected to VSS.
SPn_MODESEL (PWRUP)	I/O, LVTTL, PD	Selects the operating mode for all four serial ports within a given MAC n (n = {0,2,4,6}) 0 = MAC n operating in 4x+0x+0x+0x mode as described in section "4x + 0x + 0x + 0x Configuration" on page 77 1 = MAC n operating in 1x+1x+1x+1x mode as described in section "1x + 1x + 1x + 1x Configuration" on page 77 Note: The MAC_MODE in the "SRIO MAC x Digital Loopback and Clock Selection Register" on page 407 overrides and determine the operating mode for the corresponding ports. Output capability of this pin is only used in test mode.	Pin must be tied off according to the required configuration. Either a 10K pull up to VDD_IO or a 10K pull-down to VSS. Internal pull-down may be used for logic 0.

Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
SP{n}_PWRDN (PWRUP)	I/O, LVTTL, PU	Port n Transmit and Receive Power Down Control (where n = {2, 4, 6}) This signal controls the state of Port n inside a given MAC n. If Port n is in 4X mode, then the SPn_PWRDN controls the state of all four lanes (A/B/C/D) of SerDes Macro. If Port n is in 1X mode, related port m are controlled by SPm_PWRDN. If SPn_PWRDN is set and all three other ports in the same given MACn have their SPm_PWRDN set, then the given MACn SERDES is also powered down. When n=x, the related m ports are (x+1, x+8, x+9). 0 = Port n Powered Up 1 = Port n Powered Down Override SP{n}_PWRDN using PWDN_X4 field in the "SRIO MAC x Digital Loopback and Clock Selection Register" on page 407. Output capability of this pin is only used in test mode.	Pin must be tied off according to the required configuration. Either a 10K pull up to VDD_IO or a 10K pull-down to VSS. Internal pull-up may be used for logic 1.
SP{m}_PWRDN (PWRUP)	I/O, LVTTL, PU	Port m Transmit and Receive Power Down Control (where m= {1, 3, 5, 7,8,9,10,11,12,13,14,15}) This signal controls the state of Port m. Note that Port m is never used when 4x mode is selected for a Serial Rapid I/O MAC, and it can be powered down. 0 = Port m Powered Up 1 = Port m Powered Down If SPn is in 1X mode and SPn_PWRDN is set and all three other ports in the same given MACn have their SPm_PWRDN set, then the given MACn SERDES is also powered down. Override SP{m}_PWRDN using PWDN_X1/X4 field in the "SRIO MAC x Digital Loopback and Clock Selection Register" on page 407. Output capability of this pin is only used in test mode.	Pin must be tied off according to the required configuration. Either a 10K pull up to VDD_IO or a 10K pull-down to VSS. Internal pull-up may be used for logic 1.

Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
COMP_MODE[1:0] (PWRUP)	I, LVTTL, {PU, PD}	Tsi577 Compatibility Modes These signals are for backward compatibility with existing devices 00 = Tsi577-Z Replacement (16*1X ports) 01 = Tsi576 Replacement (2*4X + 8*1X) 10 = Tsi577 (default) 11 = Reserved For further detail refer to "Tsi577 Compatibility Modes" on page 25.	Pin must be tied off according to the required configuration. Either a 10K pull up to VDD_IO or a 10K pull-down to VSS. Internal pull-up/pull-down may be used for default setting of 2'b10
Serial Port Speed Select			
SP_IO_SPEED[1] (PWRUP)	I/O, LVTTL, PU	Serial Port Transmit and Receive operating frequency select. SP_IO_SPEED[1:0], these pin select the power-up serial port frequency for *all* ports. 00 = 1.25Gbit/s 01 = 2.5Gbit/s 10 = 3.125Gbit/s (default) 11 = Illegal Note; The SP_IO_SPEED[1:0] setting is equal to theIO_SPEED field in the "SRIO MAC x Digital Loopback and Clock Selection Register" on page 407. Output capability of this pin is only used in test mode.	Pin must be tied off according to the required configuration. Either a 10K pull-up to VDD_IO or a 10K pull-down to VSS. Internal pull-up may be used for logic 1.
SP_IO_SPEED[0] (PWRUP)	I/O, LVTTL, PD	See SP_IO_SPEED[1]	Pin must be tied off according to the required configuration. Either a 10K pull-up to VDD_IO or a 10K pull-down to VSS. Internal pull-down may be used for logic 0.

Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
SP_CLK_SEL (PWRUP)	I/O, LVTTL, PD	Reference clock speed 1 = 125-MHz Reference clock 0 = 156.25-MHz Reference clock This signal configures the MPLL settings for the RapidIO SerDes. Output capability of this pin is only used in test mode.	Pin must be tied off according to the required configuration. Either a 10K pull-up to VDD_IO or a 10K pull-down to VSS. Internal pull-down may be used for logic 0.
Serial Port Lane Ordering Select			
SP_RX_SWAP (PWRUP)	I, LVTTL, PD	Configures the order of 4X receive/transmit lanes on serial ports. 0 = A, B, C, D 1 = D, C, B, A Override SP_RX(TX)_SWAP usingSWAP_RX(TX) field in the "SRIO MAC x Digital Loopback and Clock Selection Register" on page 407. This signal is ignored in 1X mode. Note: Ports that require the use of lane swapping for ease of routing will only function as 4x mode ports. The re-configuration of a swapped port to dual 1x mode operation results in the inability to connect to a 1x mode link partner.	No termination required. Internal pull-down can be used for logic 0. Pull up to VDD_IO through 10K if external pull-up is desired. Pull down to VSS through a 10K resistor if an external pull-down is desired.
SP_TX_SWAP (PWRUP)	I, LVTTL, PD	See SP_RX_SWAP	No termination required. Internal pull-down can be used for logic 0. Pull up to VDD_IO through 10K if external pull-up is desired. Pull down to VSS through 10K resistor if an external pull-down is desired.

Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
Clock and Reset			
S_CLK_p	I, CML	Differential non-inverting reference clock. The clock is used for following purposes: SERDES reference clock, serial port system clock, ISF clock and test clock. The clock frequency is defined in the Minimum Clock Frequency Requirements section. The maximum frequency of this input clock is 156.25 MHz.	AC coupling capacitor of 0.1uF required.
S_CLK_n	I, CML		
HARD_RST_b	I LVTTL, Hyst, PU	Schmidt-triggered hard reset. Asynchronous active low reset for the entire device. The Tsi577 does not contain a voltage detector to generate internal reset.	Connect to a power-up reset source. See “Reset Requirements” on page 66 for more detail.
Interrupts			
INT_b	O, OD, LVTTL, 2mA	Interrupt signal (open drain output)	External pull-up required. Pull up to VDD_IO through a 10K resistor.
SW_RST_b	O, OD, LVTTL, 2mA	Software reset (open drain output): This signal is asserted when a RapidIO port receives a valid reset request on a RapidIO link. If self-reset is not selected, this pin remains asserted until the reset request is cleared from the status registers. If self-reset is selected, this pin remains asserted until the self reset is complete. If the Tsi577 is reset from the HARD_RST_b pin, this pin is de-asserted and remains de-asserted after HARD_RST_b is released. For more information, refer to “Resets” in the Tsi577 User’s Manual.	External pull-up required. Pull up to VDD_IO through a 10K resistor.

Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
Miscellaneous			
Multicast			
MCES	I/O, LVTTL, PD	Multicast Event Symbol pin. As an input, an edge (rising or falling) will trigger a Multicast Event Control Symbol to be sent to all enabled ports. As an output, this pin will toggle its value every time an Multicast Event Control Symbol is received by any port which is enabled for Multicast event control symbols. Refer to section "Multicast-Event Control Symbols" on page 58 for further details.	No termination required. This pin must not be driven by an external source until all power supply rails are stable.
I^2C			
I2C_SCLK	I/O, OD, LVTTL, PU 8mA	I^2C clock, up to 100 kHz. This clock signal must be connected to the clock of the serial EEPROM on the I^2C bus.	No termination required. Internal pull-up may be used for logic 1. Pull up to VDD_IO through a minimum 470 ohms resistor if higher edge rate is required.
I2C_SD	I/O, OD, LVTTL, PU 8mA	I^2C input and output data bus (bidirectional open drain)	No termination required. Internal pull-up may be used for logic 1. Pull up to VDD_IO through a minimum 470 ohms resistor if higher edge rate required.
I2C_DISABLE (PWRUP)	I, LVTTL, PD	Disable I^2C register loading after reset. When asserted, the Tsi577 will not attempt to load register values from I^2C.	No termination required.Pull up to VDD_IO through a 10K resistor if I^2C loading is not required.

Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
I2C_MA (PWRUP)	I, LVTTL, PU	I^2C Multibyte Address When driven high, I^2C module expects multi-byte peripheral addressing; otherwise, when driven low, single-byte peripheral address is assumed. The value on this pin, sets the PA_SIZE field in "I2C Master Configuration Register" on page 476 and PSIZE field in "I2C Boot Control Register" on page 496.	No termination required. Internal pull-up may be used for logic 1. Pull up to VDD_IO through 10K resistor if an external pull-up is desired. Pull down to VSS to change the logic state.
I2C_SA[1:0] (PWRUP)	I, LVTTL, {PU, PU}	I^2C Slave Address pins The values on these two pins represent the values for the lower 2 bits of the 7-bit address of Tsi577 when acting as an I^2C slave (field SLV_ADDR in "I2C Slave Configuration Register" on page 493). These pins with I2C_SEL is also used to update the lower 2 bits of the 7-bit address of the EEPROM address it boots from (field BOOT_ADDR in "I2C Boot Control Register" on page 496) and to access an external slave (field DEV_ADDR in "I2C Master Configuration Register" on page 476).	No termination required. Internal pull-up may be used for logic 1. Pull up to VDD_IO through 10K resistor if an external pull-up is desired. Pull down to VSS to change the logic state.
I2C_SEL (PWRUP)	I, LVTTL, PU	I^2C Pin Select Together with the I2C_SA[1:0] pins, Tsi577 determines the lower 2 bits of the 7-bit address of the EEPROM address it boots from. When asserted, the I2C_SA[1:0] values are also used as the lower 2 bits of the EEPROM address. When de-asserted, the I2C_SA[1:0] pins are ignored and the lower 2 bits of the EEPROM address default to 00.	No termination required. Internal pull-up may be used for logic 1. Pull up to VDD_IO through 10K resistor if an external pull-up is desired. Pull down to VSS to change the logic state.
JTAG TAP Controller			
TCK	I, LVTTL, PD	IEEE 1149.1 Test Access Port Clock input	Pull up to VDD_IO through 10K resistor if not used.

Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
TDI	I, LVTTL, PU	IEEE 1149.1 Test Access Port Serial Data Input	Pull up to VDD_IO through a 10K resistor if the signal is not used or a if higher edge rate is required.
TDO	O, LVTTL, 8mA	IEEE 1149.1 Test Access Port Serial Data Output	No connect if JTAG is not used. Pull up to VDD_IO through a 10K resistor if used.
TMS	I, LVTTL, PU	IEEE 1149.1 Test Access Port Test Mode Select	Pull up to VDD_IO through a 10K resistor if not used.
TRST_b	I, LVTTL, PU	IEEE 1149.1 Test Access Port TAP Reset Input This input must be asserted during the assertion of HARD-RST_b. Afterwards, it may be left in either state. Combine the HARD_RST_b and TRST_b signals with an AND gate and use the output to drive the TRST_b pin.	Tie to VSS through a 10K resistor if not used.
BCE	I, LVTTL, PU	Boundary Scan compatibility enabled pin. This input is used to aid 1149.6 testing. This signal also enables system level diagnostic capability using features built into the SerDes. This signal must be tied to VDD_IO during normal operation of the device, and during JTAG accesses of the device registers	This signal should have the capability to be pulled-up or pulled-low. • The default setting is to be pulled-up. • Pulling the signal low enables the signal analyzer functionality on the SerDes • A 10K resistor to VDD_IO should be used.
Power Supplies			
SP_AVDD	-	3.3V supply for bias generator circuitry. This is required to be a low-noise supply.	Refer to “Decoupling Requirements” on page 59.
REF_AVDD	-	Analog 1.2V for Reference Clock (S_CLK_P/N). Clock distribution network power supply.	Refer to “Decoupling Requirements” on page 59.

Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
Common Supply			
VDD_IO	-	Common 3.3V supply for LVTTL I/O	Refer to "Decoupling Requirements" on page 59.
VSS	-	Common ground supply for digital logic	Refer to "Decoupling Requirements" on page 59.
VDD	-	Common 1.2V supply for digital logic	Refer to "Decoupling Requirements" on page 59.
SP_VDD	-	1.2V supply for CDR, Tx/Rx, and digital logic for all RapidIO ports	Refer to "Decoupling Requirements" on page 59.

a. Signals for unused serial ports do not require termination and can be left as N/Cs.

1.1.3 Tsi577 Compatibility Modes

Table 3 lists the different COMP_MODE[1:0] pin configurations which allow backward pin and software compatibility with the Tsi576 and Tsi577-Z devices.

- When Tsi577 is placed in a Tsi577-Z socket, COMP_MODE is automatically set to 00. The device powers up with all ports (0..15) in x1.
- When Tsi577 is placed in a Tsi576 socket, COMP_MODE is automatically set to 01
  - The Tsi577 powers up with ports 0 and 6 in 4x mode and ports 2 -> 5, 10 -> 13 in 1x mode (2*x4 + 8*x1). In this case, the maximum 1x mode ports is 12.
- The default mode for Tsi577 is 10.
  - Ports 0, 2, 4, 6 can be 4x mode or all 16 ports (0..15) can be 1x mode.

Table 3: Tsi577 Compatibility Modes

Device ID	COMP_MODE[1:0]	Max Number of Ports		Port Total	Description
0x577	00	4x mode	0	16	Tsi577-Z Replacement
		1x mode	16		
0x577	01	4x mode	2	16	Tsi576 Replacement
		1x mode	12		
0x577	10	4x mode	4	16	Tsi577 Mode (default)
		1x mode	16		
0x577	11	Reserved			

1.2 Pinlist and Ballmap

The pinlist and ballmap information for the Tsi577 are available by visiting www.IDT.com and registering. For more information, see the following documents:

- *Tsi577 Pinlist*
- *Tsi577 Ballmap*