



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



---

**IDT<sup>®</sup> Tsi578**  
**Serial RapidIO Switch**

**User Manual**

June 6, 2016

---

---

#### GENERAL DISCLAIMER

Integrated Device Technology, Inc. ("IDT") reserves the right to make changes to its products or specifications at any time, without notice, in order to improve design or performance. IDT does not assume responsibility for use of any circuitry described herein other than the circuitry embodied in an IDT product. Disclosure of the information herein does not convey a license or any other right, by implication or otherwise, in any patent, trademark, or other intellectual property right of IDT. IDT products may contain errata which can affect product performance to a minor or immaterial degree. Current characterized errata will be made available upon request. Items identified herein as "reserved" or "undefined" are reserved for future definition. IDT does not assume responsibility for conflicts or incompatibilities arising from the future definition of such items. IDT products have not been designed, tested, or manufactured for use in, and thus are not warranted for, applications where the failure, malfunction, or any inaccuracy in the application carries a risk of death, serious bodily injury, or damage to tangible property. Code examples provided herein by IDT are for illustrative purposes only and should not be relied upon for developing applications. Any use of such code examples shall be at the user's sole risk.

Copyright © 2016 Integrated Device Technology, Inc.  
All Rights Reserved.

The IDT logo is registered to Integrated Device Technology, Inc. IDT and CPS are trademarks of Integrated Device Technology, Inc.

---

# Contents

<b>About this Document</b> .....	<b>17</b>
Scope .....	17
Document Conventions .....	17
Revision History .....	18
<b>1. Functional Overview</b> .....	<b>21</b>
1.1 Overview .....	21
1.1.1 Features .....	24
1.2 Serial RapidIO Interface .....	26
1.2.1 Features .....	26
1.2.2 Transaction Flow Overview .....	26
1.2.3 Maintenance Requests .....	27
1.2.4 Control Symbols .....	27
1.3 Multicast Engine .....	27
1.3.1 Multicast Operation .....	27
1.3.2 Features .....	28
1.4 Serial RapidIO Electrical Interface .....	28
1.5 Internal Switching Fabric (ISF) .....	30
1.6 Internal Register Bus (AHB) .....	30
1.7 I <sup>2</sup> C Interface .....	30
1.8 JTAG Interface .....	32
<b>2. Serial RapidIO Interface</b> .....	<b>35</b>
2.1 Overview .....	35
2.1.1 Features .....	35
2.1.2 Transaction Flow Overview .....	36
2.1.3 Maintenance Requests .....	36
2.1.4 Control Symbols .....	36
2.2 Transaction Flow .....	37
2.3 Lookup Tables .....	37
2.3.1 Filling the Lookup Tables .....	38
2.3.2 LUT Modes .....	40
2.3.3 Flat Mode .....	40
2.3.4 Hierarchical Mode .....	45
2.3.5 Mixed Mode of Operation .....	49
2.3.6 Lookup Table Parity .....	49
2.3.7 Lookup Table Error Summary .....	50
2.3.8 Lookup Table Entry States .....	51
2.4 Maintenance Packets .....	53
2.5 Multicast Event Control Symbols .....	55
2.5.1 MCS Reception .....	55
2.5.2 Generating an MCS .....	56
2.5.3 Restrictions .....	56
2.6 Reset Control Symbol Processing .....	57

2.7	Data Integrity Checking . . . . .	57
2.7.1	Packet Data Integrity Checking . . . . .	57
2.7.2	Control Symbol Data Integrity Checking . . . . .	57
2.8	Error Management . . . . .	57
2.8.1	Software Assisted Error Recovery . . . . .	58
2.9	Hot Insertion and Hot Extraction . . . . .	59
2.9.1	Hot Insertion . . . . .	60
2.9.2	Hot Extraction . . . . .	61
2.9.3	Hot Extraction System Notification . . . . .	62
2.10	Loss of Lane Synchronization . . . . .	62
2.10.1	Dead Link Timer . . . . .	64
2.10.2	Lane Sync Timer . . . . .	64
<b>3.</b>	<b>Serial RapidIO Electrical Interface . . . . .</b>	<b>65</b>
3.1	Overview . . . . .	65
3.2	Port Numbering . . . . .	67
3.2.1	Port Configuration . . . . .	67
3.3	Port Aggregation: 1x and 4x Modes . . . . .	68
3.3.1	1x + 1x Configuration . . . . .	69
3.3.2	4x Configuration . . . . .	69
3.4	Clocking . . . . .	70
3.4.1	Changing the Clock Speed . . . . .	71
3.4.2	Changing the Clock Speed Through I <sup>2</sup> C . . . . .	71
3.5	Port Power Down . . . . .	72
3.5.1	Default Configurations on Power Down . . . . .	72
3.5.2	Special Conditions for Port 0 Power Down . . . . .	73
3.5.3	Power-Down Options . . . . .	73
3.5.4	Configuration and Operation Through Power-down . . . . .	73
3.6	Port Lanes . . . . .	74
3.6.1	Lane Synchronization and Alignment . . . . .	75
3.6.2	Lane Swapping . . . . .	75
3.7	Programmable Transmit and Receive Equalization . . . . .	77
3.7.1	Transmit Drive Level and Equalization . . . . .	77
3.7.2	Receive Equalization . . . . .	78
3.8	Port Loopback Testing . . . . .	79
3.8.1	Digital Equipment Loopback . . . . .	80
3.8.2	Logical Line Loopback . . . . .	80
3.9	Bit Error Rate Testing (BERT) . . . . .	80
3.9.1	BERT Pattern Generator . . . . .	80
3.9.2	BERT Pattern Matcher and Error Counter . . . . .	82
3.9.3	Fixed Pattern-based BERT . . . . .	82
3.9.4	Using PRBS Scripts for the Transmitters and Receivers . . . . .	83
<b>4.</b>	<b>Internal Switching Fabric . . . . .</b>	<b>85</b>
4.1	Overview . . . . .	85
4.2	Functional Behavior . . . . .	86
4.2.1	Transfer Modes . . . . .	87

4.3	Arbitration for Egress Port . . . . .	88
4.3.1	Strict Priority Arbitration . . . . .	88
4.3.2	Weighted Round Robin (WRR) Arbitration. . . . .	89
4.4	Packet Queuing . . . . .	91
4.4.1	Output Queuing on the Egress Port . . . . .	91
4.4.2	Input Queue for the ISF Port . . . . .	94
4.4.3	Input Arbitration. . . . .	95
4.4.4	Input Queuing Model for the Multicast Work Queue . . . . .	99
4.4.5	Input Queuing Model for the Broadcast Buffer . . . . .	100
4.4.6	Output Queuing Model for Multicast. . . . .	100
4.4.7	ISF Bandwidth . . . . .	100
<b>5.</b>	<b>Multicast . . . . .</b>	<b>103</b>
5.1	Overview . . . . .	103
5.1.1	Multicast Operation . . . . .	103
5.1.2	Features . . . . .	103
5.1.3	Multicast Operation with Multiple Tsi57x Switches . . . . .	104
5.1.4	Multicast Terminology . . . . .	105
5.1.5	Multicast Behavior Overview . . . . .	106
5.1.6	Multicast Work Queue . . . . .	107
5.1.7	Broadcast Buffers. . . . .	107
5.2	Multicast Group Tables . . . . .	110
5.2.1	Configuring Basic Associations. . . . .	112
5.2.2	Configuring Multicast Masks. . . . .	113
5.2.3	Configuring Multicast Masks Using the IDT Specific Registers. . . . .	116
5.3	Arbitration for Multicast Engine Ingress Port . . . . .	117
5.4	Error Management of Multicast Packets . . . . .	118
5.4.1	Packet TEA . . . . .	118
5.4.2	Multicast Packet Stomping. . . . .	118
5.4.3	Multicast Maximum Latency Timer. . . . .	119
5.4.4	Silent Discard of Packets . . . . .	120
5.4.5	Port-writes and Multicast. . . . .	120
5.5	Port Reset . . . . .	120
<b>6.</b>	<b>Event Notification . . . . .</b>	<b>121</b>
6.1	Overview . . . . .	121
6.2	Event Summary . . . . .	122
6.3	Error Rate Thresholds . . . . .	126
6.3.1	Maintaining Packet Flow . . . . .	127
6.4	Error Stopped State Recovery . . . . .	128
6.4.1	Error Stopped States. . . . .	128
6.4.2	Link Error Clearing and Recovery. . . . .	129
6.5	Event Capture. . . . .	131
6.6	Port-write Notifications . . . . .	133
6.6.1	Destination ID . . . . .	134
6.6.2	Payload. . . . .	134
6.6.3	Servicing Port-writes . . . . .	135

6.6.4	Port-writes and Hot Insertion/Hot Extraction Notification . . . . .	136
6.6.5	Port-writes and Multicast . . . . .	136
6.7	Interrupt Notifications . . . . .	136
6.7.1	INT_b Signal . . . . .	138
6.7.2	Global Interrupt Status Register and Interrupt Handling . . . . .	138
6.7.3	Interrupt Notification and Port-writes . . . . .	140
6.7.4	Reset Control Symbol and Interrupt Handling . . . . .	140
<b>7.</b>	<b>I<sup>2</sup>C Interface . . . . .</b>	<b>141</b>
7.1	Overview . . . . .	141
7.2	Protocol Overview . . . . .	143
7.3	Block Diagram . . . . .	144
7.4	Tsi578 as I <sup>2</sup> C Master . . . . .	147
7.4.1	Example EEPROM Read and Write . . . . .	149
7.4.2	Master Clock Generation . . . . .	149
7.4.3	Master Bus Arbitration . . . . .	150
7.4.4	Master External Device Addressing . . . . .	150
7.4.5	Master Peripheral Addressing . . . . .	150
7.4.6	Master Data Transactions . . . . .	151
7.5	Tsi578 as I <sup>2</sup> C Slave . . . . .	151
7.5.1	Slave Clock Stretching . . . . .	153
7.5.2	Slave Device Addressing . . . . .	154
7.5.3	Slave Peripheral Addressing . . . . .	154
7.5.4	External I <sup>2</sup> C Register Map . . . . .	155
7.5.5	Slave Write Data Transactions . . . . .	156
7.5.6	Slave Read Data Transactions . . . . .	157
7.5.7	Slave Internal Register Accesses . . . . .	157
7.5.8	Slave Access Examples . . . . .	158
7.5.9	Resetting the I <sup>2</sup> C Slave Interface . . . . .	161
7.6	Mailboxes . . . . .	161
7.6.1	Incoming Mailbox . . . . .	163
7.6.2	Outgoing Mailbox . . . . .	163
7.7	SMBus Support . . . . .	163
7.7.1	Unsupported SMBus Features . . . . .	164
7.7.2	SMBus Protocol Support . . . . .	164
7.7.3	SMBus Alert Response Protocol Support . . . . .	166
7.8	Boot Load Sequence . . . . .	166
7.8.1	Idle Detect . . . . .	168
7.8.2	EEPROM Reset Sequence . . . . .	168
7.8.3	Wait for Bus Idle . . . . .	168
7.8.4	EEPROM Device Detection . . . . .	169
7.8.5	Loading Register Data from EEPROM . . . . .	169
7.8.6	Chaining . . . . .	170
7.8.7	EEPROM Data Format . . . . .	170
7.8.8	I <sup>2</sup> C Boot Time . . . . .	172
7.8.9	Accelerating Boot Load . . . . .	173
7.9	Error Handling . . . . .	174

7.10	Interrupt Handling .....	176
7.11	Events versus Interrupts .....	177
7.12	Timeouts .....	179
7.13	Bus Timing .....	183
7.13.1	Start/Restart Condition Setup and Hold .....	185
7.13.2	Stop Condition Setup .....	185
7.13.3	I2C_SD Setup and Hold .....	185
7.13.4	I2C_SCLK Nominal and Minimum Periods .....	186
7.13.5	Idle Detect Period .....	186
<b>8.</b>	<b>Performance .....</b>	<b>187</b>
8.1	Overview .....	187
8.1.1	Throughput .....	187
8.1.2	Latency .....	187
8.2	Performance Monitoring .....	188
8.2.1	Traffic Efficiency .....	190
8.2.2	Throughput .....	190
8.2.3	Bottleneck Detection .....	191
8.2.4	Congestion Detection .....	191
8.2.5	Resetting Performance Registers .....	191
8.3	Configuring the Tsi578 for Performance Measurements .....	192
8.3.1	Clock Speeds .....	192
8.3.2	Tsi578 ISF Arbitration Settings .....	192
8.3.3	Tsi578 RapidIO Transmission Scheduler Settings .....	193
8.3.4	Tsi578 RapidIO Buffer Watermark Selection Settings .....	193
8.4	Port-to-Port Performance Characteristics .....	193
8.4.1	Port-to-Port Packet Latency Performance .....	193
8.4.2	Packet Throughput Performance .....	194
8.4.3	Multicast Performance .....	195
8.5	Congestion Detection and Management .....	196
8.5.1	Congestion Registers .....	198
<b>9.</b>	<b>JTAG Interface .....</b>	<b>201</b>
9.1	Overview .....	201
9.2	JTAG Device Identification Number .....	202
9.3	JTAG Register Access Details .....	202
9.3.1	Format .....	202
9.3.2	Write Access to Registers from the JTAG Interface .....	203
9.3.3	Read Access to Registers from the JTAG Interface .....	203
<b>10.</b>	<b>Clocks, Resets and Power-up Options .....</b>	<b>205</b>
10.1	Clocks .....	205
10.1.1	Clocking Architecture .....	206
10.1.2	SerDes Clocks .....	207
10.1.3	Reference clocks .....	207
10.1.4	Clock Domains .....	208
10.1.5	Clock Gating .....	208



10.2	Resets .....	209
10.2.1	Device Reset .....	209
10.2.2	Per-Port Reset .....	211
10.2.3	Generating a RapidIO Reset Request to a Peer Device .....	211
10.2.4	JTAG Reset .....	211
10.3	Power-up Options .....	212
10.3.1	Power-up Option Signals .....	212
10.3.2	Default Port Speed .....	214
10.3.3	Port Power-up and Power-down .....	214
10.3.4	Port Width Override .....	214
<b>11.</b>	<b>Signals .....</b>	<b>215</b>
11.1	Overview .....	215
11.2	Endian Ordering .....	216
11.3	Port Numbering .....	216
11.4	Signal Groupings .....	218
11.5	Pinlist and Ballmap .....	227
<b>12.</b>	<b>Serial RapidIO Registers .....</b>	<b>229</b>
12.1	Overview .....	229
12.1.1	Reserved Register Addresses and Fields .....	230
12.2	Port Numbering .....	231
12.3	Conventions .....	231
12.4	Register Map .....	233
12.5	RapidIO Logical Layer and Transport Layer Registers .....	245
12.5.1	RapidIO Device Identity CAR .....	246
12.5.2	RapidIO Device Information CAR .....	247
12.5.3	RapidIO Assembly Identity CAR .....	248
12.5.4	RapidIO Assembly Information CAR .....	249
12.5.5	RapidIO Processing Element Features CAR .....	250
12.5.6	RapidIO Switch Port Information CAR .....	252
12.5.7	RapidIO Source Operation CAR .....	253
12.5.8	RapidIO Switch Multicast Support CAR .....	255
12.5.9	RapidIO Route LUT Size CAR .....	256
12.5.10	RapidIO Switch Multicast Information CAR .....	257
12.5.11	RapidIO Host Base Device ID Lock CSR .....	258
12.5.12	RapidIO Component Tag CSR .....	259
12.5.13	RapidIO Route Configuration DestID CSR .....	260
12.5.14	RapidIO Route Configuration Output Port CSR .....	261
12.5.15	RapidIO Route LUT Attributes (Default Port) CSR .....	262
12.5.16	RapidIO Multicast Mask Configuration Register .....	263
12.5.17	RapidIO Multicast DestID Configuration Register .....	265
12.5.18	RapidIO Multicast DestID Association Register .....	266
12.6	RapidIO Physical Layer Registers .....	268
12.6.1	RapidIO 1x or 4x Switch Port Maintenance Block Header .....	270
12.6.2	RapidIO Switch Port Link Timeout Control CSR .....	271

---

12.6.3	RapidIO Switch Port General Control CSR . . . . .	272
12.6.4	RapidIO Serial Port x Link Maintenance Request CSR . . . . .	273
12.6.5	RapidIO Serial Port x Link Maintenance Response CSR . . . . .	275
12.6.6	RapidIO Serial Port x Local ackID Status CSR . . . . .	276
12.6.7	RapidIO Port x Error and Status CSR . . . . .	278
12.6.8	RapidIO Serial Port x Control CSR . . . . .	281
12.7	RapidIO Error Management Extension Registers . . . . .	285
12.7.1	Port Behavior When Error Rate Failed Threshold is Reached . . . . .	286
12.7.2	RapidIO Error Reporting Block Header . . . . .	287
12.7.3	RapidIO Logical and Transport Layer Error Detect CSR . . . . .	288
12.7.4	RapidIO Logical and Transport Layer Error Enable CSR . . . . .	289
12.7.5	RapidIO Logical and Transport Layer Address Capture CSR . . . . .	290
12.7.6	RapidIO Logical and Transport Layer Device ID Capture CSR . . . . .	291
12.7.7	RapidIO Logical and Transport Layer Control Capture CSR . . . . .	292
12.7.8	RapidIO Port-Write Target Device ID CSR . . . . .	293
12.7.9	RapidIO Port x Error Detect CSR . . . . .	294
12.7.10	RapidIO Port x Error Rate Enable CSR . . . . .	297
12.7.11	RapidIO Port x Error Capture Attributes CSR and Debug 0 . . . . .	299
12.7.12	RapidIO Port x Packet and Control Symbol Error Capture CSR 0 and Debug 1 . . . . .	301
12.7.13	RapidIO Port x Packet Error Capture CSR 1 and Debug 2 . . . . .	302
12.7.14	RapidIO Port x Packet Error Capture CSR 2 and Debug 3 . . . . .	302
12.7.15	RapidIO Port x Packet Error Capture CSR 3 and Debug 4 . . . . .	303
12.7.16	RapidIO Port x Error Rate CSR . . . . .	304
12.7.17	RapidIO Port x Error Rate Threshold CSR . . . . .	306
12.8	IDT-Specific RapidIO Registers . . . . .	307
12.8.1	RapidIO Port x Discovery Timer . . . . .	309
12.8.2	RapidIO Port x Mode CSR . . . . .	310
12.8.3	RapidIO Port x Multicast-Event Control Symbol and Reset Control Symbol Interrupt CSR . . . . .	312
12.8.4	RapidIO Port x RapidIO Watermarks . . . . .	313
12.8.5	RapidIO Port x Route Config DestID CSR . . . . .	314
12.8.6	RapidIO Port x Route Config Output Port CSR . . . . .	315
12.8.7	RapidIO Port x Local Routing LUT Base CSR . . . . .	316
12.8.8	RapidIO Multicast Write ID x Register . . . . .	317
12.8.9	RapidIO Multicast Write Mask x Register . . . . .	318
12.8.10	RapidIO Port x Control Independent Register . . . . .	319
12.8.11	RapidIO Port x Send Multicast-Event Control Symbol Register . . . . .	322
12.8.12	RapidIO Port x LUT Parity Error Info CSR . . . . .	323
12.8.13	RapidIO Port x Control Symbol Transmit . . . . .	325
12.8.14	RapidIO Port x Interrupt Status Register . . . . .	326
12.8.15	RapidIO Port x Interrupt Generate Register . . . . .	329
12.9	IDT-Specific Performance Registers . . . . .	331
12.9.1	RapidIO Port x Performance Statistics Counter 0 and 1 Control Register . . . . .	332
12.9.2	RapidIO Port x Performance Statistics Counter 2 and 3 Control Register . . . . .	336
12.9.3	RapidIO Port x Performance Statistics Counter 4 and 5 Control Register . . . . .	340
12.9.4	RapidIO Port x Performance Statistics Counter 0 Register . . . . .	344

12.9.5	RapidIO Port x Performance Statistics Counter 1 Register . . . . .	345
12.9.6	RapidIO Port x Performance Statistics Counter 2 Register . . . . .	346
12.9.7	RapidIO Port x Performance Statistics Counter 3 Register . . . . .	347
12.9.8	RapidIO Port x Performance Statistics Counter 4 Register . . . . .	348
12.9.9	RapidIO Port x Performance Statistics Counter 5 Register . . . . .	349
12.9.10	RapidIO Port x Transmitter Output Queue Depth Threshold Register . . . . .	350
12.9.11	RapidIO Port x Transmitter Output Queue Congestion Status Register . . . . .	352
12.9.12	RapidIO Port x Transmitter Output Queue Congestion Period Register . . . . .	354
12.9.13	RapidIO Port x Receiver Input Queue Depth Threshold Register . . . . .	355
12.9.14	RapidIO Port x Receiver Input Queue Congestion Status Register . . . . .	357
12.9.15	RapidIO Port x Receiver Input Queue Congestion Period Register . . . . .	359
12.9.16	RapidIO Port x Reordering Counter Register . . . . .	360
12.10	Serial Port Electrical Layer Registers . . . . .	361
12.10.1	BYPASS_INIT Functionality . . . . .	362
12.10.2	SRIO MAC x SerDes Configuration Channel 0 . . . . .	363
12.10.3	SRIO MAC x SerDes Configuration Channel 1 . . . . .	366
12.10.4	SRIO MAC x SerDes Configuration Channel 2 . . . . .	368
12.10.5	SRIO MAC x SerDes Configuration Channel 3 . . . . .	370
12.10.6	SRIO MAC x SerDes Configuration Global . . . . .	372
12.10.7	SRIO MAC x SerDes Configuration GlobalB . . . . .	376
12.10.8	SRIO MAC x Digital Loopback and Clock Selection Register . . . . .	377
12.11	Internal Switching Fabric (ISF) Registers . . . . .	380
12.11.1	Fabric Control Register . . . . .	380
12.11.2	Fabric Interrupt Status Register . . . . .	382
12.11.3	RapidIO Broadcast Buffer Maximum Latency Expired Error Register . . . . .	384
12.11.4	RapidIO Broadcast Buffer Maximum Latency Expired Override . . . . .	386
12.12	Utility Unit Registers . . . . .	388
12.12.1	Global Interrupt Status Register . . . . .	388
12.12.2	Global Interrupt Enable Register . . . . .	390
12.12.3	RapidIO Port-Write Timeout Control Register . . . . .	392
12.12.4	RapidIO Port Write Outstanding Request Register . . . . .	393
12.12.5	MCES Pin Control Register . . . . .	394
12.13	Multicast Registers . . . . .	395
12.13.1	RapidIO Multicast Register Version CSR . . . . .	395
12.13.2	RapidIO Multicast Maximum Latency Counter CSR . . . . .	396
12.13.3	RapidIO Port x ISF Watermarks . . . . .	397
12.13.4	Port x Prefer Unicast and Multicast Packet Prio 0 Register . . . . .	398
12.13.5	Port x Prefer Unicast and Multicast Packet Prio 1 Register . . . . .	399
12.13.6	Port x Prefer Unicast and Multicast Packet Prio 2 Register . . . . .	400
12.13.7	Port x Prefer Unicast and Multicast Packet Prio 3 Register . . . . .	401
12.14	SerDes Per Lane Register . . . . .	402
12.14.1	SerDes Lane 0 Pattern Generator Control Register . . . . .	403
12.14.2	SerDes Lane 1 Pattern Generator Control Register . . . . .	404
12.14.3	SerDes Lane 2 Pattern Generator Control Register . . . . .	405
12.14.4	SerDes Lane 3 Pattern Generator Control Register . . . . .	406

12.14.5	SerDes Lane 0 Pattern Matcher Control Register	407
12.14.6	SerDes Lane 1 Pattern Matcher Control Register	408
12.14.7	SerDes Lane 2 Pattern Matcher Control Register	409
12.14.8	SerDes Lane 3 Pattern Matcher Control Register	410
12.14.9	SerDes Lane 0 Frequency and Phase Value Register	411
12.14.10	SerDes Lane 1 Frequency and Phase Value Register	412
12.14.11	SerDes Lane 2 Frequency and Phase Value Register	413
12.14.12	SerDes Lane 3 Frequency and Phase Value Register	414
<b>13.</b>	<b>I2C Registers</b>	<b>415</b>
13.1	Register Map	415
13.2	Register Descriptions	418
13.2.1	I <sup>2</sup> C Device ID Register	418
13.2.2	I <sup>2</sup> C Reset Register	419
13.2.3	I <sup>2</sup> C Master Configuration Register	420
13.2.4	I <sup>2</sup> C Master Control Register	422
13.2.5	I <sup>2</sup> C Master Receive Data Register	425
13.2.6	I <sup>2</sup> C Master Transmit Data Register	426
13.2.7	I <sup>2</sup> C Access Status Register	427
13.2.8	I <sup>2</sup> C Interrupt Status Register	430
13.2.9	I <sup>2</sup> C Interrupt Enable Register	433
13.2.10	I <sup>2</sup> C Interrupt Set Register	435
13.2.11	I <sup>2</sup> C Slave Configuration Register	437
13.2.12	I <sup>2</sup> C Boot Control Register	440
13.2.13	Externally Visible I <sup>2</sup> C Internal Write Address Register	444
13.2.14	Externally Visible I <sup>2</sup> C Internal Write Data Register	445
13.2.15	Externally Visible I <sup>2</sup> C Internal Read Address Register	446
13.2.16	Externally Visible I <sup>2</sup> C Internal Read Data Register	447
13.2.17	Externally Visible I <sup>2</sup> C Slave Access Status Register	448
13.2.18	Externally Visible I <sup>2</sup> C Internal Access Control Register	450
13.2.19	Externally Visible I <sup>2</sup> C Status Register	452
13.2.20	Externally Visible I <sup>2</sup> C Enable Register	456
13.2.21	Externally Visible I <sup>2</sup> C Outgoing Mailbox Register	460
13.2.22	Externally Visible I <sup>2</sup> C Incoming Mailbox Register	461
13.2.23	I <sup>2</sup> C Event and Event Snapshot Registers	462
13.2.24	I <sup>2</sup> C New Event Register	466
13.2.25	I <sup>2</sup> C Enable Event Register	469
13.2.26	I <sup>2</sup> C Time Period Divider Register	472
13.2.27	I <sup>2</sup> C Start Condition Setup/Hold Timing Register	473
13.2.28	I <sup>2</sup> C Stop/Idle Timing Register	474
13.2.29	I2C_SD Setup and Hold Timing Register	475
13.2.30	I2C_SCLK High and Low Timing Register	476
13.2.31	I2C_SCLK Minimum High and Low Timing Register	477
13.2.32	I2C_SCLK Low and Arbitration Timeout Register	478
13.2.33	I <sup>2</sup> C Byte/Transaction Timeout Register	479
13.2.34	I <sup>2</sup> C Boot and Diagnostic Timer	480

13.2.35	I <sup>2</sup> C Boot Load Diagnostic Progress Register	481
13.2.36	I <sup>2</sup> C Boot Load Diagnostic Configuration Register	482
<b>A.</b>	<b>Serial RapidIO Protocol Overview</b>	<b>483</b>
A.1	Protocol	483
A.2	Packets	483
A.2.1	Control Symbols	484
A.3	Physical Layer	484
A.3.1	PCS Layer	484
A.3.2	PMA Layer	484
A.3.3	Physical Protocol	484
<b>B.</b>	<b>Clocking</b>	<b>489</b>
B.1	Line Rate Support	489
B.1.1	Register Requirements Using 125 MHz S_CLK for a 3.125 Gbps Link Rate	490
B.2	P_CLK Programming	493
B.2.1	RapidIO Specifications Directly Affected by Changes in the P_CLK Frequency	493
B.2.2	IDT Specific Timers	496
B.2.3	I <sup>2</sup> C interface and Timers	497
B.2.4	Other Performance Factors	503
<b>C.</b>	<b>PRBS Scripts</b>	<b>505</b>
C.1	Tsi578_start_prbs_all.txt Script	505
C.2	Tsi578_framer_disable.txt Script	507
C.3	Tsi578_sync_prbs_all.txt Script	508
C.4	Tsi578_read_prbs_all.txt Script	511
<b>D.</b>	<b>EEPROM Scripts</b>	<b>515</b>
D.1	Script	515
	<b>Index</b>	<b>523</b>

# Figures

Figure 1:	Block Diagram . . . . .	22
Figure 2:	Processor Farm Mezzanine Diagram . . . . .	23
Figure 3:	Switch Carrier Blade . . . . .	23
Figure 4:	Tsi578 MAC Block Diagram . . . . .	29
Figure 5:	LUT Mode of Operation . . . . .	39
Figure 6:	Flat Mode Routing . . . . .	41
Figure 7:	Flat Mode Routing Example . . . . .	42
Figure 8:	Flat Mode LUT Configuration Example . . . . .	43
Figure 9:	Hierarchical Mode . . . . .	46
Figure 10:	Hierarchical Mode Routing Example . . . . .	47
Figure 11:	LOLS Silent Period . . . . .	63
Figure 12:	Tsi578 MAC Block Diagram . . . . .	66
Figure 13:	Port Configuration . . . . .	68
Figure 14:	Drive Strength and Equalization Waveform . . . . .	78
Figure 15:	Tsi578 Loopbacks . . . . .	79
Figure 16:	ISF Block Diagram . . . . .	86
Figure 17:	Egress Arbitration: Weighted Round Robin and Strict Priority . . . . .	88
Figure 18:	Weighted Round Robin Arbiter per Priority Group . . . . .	89
Figure 19:	Ingress and Egress Packet Queues in Tsi578 . . . . .	91
Figure 20:	Multicast Operation – Option 1 . . . . .	104
Figure 21:	Multicast Operation – Option 2 . . . . .	105
Figure 22:	Multicast Packet Flow in the Tsi578 . . . . .	108
Figure 23:	Relationship Representation . . . . .	112
Figure 24:	Completed Tables at the End of Configuration . . . . .	114
Figure 25:	IDT-specific Multicast Mask Configuration . . . . .	117
Figure 26:	Arbitration Algorithm for Multicast Port . . . . .	118
Figure 27:	Control Symbol Format . . . . .	130
Figure 28:	RapidIO Block Interrupt and Port Write Hierarchy . . . . .	137
Figure 29:	I <sup>2</sup> C Block Diagram . . . . .	145
Figure 30:	I <sup>2</sup> C Reference Diagram . . . . .	146
Figure 31:	Software-initiated Master Transactions . . . . .	148
Figure 32:	Transaction Protocols for Tsi578 as Slave . . . . .	153
Figure 33:	I <sup>2</sup> C Mailbox Operation . . . . .	162
Figure 34:	SMBus Protocol Support . . . . .	165
Figure 35:	SMBus Alert Response Protocol . . . . .	166
Figure 36:	Boot Load Sequence . . . . .	167
Figure 37:	I <sup>2</sup> C Interrupt Generation . . . . .	176
Figure 38:	I <sup>2</sup> C Event and Interrupt Logic . . . . .	178
Figure 39:	I <sup>2</sup> C Timeout Periods . . . . .	182
Figure 40:	I <sup>2</sup> C Bus Timing Diagrams . . . . .	184
Figure 41:	Latency Illustration . . . . .	188
Figure 42:	Congestion and Detection Flowchart . . . . .	197

---

Figure 43: Congestion Example . . . . .	200
Figure 44: Register Access From JTAG - Serial Data In . . . . .	202
Figure 45: Register Access From JTAG - Serial Data Out . . . . .	202
Figure 46: Tsi578 Clocking Architecture . . . . .	206
Figure 47: Signal Groupings . . . . .	218

## Tables

Table 1:	Error Summary	50
Table 2:	Lookup Table States	51
Table 3:	Examples of Maintenance Packets with Hop Count = 0 and Associated Tsi578 Responses	53
Table 4:	Tsi578 Port Numbering	67
Table 5:	Reference Clock Frequency and Supported Serial RapidIO Data Rates	70
Table 6:	Serial Port Power-down Procedure	73
Table 7:	Lane Sequence	75
Table 8:	Patterns Supported by Generator	80
Table 9:	Patterns Supported by Matcher	82
Table 10:	Sample Register settings for WRR in a given priority group (WRR_EN=1)	90
Table 11:	Examples of Use of Watermarks	93
Table 12:	Multicast Terminology	105
Table 13:	Tsi578 Events	122
Table 14:	Error Rate Error Events	132
Table 15:	Port Write Packet Data Payload — Error Reporting	135
Table 16:	Port x Error and Status Register Status	139
Table 17:	Externally Visible I <sup>2</sup> C Register Map	155
Table 18:	Format for Boot Loadable EEPROM	171
Table 19:	Sample EEPROM Loading Two Registers	171
Table 20:	Sample EEPROM With Chaining	172
Table 21:	I <sup>2</sup> C Error Handling	174
Table 22:	I <sup>2</sup> C Interrupt to Events Mapping	178
Table 23:	Performance Monitoring Parameters	189
Table 24:	4x/1x Latency Numbers Under No Congestion	194
Table 25:	4x/1x Multicast Latency Numbers Under No Congestion	196
Table 26:	Tsi578 Input Reference Clocks	207
Table 27:	Tsi578 Clock Domains	208
Table 28:	Power-Up Options Signals	213
Table 29:	Signal Types	215
Table 30:	Tsi578 Port Numbering	216
Table 31:	Tsi578 Signal Descriptions	219
Table 32:	Address Rules	229
Table 33:	Register Access Types	230
Table 34:	Port Numbering	231
Table 35:	Register map overview	233
Table 36:	Register Map	234
Table 37:	Physical Interface Register Offsets	268
Table 38:	Error Management Registers	285
Table 39:	STOP_FAIL_EN and DROP_EN Setting	286
Table 40:	ERR_TYPE Values	300
Table 41:	IDT-Specific Broadcast RapidIO Registers	307
Table 42:	IDT-Specific Per-Port Performance Registers	308



---

Table 43:	IDT-Specific Per-Port Performance Registers . . . . .	331
Table 44:	IDT-Specific RapidIO Registers . . . . .	361
Table 45:	Serial Port Electrical Layer Registers . . . . .	362
Table 46:	TX_LVL Values . . . . .	373
Table 47:	AC JTAG level programmed by ACJT_LVL[4:0] . . . . .	374
Table 48:	SerDes Register Map . . . . .	402
Table 49:	I <sup>2</sup> C Register Map . . . . .	415
Table 50:	Master Operation Sequence . . . . .	424
Table 51:	Special Characters and Encoding . . . . .	485
Table 52:	Control Symbol Construction . . . . .	486
Table 53:	Tsi578 Supported Line Rates . . . . .	489
Table 54:	Timer Values with P_CLK and TVAL Variations . . . . .	494
Table 55:	Timer Values with DISCOVERY_TIMER and P_CLK Variations . . . . .	495
Table 56:	Timer Values with P_CLK and DLT_THRESH Variations . . . . .	496

## About this Document

This section discusses the following topics:

- “Scope” on page 17
- “Document Conventions” on page 17
- “Revision History” on page 18

## Scope

The *Tsi578 User Manual* discusses the features, capabilities, and configuration requirements for the Tsi578. It is intended for hardware and software engineers who are designing system interconnect applications with the device.

## Document Conventions

This document uses the following conventions.

### Non-differential Signal Notation

Non-differential signals are either active-low or active-high. An active-low signal has an active state of logic 0 (or the lower voltage level), and is denoted by a lowercase “\_b”. An active-high signal has an active state of logic 1 (or the higher voltage level), and is not denoted by a special character. The following table illustrates the non-differential signal naming convention.

State	Single-line signal	Multi-line signal
Active low	NAME_b	NAME_b[3]
Active high	NAME	NAME[3]

### Differential Signal Notation

Differential signals consist of pairs of complement positive and negative signals that are measured at the same time to determine a signal’s active or inactive state (they are denoted by “\_p” and “\_n”, respectively). The following table illustrates the differential signal naming convention.

State	Single-line signal	Multi-line signal
Inactive	NAME_p = 0 NAME_n = 1	NAME_p[3] = 0 NAME_n[3] = 1
Active	NAME_p = 1 NAME_n = 0	NAME_p[3] is 1 NAME_n[3] is 0

## Object Size Notation

- A *byte* is an 8-bit object.
- A *word* is a 16-bit object.
- A *doubleword* (Dword) is a 32-bit object.

## Numeric Notation

- Hexadecimal numbers are denoted by the prefix *0x* (for example, 0x04).
- Binary numbers are denoted by the prefix *0b* (for example, 0b010).
- Registers that have multiple iterations are denoted by {*x..y*} in their names; where *x* is first register and address, and *y* is the last register and address. For example, REG{0..1} indicates there are two versions of the register at different addresses: REG0 and REG1.

## Symbols



This symbol indicates a basic design concept or information considered helpful.



This symbol indicates important configuration information or suggestions.



This symbol indicates procedures or operating levels that may result in misuse or damage to the device.

## Document Status Information

- Preliminary – Contains information about a product that is near production-ready, and is revised as required.
- Formal – Contains information about a final, customer-ready product, and is available once the product is released to production.

## Revision History

### June 6, 2016, Formal

- Updated “**Reserved Register Addresses and Fields**”
- Updated the second caution in “**RapidIO Error Management Extension Registers**”
- Updated the description of bit 31 (Reserved) in the following registers: “**SRIO MAC x SerDes Configuration Channel 0**”, “**SRIO MAC x SerDes Configuration Channel 1**”, “**SRIO MAC x SerDes Configuration Channel 2**”, and “**SRIO MAC x SerDes Configuration Channel 3**”
- Removed Ordering Information from the manual. This information now resides solely in the *Tsi578 Hardware Manual*.

---

## February 19, 2015, Formal

- Updated the “Ordering Information”

## September 16, 2014, Formal

- Updated step 2 in the “Hot Extraction” procedure
- Added a new section, “Lane Sync Timer”
- Updated “Power-Down Options”
- Updated Figure 14: Drive Strength and Equalization Waveform
- Added a new section, “Multicast Operation with Multiple Tsi57x Switches”
- Updated steps 3 and 4 in “Control Symbol Example”
- Updated the description of Fatal Port Error in Table 13: Tsi578 Events
- Updated the description of “Per-Port Reset”
- Updated the description of “RapidIO Port x Error and Status CSR”.PORT\_ERR
- Updated “Tsi578\_read\_prbs\_all.txt Script”

## May 25, 2012, Formal

- Updated the second step in “Removing a Destination ID to Multicast Mask Association”
- Updated the second paragraph in “Payload”
- Updated “Port-writes and Multicast”
- Updated the registers listed in “Global Registers to Program after Port Power Down”
- Added a note about how SW\_RST\_b is the only external indicator that a reset request has been received to “System Control of Resets” and Table 31

## November 18, 2010, Formal

- Added more information about “Lookup Table Entry States”
- Added more information about “Port Aggregation: 1x and 4x Modes”
- Added a note to the “SRIO MAC x SerDes Configuration Global” register
- Added more information about “SRIO MAC x Digital Loopback and Clock Selection Register”.DLT\_THRESH

## July 2009, Formal

This is the production version of the manual. The document has been updated with IDT formatting. There have been no technical changes.



---

# 1. Functional Overview

This chapter describes the main features and functions of the Tsi578. This chapter includes the following information:

- “Overview” on page 21
- “Serial RapidIO Interface” on page 26
- “Serial RapidIO Electrical Interface” on page 28
- “Multicast Engine” on page 27
- “Internal Switching Fabric (ISF)” on page 30
- “Internal Register Bus (AHB)” on page 30
- “I<sup>2</sup>C Interface” on page 30
- “JTAG Interface” on page 32

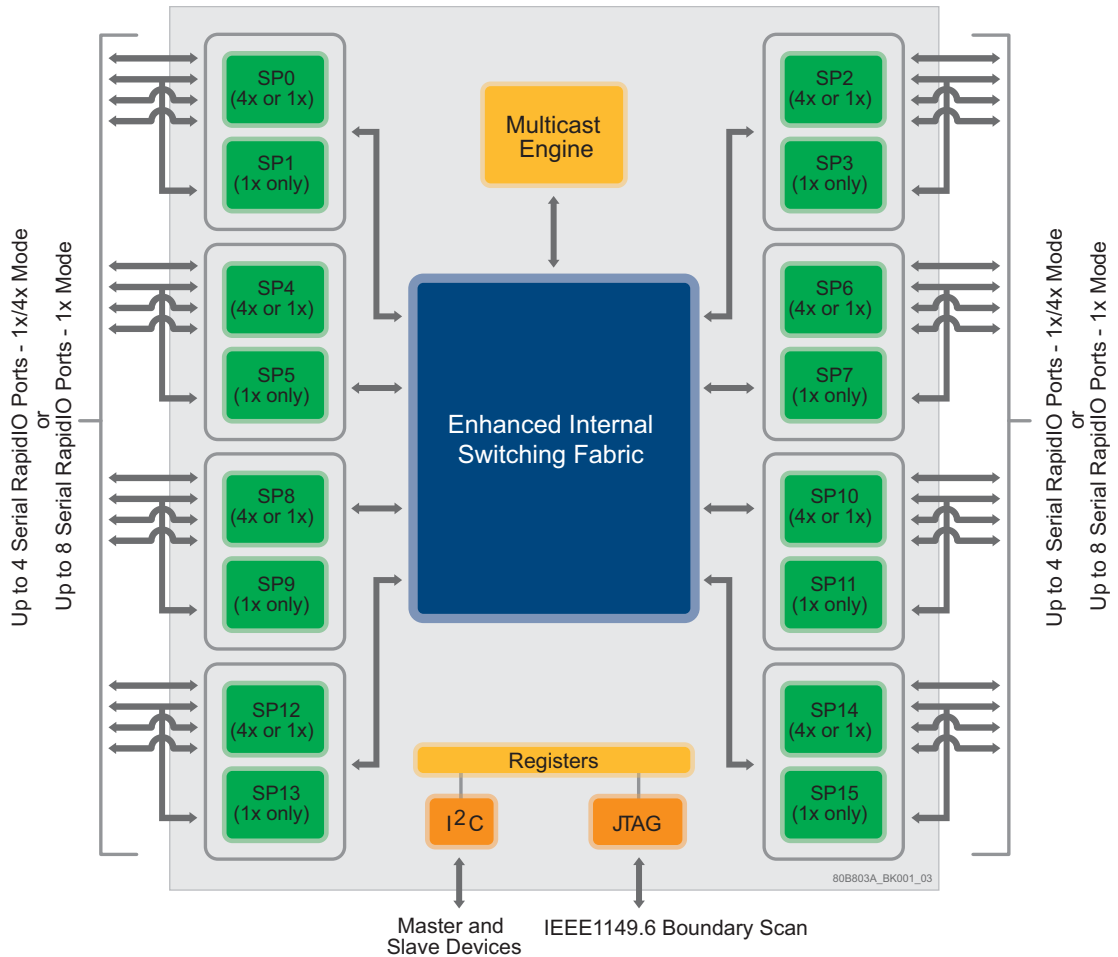
---

## 1.1 Overview

The IDT Tsi578 is a third-generation RapidIO switch supporting 80 Gbits/s aggregate bandwidth. The Tsi578 is part of a family of switches that enable customers to develop systems with robust features and high performance at low cost.

The Tsi578 provides designers and architects with maximum scalability to design the device into a wide range of applications. Flexible port configurations can be selected through multiple port width and frequency options.

Building on the industry leading Tsi568A<sup>TM</sup> Serial RapidIO Switch, the Tsi578 contains all the benefits of its predecessor plus enhances the fabric switching capabilities through the addition of multicast, traffic management through scheduling algorithms, programmable buffer depth, and fabric performance monitoring to supervise and manage traffic flow.

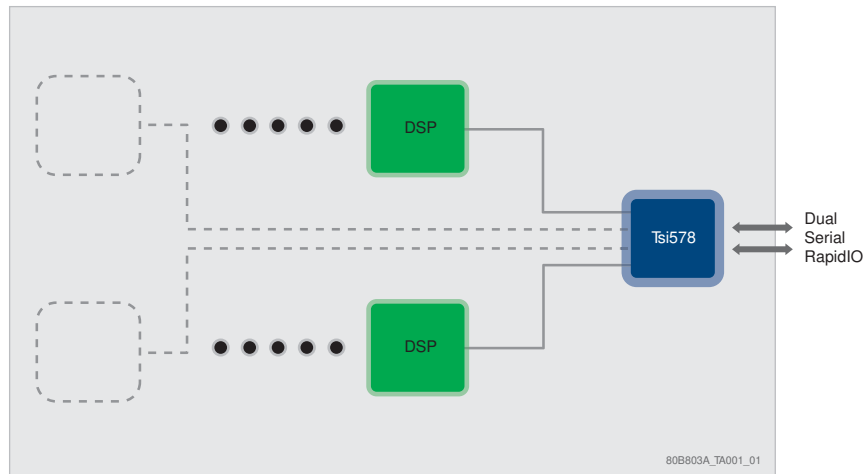
**Figure 1: Block Diagram**

Embedded applications further benefit from the ability to route packets to over 64,000 endpoints through hierarchical lookup tables, independent unicast and multicast routing mechanisms, and error management extensions that provide proactive issue notification to the fabric controller. In addition, the Tsi578 supports both in-band serial RapidIO access and out-of-band access to the full fabric register set through the I2C interface.

### **Typical Applications**

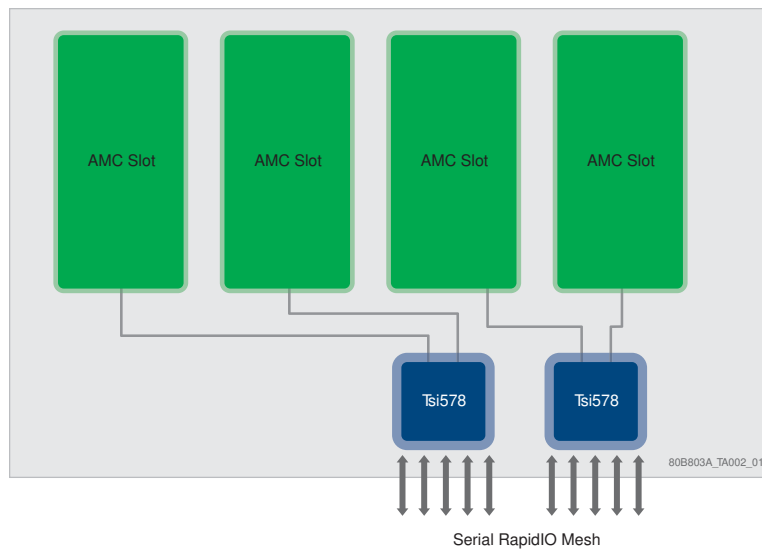
The Tsi578 can be used in many embedded communication applications. It provides chip-to-chip interconnect between I/O devices and can replace existing proprietary backplane fabrics for board-to-board interconnect which improves system cost and product time-to-market.

**Figure 2: Processor Farm Mezzanine Diagram**



The Tsi578 provides traffic aggregation through packet prioritization when it is used with RapidIO-enabled I/O devices. When it is in a system with multiple RapidIO-enabled processors it provides high performance peer-to-peer communication through its non-blocking switch fabric.

**Figure 3: Switch Carrier Blade**





## 1.1.1 Features

The Tsi578 contains the following features:

### *Electrical Layer Serial RapidIO Features*

- Up to 8 ports in 4x Serial mode
- Up to 16 ports in 1x Serial mode (each 4x port can be configured independently as two 1x ports)
- Operating baud rate per data lane: 1.25 Gbit/s, 2.5 Gbit/s, or 3.125Gbit/s
- Full duplex bandwidth:
  - 12.5 Gbit/s inbound and 12.5 Gbit/s outbound bandwidth at 3.125 GHz for a port configured for 4x mode<sup>1</sup>
  - 3.125 Gbit/s inbound and 3.125 Gbit/s outbound bandwidth at 3.125 GHz for a port configured for 1x mode<sup>2</sup>
- Programmable serial transmit current with pre-emphasis equalization
- Loopback support for system testing
- Hot-insertion capable I/Os and hardware support
- Per-port power down modes to reduce power consumption
- Ability to reverse the bit ordering of a 4x port to simplify PCB layout

### *Transport Layer RapidIO Features*

- Dedicated destination ID lookup table per port, used to direct packets through the switch
- Supports both hierarchical lookup tables and flat mode lookup tables (512 destination IDs per lookup table)
- Supports an optional, unique hierarchical destination ID lookup table covering all 64K possible destinations ID
- Low-latency forwarding of the Multicast-Event control symbol
- Error management capability
- Performance monitoring capability
- Reset-system interrupt support
- Debug packet generation in debug mode

### *Multicast Engine Features*

- One multicast engine provides dedicated multicast resources without impacting throughput on the ports
- Eight multicast groups
- Sustained multicast output bandwidth, up to 10 Gbit/s per egress port

---

1. Usable data rate is 10 Gbit/s rather than 12.5 Gbit/s due to 8B/10B physical layer encoding.

2. Usable data rate is 2.5 Gbit/s rather than 3.125 Gbit/s due to 8B/10B physical layer encoding.

- 10 Gbit/s of instantaneous multicast input bandwidth<sup>1</sup>
- Packets are replicated to each egress port in parallel
- The multicast engine can accept a bursts of traffic with different packet sizes
- Arbitration at the egress port to allow management of resource contention between multicast or non-multicast traffic.



System behavior when multicasting of packets which require responses is not defined in the *RapidIO Interconnect Specification (Revision 1.3) - Part 11 Multicast Specification*.

### **Other Device Interfaces**

- Master and Slave mode I<sup>2</sup>C port, supports up to 8 EEPROMs
- Optionally loads default configuration from ROMs during boot-up, through I<sup>2</sup>C
- Ability to read and write EEPROMs through I<sup>2</sup>C during system operation
- IEEE 1149.1 and 1149.6 boundary scan, with register access

### **Internal switching fabric (ISF)**

- Full-duplex, 80 Gbps line rate, non-blocking switching fabric
- Prevents head-of-line blocking on each port
- Eight packet buffers per ingress port
- Eight packet buffers per egress port

### **Register Access**

- Registers can be accessed from any RapidIO interface and both the JTAG interface and I<sup>2</sup>C
- Optionally loads default configuration from ROMs during boot-up, through I<sup>2</sup>C
- Supports one outstanding maintenance transaction per interface
- Supports 32-bit wide (4 byte) register access

---

1. All bandwidths assume the internal switching fabric is clocked at 156.25 MHz.