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IDT® Tsi578
Serial RapidIO Switch

User Manual

June 6, 2016

Contents

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About this Document

This section discusses the following topics:

Scope

The *Tsi578 User Manual* discusses the features, capabilities, and configuration requirements for the Tsi578. It is intended for hardware and software engineers who are designing system interconnect applications with the device.

Document Conventions

This document uses the following conventions.

Non-differential Signal Notation

Non-differential signals are either active-low or active-high. An active-low signal has an active state of logic 0 (or the lower voltage level), and is denoted by a lowercase "_b". An active-high signal has an active state of logic 1 (or the higher voltage level), and is not denoted by a special character. The following table illustrates the non-differential signal naming convention.

State	Single-line signal	Multi-line signal
Active low	NAME_b	NAME_b[3]
Active high	NAME	NAME[3]

Differential Signal Notation

Differential signals consist of pairs of complement positive and negative signals that are measured at the same time to determine a signal's active or inactive state (they are denoted by "_p" and "_n", respectively). The following table illustrates the differential signal naming convention.

State	Single-line signal	Multi-line signal
Inactive	NAME_p = 0 NAME_n = 1	NAME_p[3] = 0 NAME_n[3] =1
Active	NAME_p = 1 NAME_n = 0	NAME_p[3] is 1 NAME_n[3] is 0

Object Size Notation

- A *byte* is an 8-bit object.
- A *word* is a 16-bit object.
- A *doubleword* (Dword) is a 32-bit object.

Numeric Notation

- Hexadecimal numbers are denoted by the prefix *0x* (for example, 0x04).
- Binary numbers are denoted by the prefix *0b* (for example, 0b010).
- Registers that have multiple iterations are denoted by {x..y} in their names; where *x* is first register and address, and *y* is the last register and address. For example, REG{0..1} indicates there are two versions of the register at different addresses: REG0 and REG1.

Symbols

This symbol indicates a basic design concept or information considered helpful.

This symbol indicates important configuration information or suggestions.

This symbol indicates procedures or operating levels that may result in misuse or damage to the device.

Document Status Information

- Preliminary – Contains information about a product that is near production-ready, and is revised as required.
- Formal – Contains information about a final, customer-ready product, and is available once the product is released to production.

Revision History

June 6, 2016, Formal

- Updated "Reserved Register Addresses and Fields"
- Updated the second caution in "RapidIO Error Management Extension Registers"
- Updated the description of bit 31 (Reserved) in the following registers: "SRIO MAC x SerDes Configuration Channel 0", "SRIO MAC x SerDes Configuration Channel 1", "SRIO MAC x SerDes Configuration Channel 2", and "SRIO MAC x SerDes Configuration Channel 3"
- Removed Ordering Information from the manual. This information now resides solely in the *Tsi578 Hardware Manual*.

February 19, 2015, Formal

- Updated the "Ordering Information"

September 16, 2014, Formal

- Updated step 2 in the "Hot Extraction" procedure
- Added a new section, "Lane Sync Timer"
- Updated "Power-Down Options"
- Updated Figure 14: Drive Strength and Equalization Waveform
- Added a new section, "Multicast Operation with Multiple Tsi57x Switches"
- Updated steps 3 and 4 in "Control Symbol Example"
- Updated the description of Fatal Port Error in Table 13: Tsi578 Events
- Updated the description of "Per-Port Reset"
- Updated the description of "RapidIO Port x Error and Status CSR".PORT_ERR
- Updated "Tsi578_read_prbs_all.txt Script"

May 25, 2012, Formal

- Updated the second step in "Removing a Destination ID to Multicast Mask Association"
- Updated the second paragraph in "Payload"
- Updated "Port-writes and Multicast"
- Updated the registers listed in "Global Registers to Program after Port Power Down"
- Added a note about how SW_RST_b is the only external indicator that a reset request has been received to "System Control of Resets" and Table 31

November 18, 2010, Formal

- Added more information about "Lookup Table Entry States"
- Added more information about "Port Aggregation: 1x and 4x Modes"
- Added a note to the "SRIO MAC x SerDes Configuration Global" register
- Added more information about "SRIO MAC x Digital Loopback and Clock Selection Register".DLT_THRESH

July 2009, Formal

This is the production version of the manual. The document has been updated with IDT formatting. There have been no technical changes.

1. Functional Overview

This chapter describes the main features and functions of the Tsi578. This chapter includes the following information:

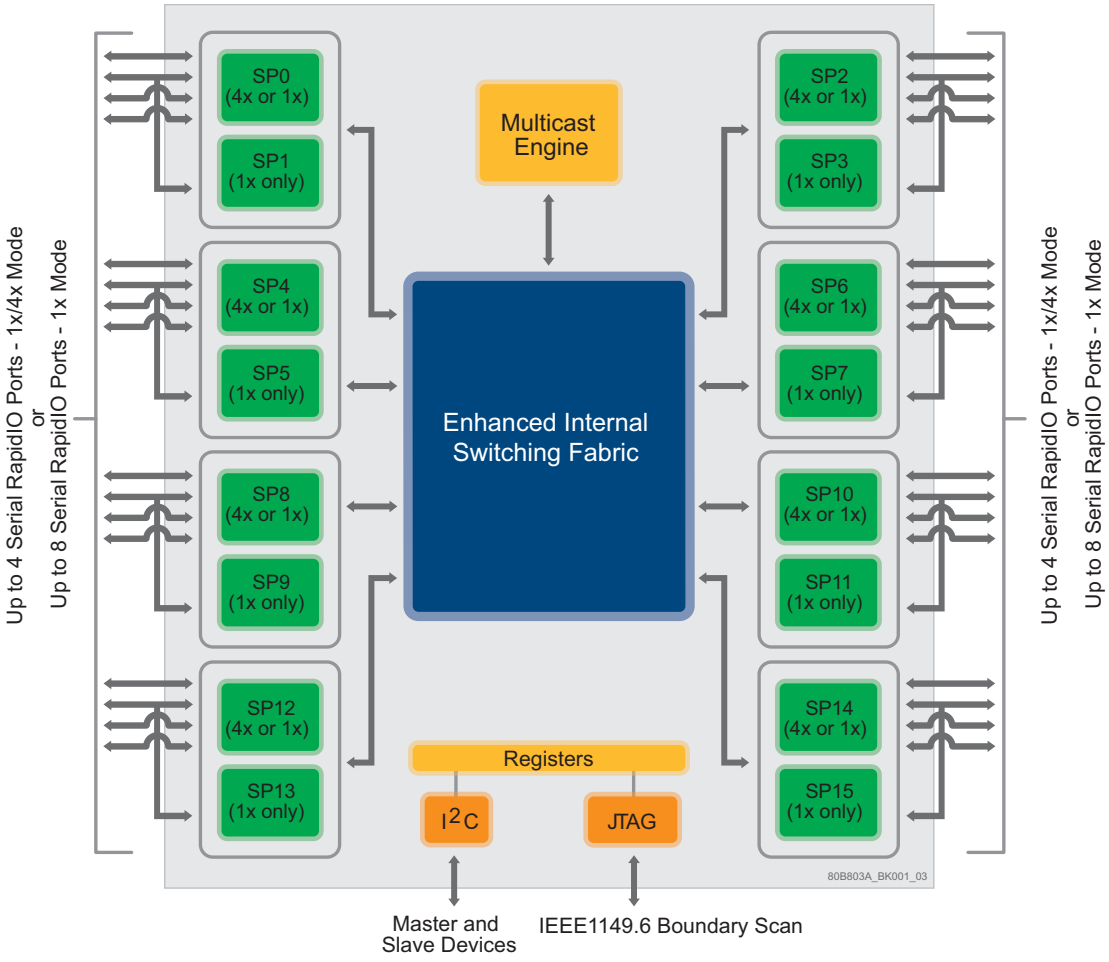
1.1 Overview

The IDT Tsi578 is a third-generation RapidIO switch supporting 80 Gbits/s aggregate bandwidth. The Tsi578 is part of a family of switches that enable customers to develop systems with robust features and high performance at low cost.

The Tsi578 provides designers and architects with maximum scalability to design the device into a wide range of applications. Flexible port configurations can be selected through multiple port width and frequency options.

Building on the industry leading Tsi568A™ Serial RapidIO Switch, the Tsi578 contains all the benefits of its predecessor plus enhances the fabric switching capabilities through the addition of multicast, traffic management through scheduling algorithms, programmable buffer depth, and fabric performance monitoring to supervise and manage traffic flow.

Figure 1: Block Diagram

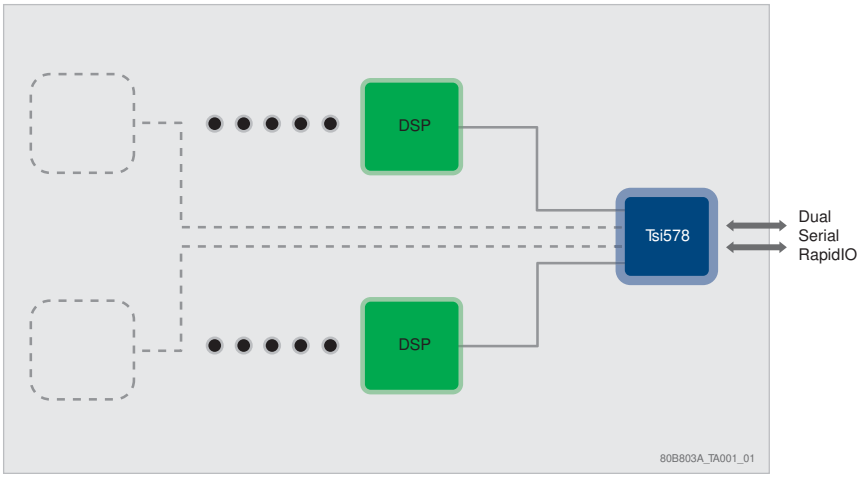


Embedded applications further benefit from the ability to route packets to over 64,000 endpoints through hierarchical lookup tables, independent unicast and multicast routing mechanisms, and error management extensions that provide proactive issue notification to the fabric controller. In addition, the Tsi578 supports both in-band serial RapidIO access and out-of-band access to the full fabric register set through the I2C interface.

Typical Applications

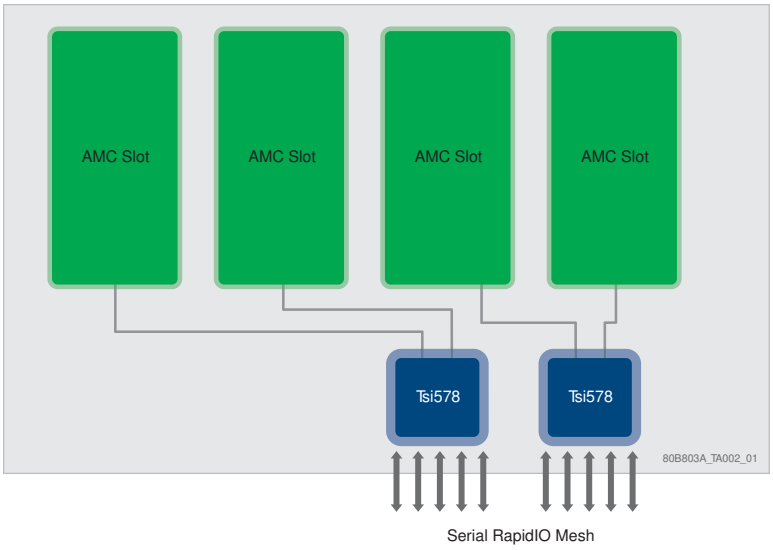
The Tsi578 can be used in many embedded communication applications. It provides chip-to-chip interconnect between I/O devices and can replace existing proprietary backplane fabrics for board-to-board interconnect which improves system cost and product time-to-market.

Figure 2: Processor Farm Mezzanine Diagram



The Tsi578 provides traffic aggregation through packet prioritization when it is used with RapidIO-enabled I/O devices. When it is in a system with multiple RapidIO-enabled processors it provides high performance peer-to-peer communication through its non-blocking switch fabric.

Figure 3: Switch Carrier Blade



1.1.1 Features

The Tsi578 contains the following features:

Electrical Layer Serial RapidIO Features

- Up to 8 ports in 4x Serial mode
- Up to 16 ports in 1x Serial mode (each 4x port can be configured independently as two 1x ports)
- Operating baud rate per data lane: 1.25 Gbit/s, 2.5 Gbit/s, or 3.125Gbit/s
- Full duplex bandwidth:
  - 12.5 Gbit/s inbound and 12.5 Gbit/s outbound bandwidth at 3.125 GHz for a port configured for 4x mode[1]
  - 3.125 Gbit/s inbound and 3.125 Gbit/s outbound bandwidth at 3.125 GHz for a port configured for 1x mode[2]
- Programmable serial transmit current with pre-emphasis equalization
- Loopback support for system testing
- Hot-insertion capable I/Os and hardware support
- Per-port power down modes to reduce power consumption
- Ability to reverse the bit ordering of a 4x port to simplify PCB layout

Transport Layer RapidIO Features

- Dedicated destination ID lookup table per port, used to direct packets through the switch
- Supports both hierarchical lookup tables and flat mode lookup tables (512 destination IDs per lookup table)
- Supports an optional, unique hierarchical destination ID lookup table covering all 64K possible destinations ID
- Low-latency forwarding of the Multicast-Event control symbol
- Error management capability
- Performance monitoring capability
- Reset-system interrupt support
- Debug packet generation in debug mode

Multicast Engine Features

- One multicast engine provides dedicated multicast resources without impacting throughput on the ports
- Eight multicast groups
- Sustained multicast output bandwidth, up to 10 Gbit/s per egress port

1. Usable data rate is 10 Gbit/s rather than 12.5 Gbit/s due to 8B/10B physical layer encoding.
2. Usable data rate is 2.5 Gbit/s rather than 3.125 Gbit/s due to 8B/10B physical layer encoding.

- 10 Gbit/s of instantaneous multicast input bandwidth[1]
- Packets are replicated to each egress port in parallel
- The multicast engine can accept a bursts of traffic with different packet sizes
- Arbitration at the egress port to allow management of resource contention between multicast or non-multicast traffic.

System behavior when multicasting of packets which require responses is not defined in the *RapidIO Interconnect Specification (Revision 1.3) - Part 11 Multicast Specification*.

Other Device Interfaces

- Master and Slave mode I^2C port, supports up to 8 EEPROMs
- Optionally loads default configuration from ROMs during boot-up, through I^2C
- Ability to read and write EEPROMs through I^2C during system operation
- IEEE 1149.1 and 1149.6 boundary scan, with register access

Internal switching fabric (ISF)

- Full-duplex,80 Gbps line rate, non-blocking switching fabric
- Prevents head-of-line blocking on each port
- Eight packet buffers per ingress port
- Eight packet buffers per egress port

Register Access

- Registers can be accessed from any RapidIO interface and both the JTAG interface and I^2C
- Optionally loads default configuration from ROMs during boot-up, through I^2C
- Supports one outstanding maintenance transaction per interface
- Supports 32-bit wide (4 byte) register access

1. All bandwidths assume the internal switching fabric is clocked at 156.25 MHz.