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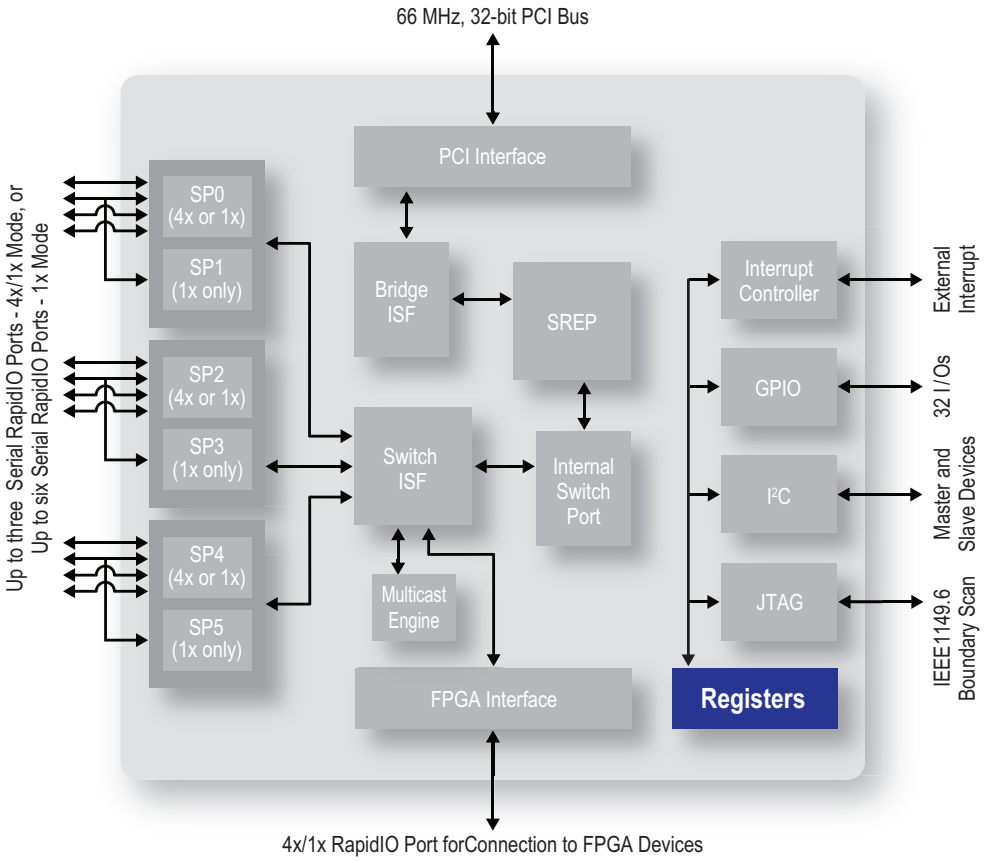
Tsi620™
RapidIO Switch / RapidIO®-to-PCI Bridge

FEATURES

- RapidIO Interface:
  - Up to three ports in 4x mode
  - Up to six ports in 1x mode
- FPGA Interface: Supports RapidIO over XGMII at 1 to 10 Gbps data rate
- PCI Interface that operates up to 66 MHz and supports up to four devices
- Low latency with cut-through capability
- Enhanced SerDes for low-power solution
- High-performance Multicast Engine
- Low power:
  - Leverages Tsi57x technology at 120-200mW per RapidIO port
  - Typical power of less than 4 W
- Software compatibility:
  - RapidIO-to-PCI bridge software compatible with the IDT Tsi108, Tsi109, and Tsi110
  - RapidIO Switch software compatible with Tsi57x products
- Packaging:
  - 27 x 27 mm, 675-pin PBGA
  - Industrial and commercial temperature operating ranges
  - Eutectic and RoHS/Green packages

RapidIO Switch

- Configurable baud rate per data lane: 1.25, 2.5 or 3.125 Gbaud/s
- 10 Gbps inbound and outbound bandwidth at 3.125 Gbaud/s per lane for a 4x mode port
- 50 Gbps aggregate bandwidth
- Loopback support for system testing
- Hot-insertion capable I/Os and hardware support
- Per-port power-down modes to reduce power consumption
- Lane swap of 4x port to simplify PCB layout
- *RapidIO Interconnect Specification (Revision 1.3)* compliant



Device Overview

The Tsi620 provides the functionality of both a serial RapidIO Switch and a RapidIO-to-PCI bridge. The RapidIO Switch offers 50 Gbps aggregate bandwidth, while the RapidIO-to-PCI bridge enables legacy systems to link to the high-bandwidth RapidIO interconnect. The Tsi620 contains all the benefits of IDT's RapidIO switches, and adds interfaces to PCI-enabled processors as well as to low-cost FPGAs.

The Tsi620 allows system designers to develop applications with a variety of interfaces. The device is optimized to reduce the design costs for wireless, networking, storage, and military applications.

Multiple Interfaces

The PCI Interface enables system OEMs to select from a range of processor options to optimize their designs from a cost and software perspective. The Tsi620 allows designers to maintain their investment in existing PCI infrastructure while accessing the bandwidth capabilities of RapidIO.

The FPGA Interface supports a single, 4x/1x RapidIO port. It is a parallel interface that connects to low-cost FPGAs without the need for an XAUIenabled SerDes (Serializer/Deserializer), and has flexible test features including multiple loopback modes.

FEATURES (continued)

RapidIO-to-PCI Bridge

- RapidIO-to-PCI and PCI-to-RapidIO bridging functions
- Non-transparent bridging between PCI and RapidIO

PCI Interface

- 32/64-bit addressing, 32-bit data
- Operates from 25 to 66 MHz
- Provides arbitration for four PCI devices
- Supports vital product data
- Supports message signaled interrupts
- PCI master and target capability
- CompactPCI Hot Swap
- Compliant with the following specifications:
  - PCI Local Bus Specification (Rev. 2.3)
  - PCI Bus Power Management Interface Specification (Rev 1.1)

The Tsi620 allows designers to maintain their investment in existing PCI infrastructure while accessing the bandwidth capabilities of RapidIO.

BENEFITS

- Decreases system costs: RapidIO over XGMII FPGA Interface eliminates the need for an external SerDes or FPGA with embedded SerDes, and reduces latency by up to 300 ns in real-time applications
- Maintains system investment: Allows use of existing PCI infrastructure with the higher bandwidth RapidIO
- Builds on proven technology: The Tsi620 is based on IDT's Tsi57x RapidIO switches

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The RapidIO Advantage

The Tsi620 builds on the RapidIO features of IDT's RapidIO switches. It has low power per port, multicasting, traffic management through scheduling algorithms, programmable buffer depth, and fabric performance monitoring.

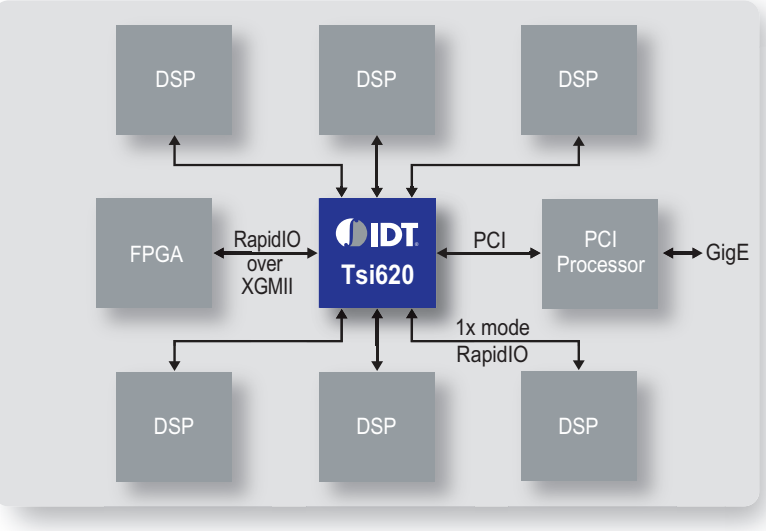
Embedded applications further benefit from the ability to route packets to thousands of endpoints through hierarchical lookup tables, and independent unicast and multicast routing mechanisms. Support for error management extensions provide proactive issue notification to the device's Switch ISF. In addition, the Tsi620 supports both in-band serial RapidIO access and out-ofband access to its registers through the I^2C Interface.

Typical Applications

3G Wireless Baseband

In 3G wireless applications, the architecture is usually divided between chip rate processing in the FPGA, and symbol rate processing in the DSPs. The overall cost of a baseband line card, however, can be reduced by using a Tsi620 to cluster the FPGA, Control Plane Processor, and Symbol Rate DSPs. Because of the Tsi620's SerDes and PCI features, the baseband application can use a low-cost FPGA (without an embedded SerDes) and a processor with a PCI interface (instead of using RapidIO-enabled processors), allowing the reuse of existing software investments. The PCI interface can also connect legacy ASICs directly to a cloud of RapidIO-based multicore DSPs, which previously was not possible using RapidIO switches.

Application Diagram



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