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Tsi721™ Datasheet

April 4, 2016

Table of Contents

List of Figures

List of Tables

About this Document

Topics discussed include the following:

Overview

The *Tsi721 Datasheet* provides signal, electrical, and packaging information about the Tsi721. It is intended for hardware engineers who are designing system interconnect applications with the device.

Document Conventions

This document uses the following conventions.

Non-differential Signal Notation

Non-differential signals are either active-low or active-high. An active-low signal has an active state of logic 0 (or the lower voltage level), and is denoted by a lowercase “n”. An active-high signal has an active state of logic 1 (or the higher voltage level), and is not denoted by a special character. The following table illustrates the non-differential signal naming convention.

State	Single-line signal	Multi-line signal
Active low	NAMEn	NAMEn[3]
Active high	NAME	NAME[3]

Differential Signal Notation

Differential signals consist of pairs of complement positive and negative signals that are measured at the same time to determine a signal’s active or inactive state (they are denoted by “_p” and “_n”, respectively). The following table illustrates the differential signal naming convention.

State	Single-line signal	Multi-line signal
Inactive	NAME_p = 0 NAME_n = 1	NAME_p[3] = 0 NAME_n[3] = 1
Active	NAME_p = 1 NAME_n = 0	NAME_p[3] is 1 NAME_n[3] is 0

Object Size Notation

- A *byte* is an 8-bit object.
- A PCIe *word* is a 16-bit object.
- A PCIe *doubleword* (DW) is a 32-bit object.
- An S-RIO *word* is a 32-bit object.
- An S-RIO *doubleword* (Dword) is a 64-bit object.

Numeric Notation

- Hexadecimal numbers are denoted by the prefix *0x* (for example, 0x04).
- Binary numbers are denoted by the prefix *0b* (for example, 0b010).
- Registers that have multiple iterations are denoted by {x..y} in their names; where *x* is first register and address, and *y* is the last register and address. For example, REG{0..1} indicates there are two versions of the register at different addresses: REG0 and REG1.

Symbols

This symbol indicates important configuration information or suggestions.

This symbol indicates procedures or operating levels that may result in misuse or damage to the device.

Revision History

April 4, 2016

- Added GCLV, GILH, and GILV part numbers to Ordering Information

May 5, 2014

- Updated the description of the V_{IN_DIFF} parameter in Table 32

December 3, 2012

- Updated Ordering Information with production ordering numbers

February 28, 2012

- Added a footnote to Absolute Maximum Ratings, and removed the minimum rating for T_{JN} from the same section
- Added T_{JN} and a footnote to Recommended Operating Conditions

December 16, 2011

- Updated the minimum and maximum values for AVDD10 in Recommended Operating Conditions
- Added Power Consumption data
- Changed the Moisture Sensitivity Level to 4

1. Device Overview

Topics discussed include the following:

1.1 Overview

IDT is the leading supplier of RapidIO® and PCI Express Interconnect solutions, providing a broad portfolio of switches, bridges, IP, and development platforms for defense aerospace, video, imaging, and wireless markets. The Tsi721 is IDT's solution for hardware-based PCIe Gen2 to RapidIO Gen2 protocol conversion in a bridging device.

The Tsi721 converts transactions from PCIe to RapidIO, and vice versa, and provides full line rate bridging at 20 Gbaud. Using the Tsi721, designers can develop heterogeneous systems that leverage the peer-to-peer networking performance of RapidIO while using multiprocessor clusters that may be only PCIe enabled. In addition, applications that require large amounts of data transferred efficiently without processor involvement can be executed using the full line rate of the Tsi721's Block DMA Engine and Messaging Engine.

Key to the Tsi721 is the hardware bridging functionality that converts PCIe transactions to RapidIO, and vice versa. The Tsi721 supports PCIe non-transparent bridging for transaction mapping. The device has both RapidIO and PCIe endpoints embedded in the bridge, and each of its Block DMA/Messaging DMA channels can buffer up to 8 KB of data on the PCIe side.

1.2 Features

The Tsi721 supports the following features.

1.2.1 PCIe Features

- PCIe 2.1 standard compliant
- 5/2.5 Gbaud link speed
- x4/x2/x1 link width
- 128- and 256-byte maximum payload
- Advanced error reporting
- Internal error reporting
- Lane reversal
- Automatic polarity inversion
- Dynamic port width: x4 drops to x1
- ECRC support
- INTx, MSI, and MSI-X support

- Single virtual channel, VC0
- Single traffic class, TC0
  - Generates only PCIe posted/non-posted TLPs with TC0
  - Generates only PCIe Cpl/CplD TLPs with TC matching their requests
  - Accepts PCIe TLPs with any TC
- Four BARs
  - Prefetchable BAR with 32- or 64-bit addressing for PCIe-to-S-RIO bridging
  - Non-prefetchable BAR with 32- or 64-bit addressing for PCIe-to-S-RIO bridging
  - Non-prefetchable BAR with 32-bit addressing for PCIe MWr to S-RIO doorbell bridging
  - Non-prefetchable BAR with 32-bit addressing for Tsi721 internal register access
- Initial credit advertisement programmable through EEPROM
- Dynamic control of credits through registers
- Starvation prevention based on flow control credit updates
- Large buffers
  - 12 KB/2 KB/12 KB input buffers for up to 127 posted/non-posted/completion TLPs
  - 12 KB/2 KB/12 KB output buffers for up to 128 posted/non-posted/completion TLPs
- Debug features
  - Slave analog loopback through a control register
  - Slave loopback using TS1/TS2 ordered sets
  - Master loopback
  - Internal error reporting
  - ECC protection on internal memories

1.2.2 S-RIO Features

- S-RIO 2.1 standard compliant
- 5/3.125/2.5/1.25 Gbaud link speed
- x4/x2/x1 link width
- 34-, 50-, and 66-bit addressing
- 16 destID filters
- 8 S-RIO flows
- 9-KB ingress buffer (32 x 288)
- 9-KB egress buffer (32 x 288)
- Lane reversal
- Lane polarity inversion

1.2.3 Bridging Features

- Store and forward from PCIe to S-RIO
- Store and forward from S-RIO to PCIe
- Line rate support for 64 byte and larger packets
- 32 outstanding PCIe requests to root complex

- 32 outstanding S-RIO NREAD/maintenance read requests to S-RIO network
- 32 outstanding S-RIO NWRITE_R/maintenance write/doorbell requests to S-RIO network
- 12-KB completion reassembly buffer
- 8 windows from PCIe to S-RIO with 8 zones (sub windows) per window
- 8 windows from S-RIO to PCIe
- Initiates and receives the following S-RIO transactions:
  - NREAD
  - SWRITE/NWRITE/NWRITE_R
  - Maintenance read and write
  - Port-write
  - Doorbell
  - Type 8 response
  - Type 13 response
- Initiates and receives the following PCIe transactions:
  - MWr
  - MRd
  - Cpl
  - CplD
- Round-robin scheduling between Mapping Engine, Block DMA Engine, and Messaging traffic to the S-RIO link
- Round-robin scheduling between Mapping Engine, Block DMA Engine, and Messaging traffic to the PCIe link
- Forward bridge
  - Connects PCIe root complex to S-RIO network
  - PCIe Type 0 configuration header

1.2.4 Messaging Features

- 8 Tx queues with one dedicated messaging DMA engine per Tx queue
- 8 Rx queues with one dedicated messaging DMA engine per Rx queue
- Descriptor prefetch per Tx queue
- 32 outstanding PCIe requests to root complex
- 8-KB message segment reassembly buffer per Tx queue
- Round-robin scheduling among Tx queues
- One outstanding message per Tx queue
- 16 receive contexts per Rx queue

1.2.5 Block DMA Engine Features

- 8 DMA channels
- Each DMA channel can perform DMA writes from root complex to S-RIO network, or DMA reads from S-RIO network to root complex
  - DMA from PCIe port to PCIe port is not supported
  - DMA from S-RIO port to S-RIO port is not supported

- Round-robin scheduling among DMA channels
- DMA descriptors for all channels reside on PCIe side
- Scatter-and-gather with descriptor list
- Supports DMA strides
- Supports up to 64 MB data for a single descriptor
- Supports both read and write descriptors per DMA channel
- Dynamic descriptor chaining
- Flexible addressing modes
  - Linear addressing
  - Constant addressing
- Descriptor prefetch
- 32 outstanding PCIe requests to root complex
- 64 outstanding S-RIO NREAD/maintenance read requests to S-RIO network
- 64 outstanding S-RIO NWRITE_R/maintenance write requests to S-RIO network
- Supports the following S-RIO transactions:
  - NREAD
  - NWRITE
  - SWRITE
  - NWRITE_R
  - Maintenance read
  - Maintenance write

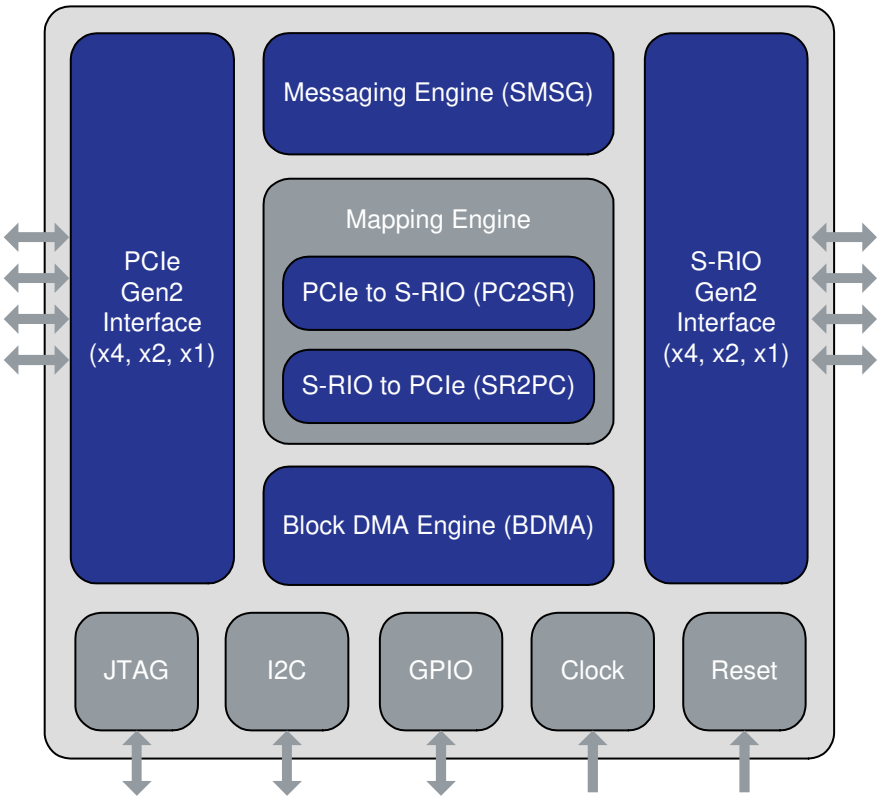
1.2.6 Miscellaneous Features

- I^2C interface supports the following:
  - As a slave, being read/written by an external master during normal operations
  - As a master, reading external EEPROM during boot load
  - As a master, reading/writing other external devices during normal operations
- JTAG 1149.1, 1149.6 (AC JTAG)
- 16 GPIO pins

1.3 Block Diagram

The Tsi721 block diagram is displayed in the following figure. The five main functions of the device are briefly described below.

Figure 1: Block Diagram



1.3.1 PCIe Interface

The PCIe Interface performs all the physical, data link, and transport layer protocols associated with PCIe.

1.3.2 S-RIO Interface

The S-RIO Interface performs all the physical and transport layer protocols associated with S-RIO.

1.3.3 Messaging Engine

The Messaging Engine uses S-RIO messaging logical layer functions with dedicated messaging DMA channels per Tx queue and per Rx queue.

1.3.4 Mapping Engine

The Mapping Engine maps between PCIe and S-RIO transactions, including segmentation and reassembly as required.

1.3.5 Block DMA Engine

The Block DMA Engine uses 8 DMA channels, where descriptors of each DMA channel can perform read or write.

1.4 Typical Applications

The Tsi721 supports the following typical applications:

- Defense and aerospace
  - Radar
  - Sonar
  - Navigations systems
- Medical imaging
  - CT scanners
  - MRIs
- Video
  - Teleconferencing
  - Head end
- Wireless
  - Baseband cards with x86

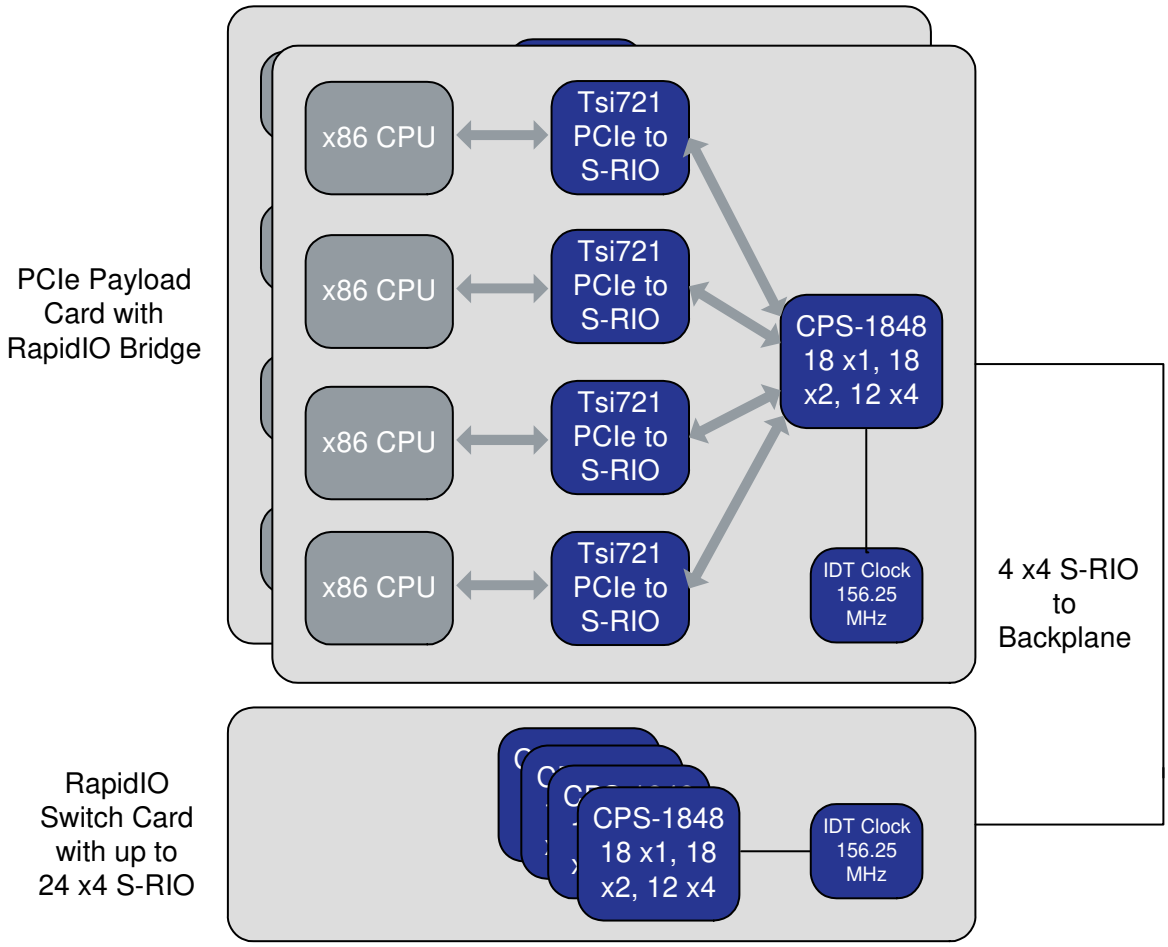
Three of Tsi721's typical applications – defense/aerospace, video/imaging, and wireless – are discussed in the following sections.

1.4.1 Defense/Aerospace Application

In defense applications, the Tsi721 supports the use of PCIe enabled x86 processors to RapidIO backplanes. This provides system designers with the best of both worlds: the floating point and MIPs horsepower of the latest generation of x86 solutions, with the superior peer-to-peer networking performance of RapidIO architectures.

By using the Tsi721 combined with IDT's RapidIO Gen2 switches, payload processor cards with x86 processors can be used with existing RapidIO 1.3 backplanes operating at up to 3.125 Gbaud, or the same card can be used with RapidIO Gen2 compatible backplanes operating at 5 Gbaud.

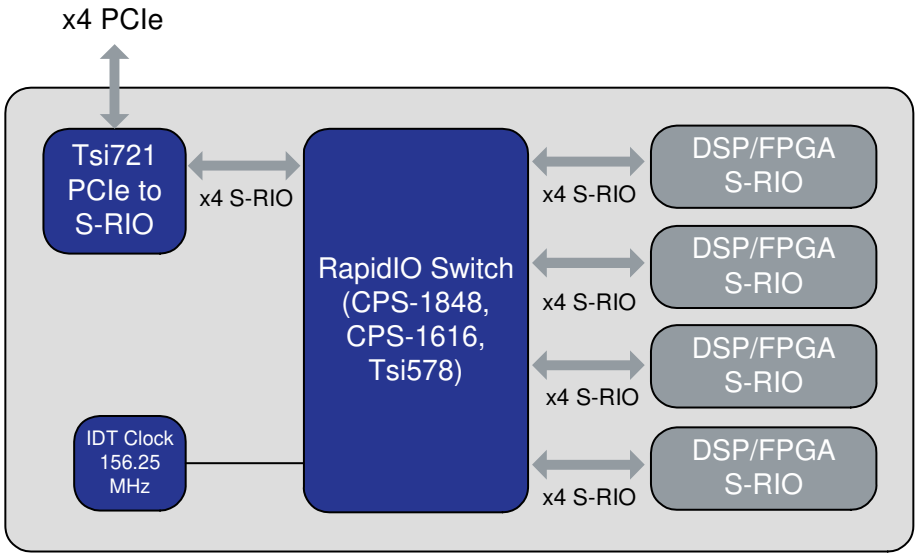
Figure 2: Defense/Aerospace Application



1.4.2 Video and Imaging Application

In video and imaging applications, system designers need to cluster large numbers of DSPs or FPGAs to perform encoding/decoding/trans coding, or do FFTs (Fast Fourier Transform) on large arrays of data. The RapidIO protocol is optimal for this DSP/FPGA cluster requirement. However, the analog front-end to the system is usually a sensor with streaming data terminated in an FPGA (for example, a camera subsystem). This is usually in an PCIe network, often with a PC back-end. In these applications the designer needs to bridge between a PCIe network and the RapidIO DSP/FPGA cluster. The Tsi721 is ideal for this application.

Figure 3: Video and Imaging Application

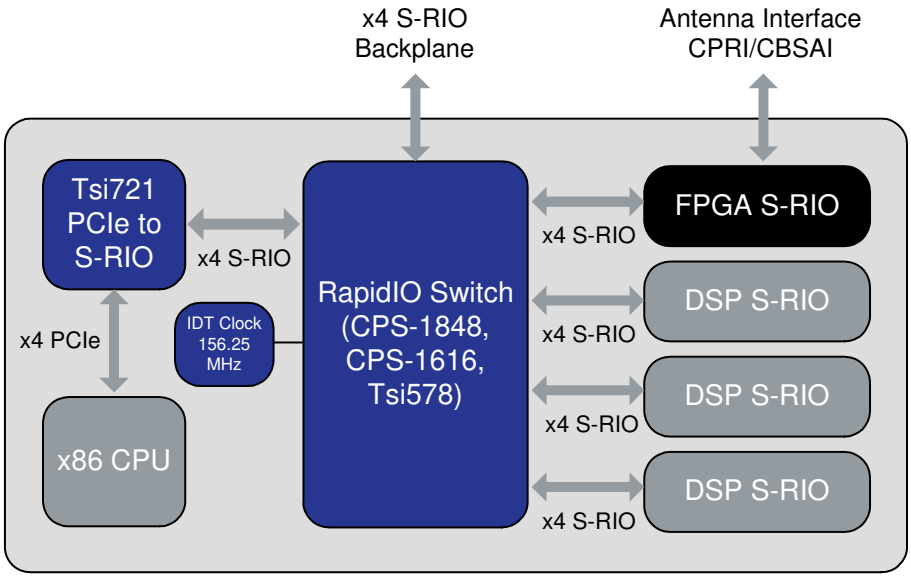


1.4.3 Wireless Application

In wireless base stations, the incumbent interconnect technology in the baseband processing cards – LTE, WiMAX, WCDMA, and TD-SCDMA – is RapidIO. RapidIO connects a cluster of DSPs, processor, and FPGA, locally on the baseband processor for MAC and PHY layer processing. However, the LTE standard pushes the performance available in existing RapidIO enabled microprocessors.

The Tsi721 provides wireless OEMs with an additional option to use an x86 processor with superior MIPs in a baseband card that is predominantly RapidIO. In these card designs, RapidIO is the interconnect between devices and functions as the backplane interconnect. x86 processors can now be used with other RapidIO devices on the baseband card and leverage the messaging performance of RapidIO for this peer-to-peer multiprocessor network.

Figure 4: Wireless Application



2. Signals

Topics discussed include the following:

2.1 Overview

The following conventions are used in this chapter:

- Signals with the suffix “P” are the positive half of a differential pair.
- Signals with the suffix “N” are the negative half of a differential pair.
- Signals with the suffix “n” are active low.

Signals are classified according to the types defined in the following table.

Table 1: Signal Types

Pin Type	Definition
I	3.3/2.5V LVTTL Input
O	3.3/2.5V LVTTL Output
IO	3.3/2.5V LVTTL Bidirectional
IO-OD	3.3/2.5V LVTTL Bidirectional Open Drain
OD	3.3/2.5V LVTTL Open Drain
I-PU	3.3/2.5V LVTTL Input with Pull-up
I-PD	3.3/2.5V LVTTL Input with Pull-down

Table 1: Signal Types (Continued)

Pin Type	Definition
IO-PD	3.3/2.5V LVTTL Bidirectional with Pull-down
IO-PU	3.3/2.5V LVTTL Bidirectional with Pull-up
PCIE_O	Differential CML PCIe output
PCIE_I	Differential CML PCIe input
SRIO_O	Differential CML S-RIO output
SRIO_I	Differential CML S-RIO input
DIFF_I	Differential CML input
PWR	Power
GND	Ground

2.2 Ballmap

Figure 5: Ballmap

	1	2	3	4	5	6	7	8	9	10	11	12
A	NO_BALL	GPIO[9]	VSS	PCRP[0]	PCTP[0]	PCTP[1]	PCRP[1]	PCRP[2]	PCTP[2]	PCTP[3]	PCRP[3]	PCCLKP
B	GPIO[0]	GPIO[10]	VSS	PCRN[0]	PCTN[0]	PCTN[1]	PCRN[1]	PCRN[2]	PCTN[2]	PCTN[3]	PCRN[3]	PCCLKN
C	GPIO[1]	GPIO[11]	VSS	VSS	AVDD25	AVDD25	AVDD25	AVDD25	VSS	VSS	VSS	PCBIAS
D	GPIO[2]	GPIO[12]	VDDIO	AVTT	AVTT	VSS	VSS	AVDD10	AVDD10	VSS	TDO	PCRSTOn
E	GPIO[3]	GPIO[13]	VDDIO	AVTT	VDD	VSS	VSS	VDD	AVDD10	VDDIO	TCK	TEST_BCE
F	GPIO[4]	GPIO[14]	VDDIO	AVTT	VSS	VDD	VDD	VSS	AVDD10	VDDIO	TDI	TEST_ON
G	GPIO[5]	GPIO[15]	VDDIO	AVTT	VSS	VDD	VDD	VSS	AVDD10	VDDIO	VSS	TEST_BIDIR_CTL
H	GPIO[6]	STRAP_RATE[0]	VDDIO	AVTT	VDD	VSS	VSS	VDD	AVDD10	VDDIO	TMS	RSTn
J	GPIO[7]	STRAP_RATE[1]	VDDIO	AVTT	AVTT	VSS	VSS	AVDD10	AVDD10	VSS	TRSTn	SRRSTOn
K	GPIO[8]	STRAP_RATE[2]	VSS	VSS	AVDD25	AVDD25	AVDD25	AVDD25	VSS	VSS	VSS	SRBIAS
L	I2C_SCL	CLKMOD	VSS	SRRN[0]	SRTN[0]	SRTN[1]	SRRN[1]	SRRN[2]	SRTN[2]	SRTN[3]	SRRN[3]	REFCLKN
M	I2C_SDA	MECS	SR_BOOT	SRRP[0]	SRTP[0]	SRTP[1]	SRRP[1]	SRRP[2]	SRTP[2]	SRTP[3]	SRRP[3]	REFCLKP

2.3 Pinlist

For a list-based version of Tsi721's pin to signal mapping, see the *Tsi721 Ballmap and Pinlist*.

2.4 PCIe Signals

Table 2: PCIe Signals

Name	Pin Type	Description
PCTP[3:0] PCTN[3:0]	PCIE_O	Differential transmit data for the PCIe port.
PCRP[3:0] PCRN[3:0]	PCIE_I	Differential receive data for the PCIe port.
PCCLKP PCCLKN	DIFF_I	PCIe reference clock input. When in PCIe common clock mode (CLKMOD pin is high, see the "Clocking" chapter in the Tsi721 User Manual), PCCLKP/N requires a clock frequency of 100 MHz. When in PCIe non-common clock mode (CLKMOD pin is low), PCCLKP/N requires a clock frequency as selected by CLKSEL[1:0], and must have the same clock frequency as REFCLKP/N.
PCRSTOn	IO	It is an output for normal operation and an input during scan test mode. As an asynchronous active-low reset output, this pin is low when the following occurs: • The PCIe port detects hot reset • The PCIe port is DL_DOWN

2.5 S-RIO Signals

Table 3: S-RIO Signals

Name	Pin Type	Description[a]
SRTP[3:0] SRTN[3:0]	SRIO_O	Differential transmit data for the S-RIO port.
SRRP[3:0] SRRN[3:0]	SRIO_I	Differential receive data for the S-RIO port.
SRRSTOn	IO	It is an output for normal operation and an input during scan test mode. As an asynchronous active-low reset output, this pin is low when four consecutive S-RIO reset symbols are received, and SELF_RST is set to 1 in the RapidIO PLM Port Implementation Specific Control Register
MECS	IO-PD	Asynchronous S-RIO Multicast Event Control Symbol (MECS). Its direction is controlled by the MECS_O bit in the Device Control Register. As an *input*, a rising or falling edge triggers an S-RIO MECS to be sent on the S-RIO link. Use the RIO_PLM_SP0_MECS_FWD.SUBSCRIPTION/MULT_CS and RIO_EM_MECS_TRIG_EN.CMD_EN to select the CMD field that should be set with the MECS. Multiple MECSs with different CMD fields can be generated by setting these fields appropriately. As an *output*, this signal is toggled when an S-RIO MECS is received. Only a single MECS CMD value should be selected to toggle the MECS input. Set the RIO_EM_MECS_CAP_EN.CMD_EN to select the CMD value to be propagated to the MECS pin. Note: Only 1 bit should be enabled in CMD_EN.

a. For information on S-RIO signals that are used for power-up purposes only, see Power-up Signals.

2.6 General Signals

Table 4: General Signals

Name	Pin Type	Description
RSTn	I-PU	Fundamental reset (device reset).Assertion of this signal resets all logic inside the Tsi721.
REFCLKP REFCLKN	DIFF_I	S-RIO reference clock input. REFCLK requires a clock frequency as selected by CLKSEL[1:0].

2.7 I2C Signals

The I2C Interface is used for the following:

- As a master, downloading configuration from EEPROM
- As a master, allowing the PCIe root complex or the S-RIO host to configure other I2C expansion devices
- As a slave, exposing internal register space to an I2C master (Note: To be used for lab debug or another master-driven initialization).

Table 5: I^2C Signals

Name	Pin Type	Description[a]
I2C_SCL	IO-OD	Serial clock for the I2C Interface with a maximum frequency of 100 kHz.
I2C_SDA	IO-OD	Serial data for the I2C Interface.

a. For information on I2C signals that are used for power-up purposes only, see Power-up Signals.

2.8 JTAG and Test Interface Signals

Table 6: JTAG Interface Signals

Name	Pin Type	Description
TCK	I-PD	IEEE 1149.1/1149.6 test access port. Clock input.
TDI	I-PU	IEEE 1149.1/1149.6 test access port. Serial data input
TDO	O	IEEE 1149.1/1149.6 test access port. Serial data output
TMS	I-PU	IEEE 1149.1/1149.6 test access port. Test mode select
TRSTn	I-PU	IEEE 1149.1/1149.6 test access port. Reset input. This input must be asserted during the assertion of RSTn. Thereafter, it can be left in either state.
TEST_ON	I-PD	Test mode pin. Tie low or NC for normal operation.
TEST_BCE	I-PU	Boundary scan compatibility enabled pin. This input aids 1149.6 testing. It must be tied to VDDIO (or NC as there is internal pull up in pad) during normal operation of the device. 0 = JTAG chain includes SerDes registers. SerDes registers are accessible to external JTAG pins. Used during ATE and lab debug of SerDes registers through an external JTAG Controller. 1 = JTAG chain does not include SerDes registers. SerDes register are accessible through the internal register bus for BAR 0 access.
TEST_BIDIR_CTL	I-PU	Test mode pin. Tie high or NC for normal operation.

2.9 GPIO Signals

Table 7: GPIO Signals

Name	Pin Type	Description
GPIO[15:0]	IO	Asynchronous general purpose I/O. • Each GPIO pin can be configured as a general purpose I/O pin. • Each pin can be configured as either an input or an output • When configured as an output, GPIO[0] is asserted high when BDMA/SMSG/PC2SR/SR2PC has an uncorrectable ECC error or S-RIO MAC has a non-data memory uncorrectable ECC error • When configured as an output, GPIO[1] is asserted high when Tsi721 PCIe port is not in the data link active state • When configured as an output, GPIO[2] is asserted high when Tsi721 has an active interrupt (for more information, see Figure 18 and Figure 19) • When configured as an output, GPIO[15:3] can be programmed through software GPIO[12:0] are used as power-up pins as displayed in Table 8. These signals must remain stable for 4000 REFCLKP/REFCLKN cycles after RSTn is de-asserted. They are ignored after reset.

Table 8: GPIO Mapping to Power-up Signals

GPIO Pin Name (Primary Function)	Power-up Pin Name[a] (Secondary Function)
GPIO[3:0]	I2C_SA[3:0]
GPIO[4]	I2C_DISABLE
GPIO[5]	I2C_SEL
GPIO[6]	I2C_MA
GPIO[7]	SP_SWAP_RX
GPIO[8]	SP_SWAP_TX
GPIO[9]	SP_HOST
GPIO[10]	SP_DEVID
GPIO[12:11]	CLKSEL[1:0]

a. For more information about these signals, see Power-up Signals.

2.10 Power-up Signals

Table 9: Power-Up Signals

Name	Pin Type	Description
CLKMOD	I-PU	Clock mode. When high, Tsi721 uses “PCIe common clocked mode.” When low, it uses “PCIe non-common clocked mode.” It is a static signal.
CLKSEL[1:0]	IO	REFCLKP/REFCLKN clock frequency select; PCCLKP/PCCLKN clock frequency select when in PCIe non-common clock mode. • 0b11 = 125 MHz • 0b10 = 100 MHz • 0b01 = 156.25 MHz • Others = Reserved When a 100-MHz clock is used, S-RIO SerDes rates of 1.25/2.5/5 Gbaud are supported. When a 125/156.25-MHz clock is used, S-RIO SerDes rates of 1.25/2.5/3.125/5 Gbaud are supported. When either a 100/125/156.25-MHz clock is used, PCIe SerDes rates of 2.5/5 Gbaud are supported. These power-up signals are multiplexed with GPIO[12:11]. It is a static signal.
I2C_DISABLE	IO	Disable I^2C register loading after reset. When asserted, Tsi721 does not attempt to load register values from an EEPROM over the I^2C bus. 0 = Enable boot load from EEPROM 1 = Disable boot load from EEPROM This power-up signal is multiplexed with GPIO[4]. It is a static signal.
I2C_MA	IO	I^2C multi-byte address mode. If I2C_DISABLE == 0 (that is, download registers from EEPROM) then: 0 = Tsi721 uses 1-byte addressing for EEPROM 1 = Tsi721 uses 2-byte addressing for EEPROM Else I2C_DISABLE == 1 (do not download from EEPROM) • 0 = Tsi721 is boot loaded by the PCIe root complex after reset • 1 = Tsi721 is boot loaded by an external I2C master after reset This power-up signal is multiplexed with GPIO[6]. It is a static signal.
I2C_SA[3:0]	IO	I2C slave address. The values on these pins represent the values for the 7-bit address of the Tsi721 when acting as an I^2C slave. These signals, in combination with the I2C_SEL signal, determine the address of the EEPROM to boot from (see I2C_SEL pin description). The values on these pins can be overridden after a reset by writing to the I2C Slave Configuration Register. These power-up signals are multiplexed with GPIO[3:0]. It is a static signal.

Table 9: Power-Up Signals (Continued)

Name	Pin Type	Description
I2C_SEL	IO	I^2C pin select. Combined with the I2C_SA[1,0] pins, Tsi721 will determine the lower 2 bits of the 7-bit address of the EEPROM address it boots from. When asserted, the I2C_SA[1:0] pins represent the two LSBs of the 7-bit EEPROM slave address when Tsi721 acts as a I^2C master downloading from an EEPROM. The EEPROM slave address is as follows: A6 = 1 A5 = 0 A4 = 1 A3 = 0 A2 = 0 A1 = I2C_SA[1] A0 = I2C_SA[0] When de-asserted, the I2C_SA[1:0] pins are ignored and the lower two bits of the EEPROM address default to 00. The values of the EEPROM address can be overridden by software after initialization. This power-up signal is multiplexed with GPIO[5]. It is a static signal.
SP_DEVID	IO	S-RIO base deviceID control When the SP_HOST pin is high, it configures the reset value of the RapidIO Base deviceID CSR: the LSB of the CSR's BASE_ID and LAR_BASE_ID fields are set to SP_DEVID, while other bits of these fields are set to 0. When the SP_HOST pin is low and SP_DEVID is high, it configures the reset value of the RapidIO Base deviceID CSR: the CSR's BASE_ID and LAR_BASE_ID fields are set to all ones. When the SP_HOST pin is low and SP_DEVID is low, it configures the reset value of the RapidIO Base deviceID CSR: the CSR's BASE_ID field is set to 0xFE and the CSR's LAR_BASE_ID field are set to 0x00FE. This signal is multiplexed with GPIO[10]. It is a static signal.
SP_HOST	IO	S-RIO host / slave control. This signal sets the reset value of the HOST bit of the RapidIO Port General Control CSR. 0 = Tsi721 is an S-RIO slave. 1 = Tsi721 is an S-RIO host. This signal is multiplexed with GPIO[9]. It is a static signal.
SP_SWAP_RX	IO	S-RIO receive lane swap. This signal sets the reset value of the SWAP_RX[1:0] bits of RapidIO PLM Port Implementation Specific Control Register. 0 = Disable S-RIO port receive lane swap; that is, set the SWAP_RX[1:0] register bits to 0b00. 1 = Enable S-RIO port receive 4x lane swap; that is, set the SWAP_RX[1:0] register bits to 0b10. This signal is multiplexed with GPIO[7].

Table 9: Power-Up Signals (Continued)

Name	Pin Type	Description
SP_SWAP_TX	IO	S-RIO transmit lane swap. This signal sets the reset value of the SWAP_TX bit of RapidIO PLM Port Implementation Specific Control Register. 0 = Disable S-RIO port transmit lane swap. 1 = Enable S-RIO port transmit lane swap. This signal is multiplexed with GPIO[8]. It is a static signal.
SR_BOOT	I-PD	Boot from S-RIO. It can be asserted high only when I2C_DISABLE is also high. 1 = The Tsi721 S-RIO link can start training immediately after a fundamental reset and Tsi721 automatically sets the SRBOOT_CMPL bit of Device Control Register. 0 = The Tsi721 S-RIO link can start training only after software sets the SRBOOT_CMPL bit. It is a static signal.
STRAP_RATE[2:0]	I-PU	S-RIO link rate. These signals control the reset value of the BAUD_SEL field of the RapidIO Port Control 2 CSR . Note that the BAUD_SEL encoding is different than that of STRAP_RATE. • 0b111 = 5 Gbaud • 0b110 = 2.5 Gbaud • 0b101 = 1.25 Gbaud • 0b010 = 3.125 Gbaud • Others: Reserved It is a static signal.