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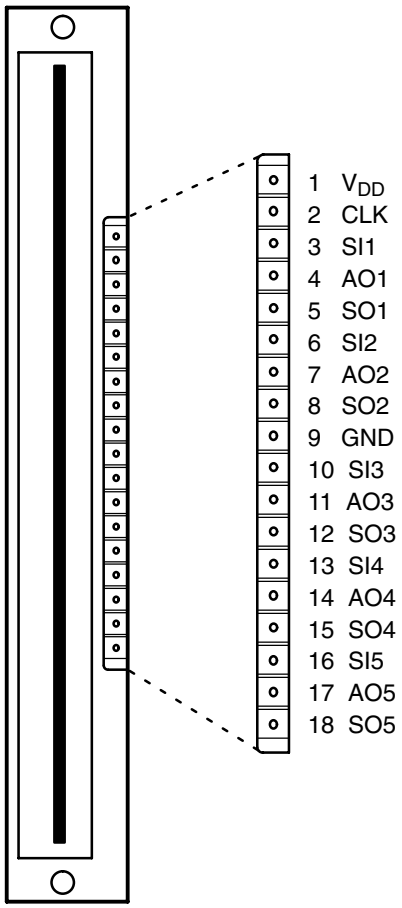
- **640 × 1 Sensor-Element Organization**
- **200 Dots-Per-Inch (DPI) Sensor Pitch**
- **High Linearity and Uniformity**
- **Wide Dynamic Range . . . 2000:1 (66 dB)**
- **Output Referenced to Ground**
- **Low Image Lag . . . 0.5% Typ**
- **Operation to 5 MHz**
- **Single 5-V Supply**

PACKAGE
(TOP VIEW)

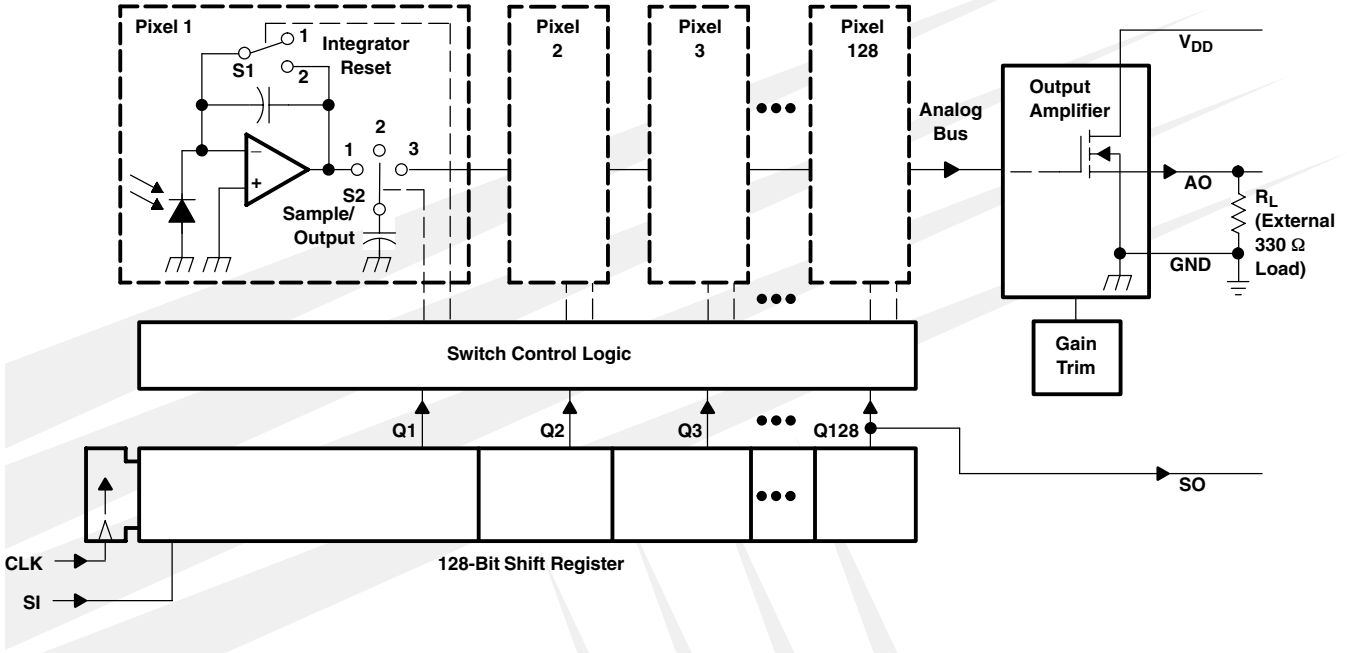


Description

The TSL210 linear sensor array consists of five sections of 128 photodiodes, each with associated charge amplifier circuitry, running from a common clock. These sections can be connected to form a contiguous 640 × 1 pixel array. Device pixels measure 120 µm (H) by 70 µm (W) with 125-µm center-to-center pixel spacing. Operation is simplified by internal logic that requires only a serial input (SI1 through SI5) for each section and a common clock for the five sections.

The device is intended for use in a wide variety of applications including contact imaging, mark and code reading, bar-code reading, edge detection and positioning, OCR, level detection, and linear and rotational encoding.

Functional Block Diagram (each section)



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Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AO1	4	O	Analog output of section 1.
AO2	7	O	Analog output of section 2.
AO3	11	O	Analog output of section 3.
AO4	14	O	Analog output of section 4.
AO5	17	O	Analog output of section 5.
CLK	2	I	Clock input for all sections. The clock controls the charge transfer, pixel output, and reset.
GND	9		Ground (substrate). All voltages are referenced to the substrate.
SI1	3	I	SI1 defines the start of the data out sequence for section 1.
SI2	6	I	SI2 defines the start of the data out sequence for section 2.
SI3	10	I	SI3 defines the start of the data out sequence for section 3.
SI4	13	I	SI4 defines the start of the data out sequence for section 4.
SI5	16	I	SI5 defines the start of the data out sequence for section 5.
SO1	5	O	SO1 provides the signal to drive the SI2 input in serial mode or *end of data* for section 1 in parallel mode.
SO2	8	O	SO2 provides the signal to drive the SI3 input in serial mode or *end of data* for section 2 in parallel mode.
SO3	12	O	SO3 provides the signal to drive the SI4 input in serial mode or *end of data* for section 3 in parallel mode.
SO4	15	O	SO4 provides the signal to drive the SI5 input in serial mode or *end of data* for section 4 in parallel mode.
SO5	18	O	SO5 provides the signal to drive the SI input of another device for cascading or as an *end of data* indication.
VDD	1		Supply voltage for both analog and digital circuits.

Detailed Description

The device consists of five sections of 128 photodiodes (called pixels — 640 total in the device) arranged in a linear array. Each section has its own signal input and output lines, and all five sections are connected to a common clock line. Light energy impinging on a pixel generates photocurrent that is then integrated by the active integration circuitry associated with that pixel.

During the integration period, a sampling capacitor connects to the output of the integrator through an analog switch. The amount of charge accumulated at each pixel is directly proportional to the light intensity on that pixel and the integration time. The voltage output developed for each pixel is according to the following relationship:

$$V_{out} = V_{drk} + (R_e)\ (E_e)\ (t_{int})$$

where:

- V_{out} is the analog output voltage for white condition
- V_{drk} is the analog output voltage for dark condition
- R_e is the device responsivity for a given wavelength of light given in V/(μJ/cm^2)
- E_e is the incident irradiance in μW/cm^2
- t_{int} is integration time in seconds

The output and reset of the integrators in each section are controlled by a 128-bit shift register and reset logic. An output cycle is initiated by clocking in a logic 1 on SI. As the SI pulse is clocked through the shift register, the charge stored on the sampling capacitors of each pixel is sequentially connected to a charge-coupled output amplifier that generates a voltage on analog output AO (given above). After being read, the pixel integrator is then reset, and the next integration period begins for that pixel. On the 129th clock rising edge, the SO pulse is clocked out on SO signifying the end of the read cycle. The section is then ready for another read cycle. The SO of each section can be connected to SI on the next section in the array (Figure 4). SO can be used to signify the read is complete.

AO is driven by a source follower that requires an external pulldown resistor (330-Ω typical). The output is nominally 0 V for no light input, 2 V for normal white-level, and 3.4 V for saturation light level. When the device is not in the output phase, AO is in a high impedance state.

A 0.1 μF bypass capacitor should be connected between V_{DD} and ground as close as possible to the device.

Absolute Maximum Ratings†

Supply voltage range, V_{DD} . . . . . –0.3 V to 6 V
Input voltage range, V_I . . . . . –0.3 V to V_{DD} + 0.3V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) . . . . . –20 mA to 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) . . . . . –25 mA to 25 mA
Voltage range applied to any output in the high impedance or
power-off state, V_O . . . . . –0.3 V to V_{DD} + 0.3V
Continuous output current, I_O (V_O = 0 to V_{DD}) . . . . . –25 mA to 25 mA
Continuous current through V_{DD} or GND . . . . . –100 mA to 100 mA
Analog output current range, I_O . . . . . –25 mA to 25 mA
Operating free-air temperature range, T_A . . . . . –25°C to 85°C
Storage temperature range, T_{stg} . . . . . –25°C to 85°C
Lead temperature on connection pad for 10 seconds . . . . . 260°C
ESD tolerance, human body model . . . . . 2000 V

† Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions (see Figure 1 and Figure 2)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5	5	5.5	V
Input voltage, V_I	0		V_{DD}	V
High-level input voltage, V_{IH}	2		V_{DD}	V
Low-level input voltage, V_{IL}	0		0.8	V
Wavelength of light source, λ	400		1000	nm
Clock frequency, f_{clock}	5		5000	kHz
Sensor integration time, serial, t_{int}	0.128		100	ms
Sensor integration time, parallel, t_{int}	0.026		100	ms
Load capacitance, C_L			330	pF
Load resistance, R_L	300		4700	Ω
Operating free-air temperature, T_A	0		70	°C

NOTE 1: SI must go low before the rising edge of the next clock pulse.

Electrical Characteristics at f_{clock} = 200 kHz, V_{DD} = 5 V, T_A = 25°C, λ_p = 640 nm, t_{int} = 5 ms, R_L = 330 Ω, E_e = 18μW/cm² (unless otherwise noted) (see Note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Analog output voltage (white, average over 640 pixels)	See Note 2	1.6	2	2.4	V
V_{DRK}	Analog output voltage (dark, average over 640 pixels)	E_e = 0	0	0.05	0.15	V
PRNU	Pixel response nonuniformity	See Note 4			±20	%
	Nonlinearity of analog output voltage	See Note 5		±0.4%		FS
	Output noise voltage	See Note 6		1		mVrms
R_e	Responsivity		16	22	28	V/(μJ/cm²)
SE	Saturation exposure	See Note 7		155		nJ/cm²
V_{SAT}	Analog output saturation voltage		2.5	3.4		V
DSNU	Dark signal nonuniformity	All pixels, E_e = 0, See Note 8		0.04	0.12	V
IL	Image lag	See Note 9		0.5		%
I_{DD}	Supply current			37	50	mA
I_{IH}	High-level input current	$V_I = V_{DD}$			10	μA
I_{IL}	Low-level input current	V_I = 0			10	μA
V_{OH}	High-level output voltage, SO1 – SO5	I_O = 50 μA	4.5	4.95		V
		I_O = 4 mA		4.6		
V_{OL}	Low-level output voltage, SO1 – SO5	I_O = 50 μA		0.01	0.1	V
		I_O = 4 mA		0.4		
$C_{i(SI)}$	Input capacitance, SI			20		pF
$C_{i(CLK)}$	Input capacitance, CLK			50		pF

NOTES: 2. The array is uniformly illuminated with a diffused LED source having a peak wavelength of 640 nm.
3. Clock duty cycle is assumed to be 50%.
4. PRNU is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test when the array is uniformly illuminated.
5. Nonlinearity is defined as the maximum deviation from a best-fit straight line over the dark-to-white irradiance levels, as a percent of analog output voltage (white).
6. RMS noise is the standard deviation of a single-pixel output under constant illumination as observed over a 5-second period.
7. Minimum saturation exposure is calculated using the minimum V_{sat}, the maximum V_{drk}, and the maximum R_e.
8. DSNU is the difference between the maximum and minimum output voltage in the absence of illumination.
9. Image lag is a residual signal left in a pixel from a previous exposure. It is defined as a percent of white-level signal remaining after a pixel is exposed to a white condition followed by a dark condition:

$$IL = \frac{V_{out\ (IL)} - V_{drk}}{V_{out\ (white)} - V_{drk}} \times 100$$

Timing Requirements (see Figure 1 and Figure 2)

		MIN	NOM	MAX	UNIT
$t_{su(SI)}$	Setup time, serial input (see Note 10)	20			ns
$t_{h(SI)}$	Hold time, serial input (see Note 10 and Note 11)	0			ns
t_w	Pulse duration, clock high or low	50			ns
t_r, t_f	Input transition (rise and fall) time	0		500	ns

NOTES: 10. Input pulses have the following characteristics: t_r = 6 ns, t_f = 6 ns.
11. SI must go low before the rising edge of the next clock pulse.

Dynamic Characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_s	Analog output settling time to ±1%	C_L = 10 pF		185		ns

TYPICAL CHARACTERISTICS

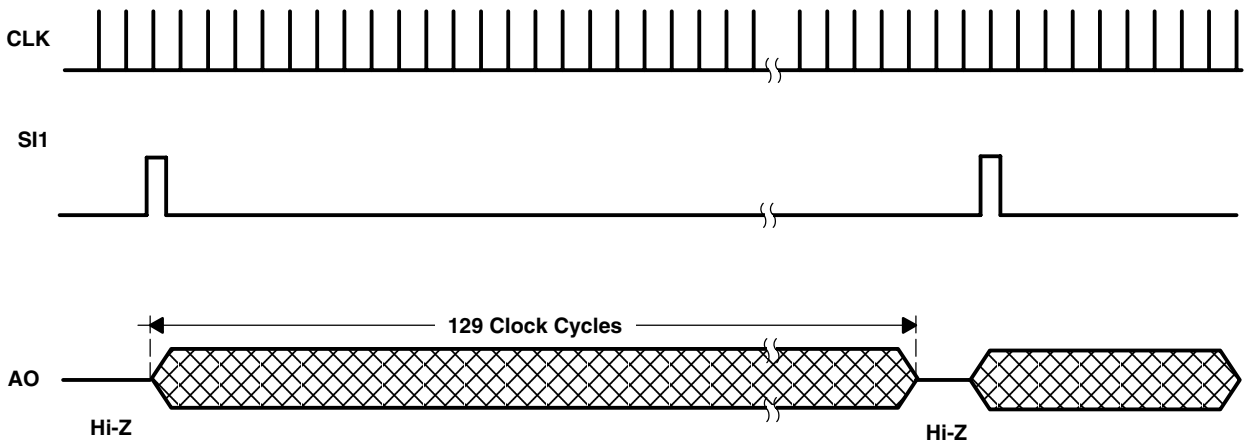


Figure 1. Timing Waveforms (each section)

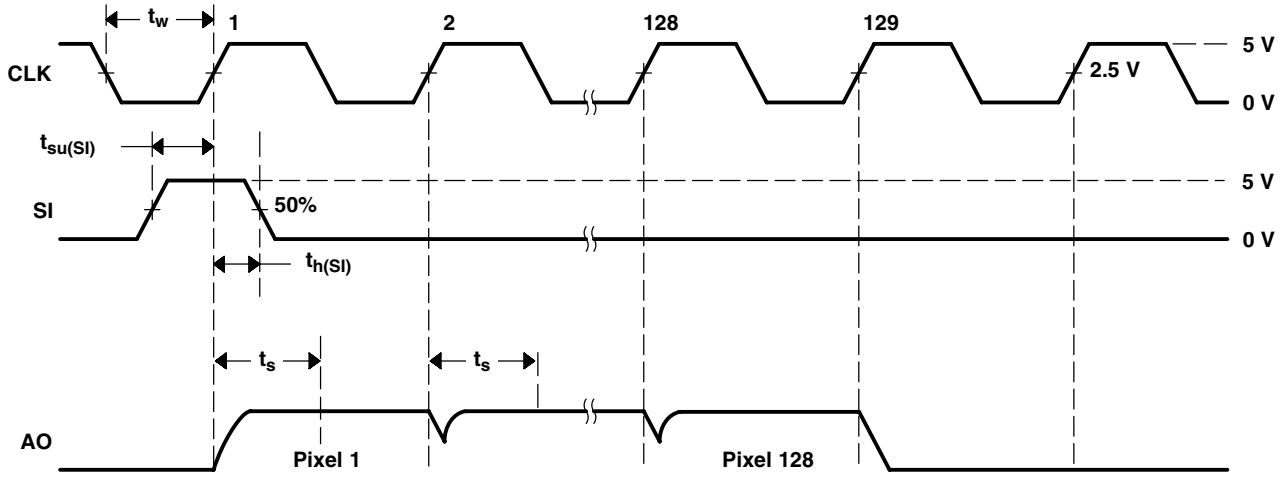


Figure 2. Operational Waveforms (each section)

TYPICAL CHARACTERISTICS

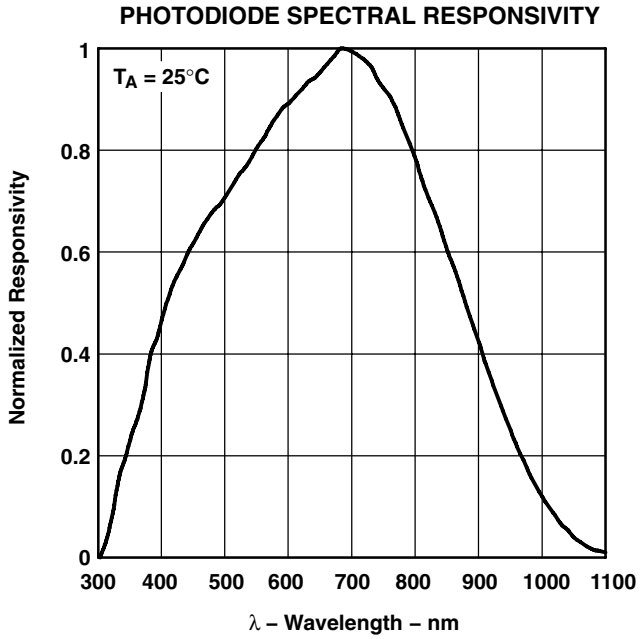


Figure 3

APPLICATION INFORMATION

Integration Time

The integration time of the linear array is the period during which light is sampled and charge accumulates on each pixel's integrating capacitor. The flexibility to adjust the integration period is a powerful and useful feature of the TAOS TSL2xx linear array family. By changing the integration time, a desired output voltage can be obtained on the output pin while avoiding saturation for a wide range of light levels.

Each pixel of the linear array consists of a light-sensitive photodiode. The photodiode converts light intensity to a voltage. The voltage is sampled on the Sampling Capacitor by closing switch S2 (position 1) (see the functional block diagram on page 1). Logic controls the resetting of the Integrating Capacitor to zero by closing switch S1 (position 2).

At SI input (Start Integration), pixel 1 is accessed. During this event, S2 moves from position 1 (sampling) to position 3 (holding). This holds the sampled voltage for pixel 1. Switch S1 for pixel 1 is then moved to position 2. This resets (clears) the voltage previously integrated for that pixel so that pixel 1 is now ready to start a new integration cycle. When the next clock period starts, the S1 switch is returned to position 1 to be ready to start integrating again. S2 is returned to position 1 to start sampling the next light integration. Then the next pixel starts the same procedure. The integration time is the time from a specific pixel read to the next time that pixel is read again. If either the clock speed or the time between successive SI pulses is changed, the integration time will vary. After the final (n^{th}) pixel in the array is read on the output, the output goes into a high-impedance mode. A new SI pulse can occur on the (n+1) clock causing a new cycle of integration/output to begin. Note that the time between successive SI pulses must not exceed the maximum integration time of 100 msec.

The minimum integration time for any given array is determined by time required to clock out all the pixels in the array and the time to discharge the pixels. The time required to discharge the pixels is a constant. Therefore, the minimum integration period is simply a function of the clock frequency and the number of pixels in the array. A slower clock speed increases the minimum integration time and reduces the maximum light level for saturation on the output. The minimum integration time shown in this data sheet is based on the maximum clock frequency of 5 MHz.

The minimum integration time can be calculated from the equation:

$$T_{int(min)} = \left(\frac{1}{maximum\ clock\ frequency}\right) \times n$$

where:

n is the number of pixels

In the case of the TSL210, the minimum integration time would be:

$$T_{int(min)} = 200ns \times 640 = 128\mu s$$

It is important to note that not all pixels will have the same integration time if the clock frequency is varied while data is being output.

APPLICATION INFORMATION

It is good practice on initial power up to run the clock (*n*+1) times after the first SI pulse to clock out indeterminate data from power up. After that, the SI pulse is valid from the time following (*n*+1) clocks. The output will go into a high-impedance state after the *n*+1 high clock edge. It is good practice to leave the clock in a low state when inactive because the SI pulse required to start a new cycle is a low-to-high transition.

The integration time chosen is valid as long as it falls in the range between the minimum and maximum limits for integration time. If the amount of light incident on the array during a given integration period produces a saturated output (Max Voltage output), then the data is not accurate. If this occurs, the integration period should be reduced until the analog output voltage for each pixel falls below the saturation level. The goal of reducing the period of time the light sampling window is active is to lower the output voltage level to prevent saturation. However, the integration time must still be greater than or equal to the minimum integration period.

If the light intensity produces an output below desired signal levels, the output voltage level can be increased by increasing the integration period provided that the maximum integration time is not exceeded. The maximum integration time is limited by the length of time the integrating capacitors on the pixels can hold their accumulated charge. The maximum integration time should not exceed 100 ms for accurate measurements.

Although the linear array is capable of running over a wide range of operating frequencies up to a maximum of 5 MHz, the speed of the A/D converter used in the application is likely to be the limiter for the maximum clock frequency. The voltage output is available for the whole period of the clock, so the setup and hold times required for the analog-to-digital conversion must be less than the clock period.

APPLICATION INFORMATION

Connection Diagrams

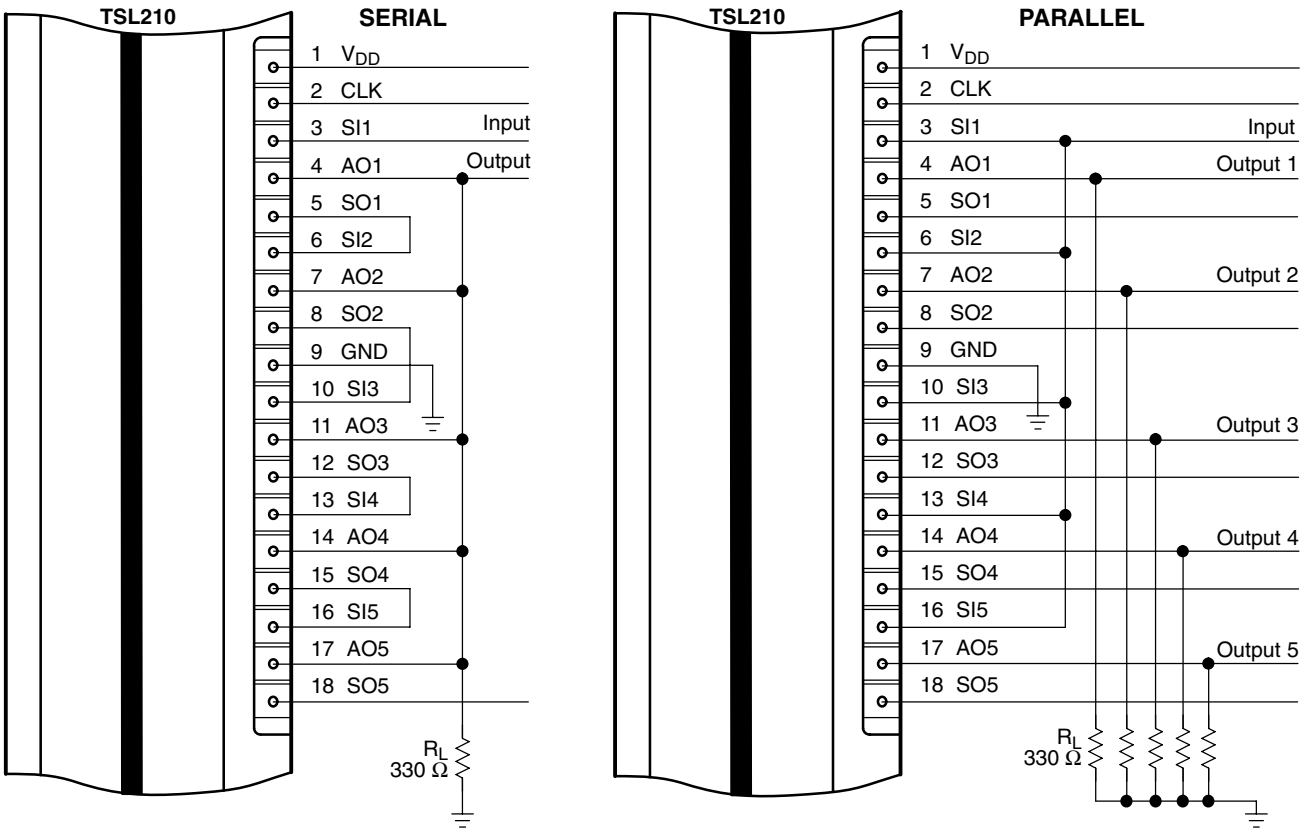
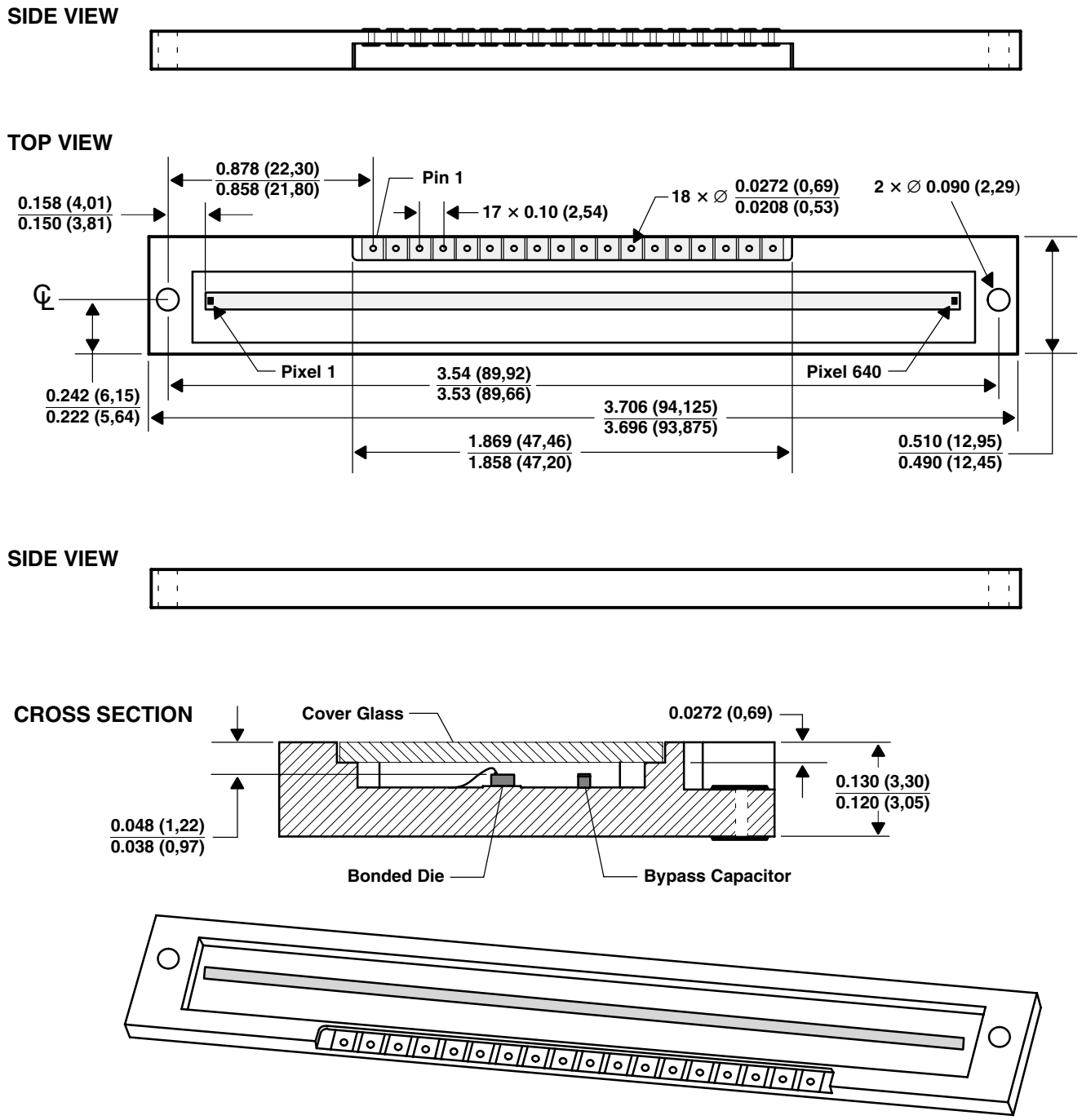


Figure 4. Connection Diagrams

MECHANICAL INFORMATION



NOTES: A. All linear dimensions are in inches (millimeters).
B. Pixel centers are located along the center line of the mounting holes.
C. Cover glass index of refraction is 1.52.
D. This drawing is subject to change without notice.

Figure 5. TSL210 Mechanical Specifications

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