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TSL2568, TSL2569

Light-to-Digital Converter

General Description

The TSL2568 and TSL2569 are high-sensitivity light-to-digital converters that transform light intensity to a digital signal output capable of direct I^2C (TSL2569) or SMBus (TSL2568) interface. Each device combines one broadband photodiode (visible plus infrared) and one infrared-responding photodiode on a single CMOS integrated circuit capable of providing a near-photopic response over an effective 20-bit dynamic range (16-bit resolution). Two integrating ADCs convert the photodiode currents to a digital output that represents the irradiance measured on each channel. This digital output can be input to a microprocessor where illuminance (ambient light level) in lux is derived using an empirical formula to approximate the human eye response. The TSL2568 device permits an SMB-Alert style interrupt, and the TSL2569 device supports a traditional level style interrupt that remains asserted until the firmware clears it.

While useful for general purpose light sensing applications, the TSL2568/69 devices are designed particularly for display panels (LCD, OLED, etc.) with the purpose of extending battery life and providing optimum viewing in diverse lighting conditions. Display panel backlighting, which can account for up to 30 to 40 percent of total platform power, can be automatically managed. Both devices are also ideal for controlling keyboard illumination based upon ambient lighting conditions. Illuminance information can further be used to manage exposure control in digital cameras. The TSL2568/69 devices are ideal in notebook/tablet PCs, LCD monitors, flat-panel televisions, cell phones, and digital cameras. In addition, other applications include street light control, security lighting, sunlight harvesting, machine vision, and automotive instrumentation clusters.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TSL2568 and TSL2569, Light-to-Digital Converters, are listed below:

Figure 1:
Added Value of Using TSL2568 and TSL2569

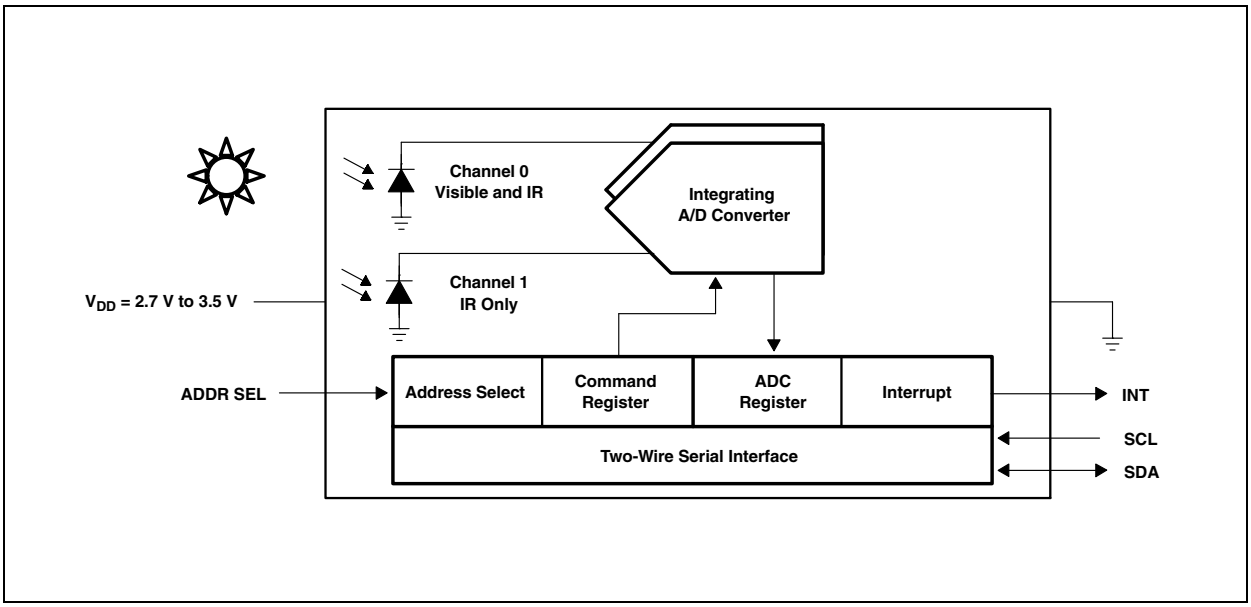
Benefits	Features
• Enables Operation in IR Light Environments	• Patented Dual-Diode Architecture
• Enables Dark Room to High Lux Sunlight Operation	• 1M:1 Dynamic Range
• Reduces Micro-Processor Interrupt Overhead	• Programmable Interrupt Function
• Digital Interface is Less Susceptible to Noise	• SMBus (TSL2568) and I^2C (TSL2569) Digital Interface
• Reduces Board Space Requirements while Simplifying Designs	• Available in 1.25mm x 1.75mm Chipscale or 2.6mm x 3.8mm TMB Packages

- Approximates human eye response
- Approximately 4× more sensitive than TSL2560/61 device
- Programmable interrupt function with user-defined upper and lower threshold settings
- 16-Bit digital output with SMBus (TSL2568) at 100kHz or
- I^2C (TSL2569) fast-mode at 400kHz
- Programmable analog gain and integration time supporting 1,000,000-to-1 dynamic range
- Available in ultra-small 1.25 mm × 1.75 mm chipscale package
- Automatically rejects 50/60Hz lighting ripple
- Low active power (0.75mW typical) with power down mode

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
TSL2568 and TSL2569 Block Diagram



Detailed Description

The TSL2568 and TSL2569 are second-generation ambient light sensor devices. Each contains two integrating analog-to-digital converters (ADC) that integrate currents from two photodiodes. Integration of both channels occurs simultaneously. Upon completion of the conversion cycle, the conversion result is transferred to the Channel 0 and Channel 1 data registers, respectively. The transfers are double-buffered to ensure that the integrity of the data is maintained. After the transfer, the device automatically begins the next integration cycle.

Communication to the device is accomplished through a standard, two-wire SMBus or I^2C serial bus. Consequently, the TSL256x device can be easily connected to a microcontroller or embedded controller. No external circuitry is required for signal conditioning, thereby saving PCB real estate as well. Since the output of the TSL256x device is digital, the output is effectively immune to noise when compared to an analog signal.

The TSL256x devices also support an interrupt feature that simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity value. The primary purpose of the interrupt function is to detect a meaningful change in light intensity. The concept of a *meaningful change* can be defined by the user both in terms of light intensity and time, or persistence, of that change in intensity. The TSL256x devices have the ability to define a threshold above and below the current light level. An interrupt is generated when the value of a conversion exceeds either of these limits.

Pin Assignments

The TSL2568 and TSL2569 pin assignments are described below:

Figure 3:
Pin Diagram of Package CS 6-Lead Chipscale (Top View)

Package drawings are not to scale

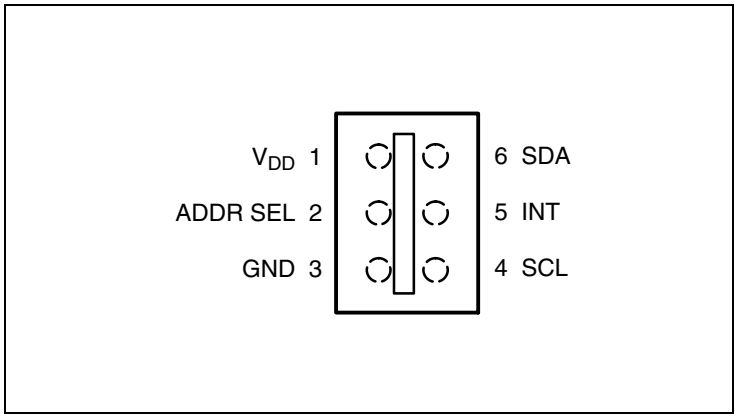


Figure 4:
Pin Diagram of Package T 6-Lead TMB (Top View)

Package drawings are not to scale

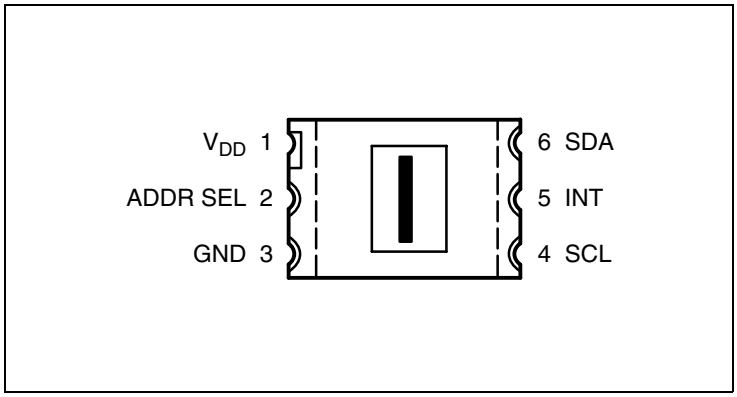


Figure 5:
Terminal Functions

Terminal		Type	Description
Name	T Pkg No.		
V_{DD}	1		Supply voltage
ADDR SEL	2	I	SMBus device select - three-state
GND	3		Power supply ground. All voltages are referenced to GND.
SCL	4	I	SMBus serial clock input terminal - clock signal for SMBus serial data
INT	5	O	Level or SMB Alert interrupt - open drain
SDA	6	I/O	SMBus serial data I/O terminal - serial data I/O for SMBus

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings over Operating Free-Air Temperature Range (unless otherwise noted)

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage (1)		3.8	V
V_O	Digital output voltage range	-0.5	3.8	V
I_O	Digital output current	-1	20	mA
T_{strg}	Storage temperature range	-40	85	°C
ESD	ESD tolerance, human body model	±2000		V

Note(s):

1. All voltages are with respect to GND.

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 7:
Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Unit
V_{DD}	Supply voltage	2.7	3	3.6	V
T_A	Operating free-air temperature	-30		70	°C
V_{IL}	SCL, SDA input low voltage	-0.5		0.8	V
V_{IH}	SCL, SDA input high voltage	2.1		3.6	V

Figure 8:
Electrical Characteristics over Recommended Operating Free-Air Temperature Range (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Active		0.24	0.6	mA
		Power down		3.2	15	µA
V_{OL}	INT, SDA output low voltage	3mA sink current	0		0.4	V
I_{LEAK}	Leakage current		-5		5	µA

Figure 9:
Operating Characteristics, High Gain (16×), V_{DD} = 3V, T_A = 25°C (unless otherwise noted) (1), (2), (3), (4)

Symbol	Parameter	Test Conditions	Channel	TSL2568T, TSL2569T			TSL2568CS, TSL2569CS			Unit
				Min	Typ	Max	Min	Typ	Max	
f_{OSC}	Oscillator frequency			690	735	780	690	735	780	kHz
	Dark ADC count value	E_e = 0, T_{int} = 402ms	Ch0	0		8	0		8	counts
			Ch1	0		8	0		8	
	Full scale ADC count value (5)	T_{int} > 178ms	Ch0			65535			65535	counts
			Ch1			65535			65535	
		T_{int} = 101ms	Ch0			37177			37177	
			Ch1			37177			37177	
		T_{int} = 13.7ms	Ch0			5047			5047	
			Ch1			5047			5047	

Symbol	Parameter	Test Conditions	Channel	TSL2568T, TSL2569T			TSL2568CS, TSL2569CS			Unit
				Min	Typ	Max	Min	Typ	Max	
	ADC count value	λ_p = 640nm, T_{int} = 101ms E_e = 33µW/cm^2	Ch0	3000	4000	5000				counts
			Ch1		1000					
		λ_p = 940nm, T_{int} = 101ms E_e = 106µW/cm^2	Ch0	2800	4000	5200				
			Ch1		3520					
		λ_p = 640nm, T_{int} = 101ms E_e = 34.5µW/cm^2	Ch0				3000	4000	5000	counts
			Ch1					840		
		λ_p = 940nm, T_{int} = 101ms E_e = 110.9µW/cm^2	Ch0				2800	4000	5200	
			Ch1					3440		
	ADC count value ratio: Ch1/Ch0	λ_p = 640nm, T_{int} = 101ms		0.18	0.25	0.32	0.14	0.21	0.28	
		λ_p = 940nm, T_{int} = 101ms		0.73	0.88	1.03	0.70	0.86	1.01	
R_e	Irradiance responsivity	λ_p = 640nm, T_{int} = 101ms	Ch0		121			116		counts/ (µW/cm^2)
			Ch1		30.3			24		
		λ_p = 940nm, T_{int} = 101ms	Ch0		37.7			36		
			Ch1		33.2			31		
R_v	Illuminance responsivity	Fluorescent light source: T_{int} = 402ms	Ch0		185			180		counts/lux
			Ch1		35			33.3		
		Incandescent light source: T_{int} = 402ms	Ch0		599			537		
			Ch1		330			307		

Symbol	Parameter	Test Conditions	Channel	TSL2568T, TSL2569T			TSL2568CS, TSL2569CS			Unit
				Min	Typ	Max	Min	Typ	Max	
	ADC count value ratio: Ch1/Ch0	Fluorescent light source: T_{int} = 402ms			0.19			0.19		
		Incandescent light source: T_{int} = 402ms			0.55			0.57		
R_V	Illuminance responsivity, low gain mode (6)	Fluorescent light source: T_{int} = 402ms	Ch0		11.6			11.1		counts/lux
			Ch1		2.2			2.1		
		Incandescent light source: T_{int} = 402ms	Ch0		37.5			33.8		
			Ch1		20.7			19.3		
	(Sensor Lux)/(actual Lux), high gain mode (7)	Fluorescent light source: T_{int} = 402ms		0.65	1	1.35	0.65	1	1.35	
		Incandescent light source: T_{int} = 402ms		0.60	1	1.40	0.60	1	1.40	

Note(s):

1. Optical measurements are made using small-angle incident radiation from light-emitting diode optical sources. Visible 640nm LEDs and infrared 940nm LEDs are used for final product testing for compatibility with high-volume production.
2. The 640nm irradiance E_e is supplied by an AlInGaP light-emitting diode with the following characteristics: peak wavelength λ_p = 640nm and spectral halfwidth $\Delta\lambda$½ = 17nm.
3. The 940nm irradiance E_e is supplied by a GaAs light-emitting diode with the following characteristics: peak wavelength λ_p = 940nm and spectral halfwidth $\Delta\lambda$½ = 40nm.
4. Integration time T_{int}, is dependent on internal oscillator frequency (f_{osc}) and on the integration field value in the Timing Register as described in the *Register Set* section. For nominal f_{osc} = 735kHz, nominal T_{int} = (number of clock cycles)/f_{osc}.
   Field value 00: $T_{int} = (11 \times 918)/f_{osc}$ = 13.7ms
   Field value 01: $T_{int} = (81 \times 918)/f_{osc}$ = 101ms
   Field value 10: $T_{int} = (322 \times 918)/f_{osc}$ = 402ms
   Scaling between integration times vary proportionally as follows: 11/322 = 0.034 (field value 00), 81/322 = 0.252 (field value 01), and 322/322 = 1 (field value 10).

5. Full scale ADC count value is limited by the fact that there is a maximum of one count per two oscillator frequency periods and also by a 2-count offset.
   Full scale ADC count value = ((number of clock cycles)/2 − 2)
   Field value 00: Full scale ADC count value = ((11 × 918)/2 − 2) = 5047
   Field value 01: Full scale ADC count value = ((81 × 918)/2 − 2) = 37177
   Field value 10: Full scale ADC count value = 65535, which is limited by 16-bit register. This full scale ADC count value is reached for 131074 clock cycles, which occurs for T_{int} = 178ms for nominal f_{osc} = 735kHz.
6. Low gain mode has 16× lower gain than high gain mode: (1/16 = 0.0625).
7. The sensor Lux is calculated using the empirical formula shown in "Calculating Lux" on page 35 of this data sheet based on measured Ch0 and Ch1 ADC count values for the light source specified. Actual Lux is obtained with a commercial luxmeter. The range of the (sensor Lux) / (actual Lux) ratio is estimated based on the variation of the 640nm and 940nm optical parameters. Devices are not 100% tested with fluorescent or incandescent light sources.

Figure 10:
AC Electrical Characteristics, V_{DD} = 3V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter (1)	Test Conditions	Min	Typ	Max	Unit
$t_{(CONV)}$	Conversion time		12	100	400	ms
$f_{(SCL)}$	Clock frequency (I^2C only)		0		400	kHz
	Clock frequency (SMBus only)		10		100	kHz
$t_{(BUF)}$	Bus free time between start and stop condition		1.3			µs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.		0.6			µs
$t_{(SUSTA)}$	Repeated start condition setup time		0.6			µs
$t_{(SUSTO)}$	Stop condition setup time		0.6			µs
$t_{(HDDAT)}$	Data hold time		0		0.9	µs
$t_{(SUDAT)}$	Data setup time		100			ns
$t_{(LOW)}$	SCL clock low period		1.3			µs
$t_{(HIGH)}$	SCL clock high period		0.6			µs
$t_{(TIMEOUT)}$	Detect clock/data low timeout (SMBus only)		25		35	ms
t_F	Clock/data fall time				300	ns
t_R	Clock/data rise time				300	ns
C_i	Input pin capacitance				10	pF

Note(s):

1. Specified by design and characterization; not production tested.

Figure 11:
Timing Diagrams

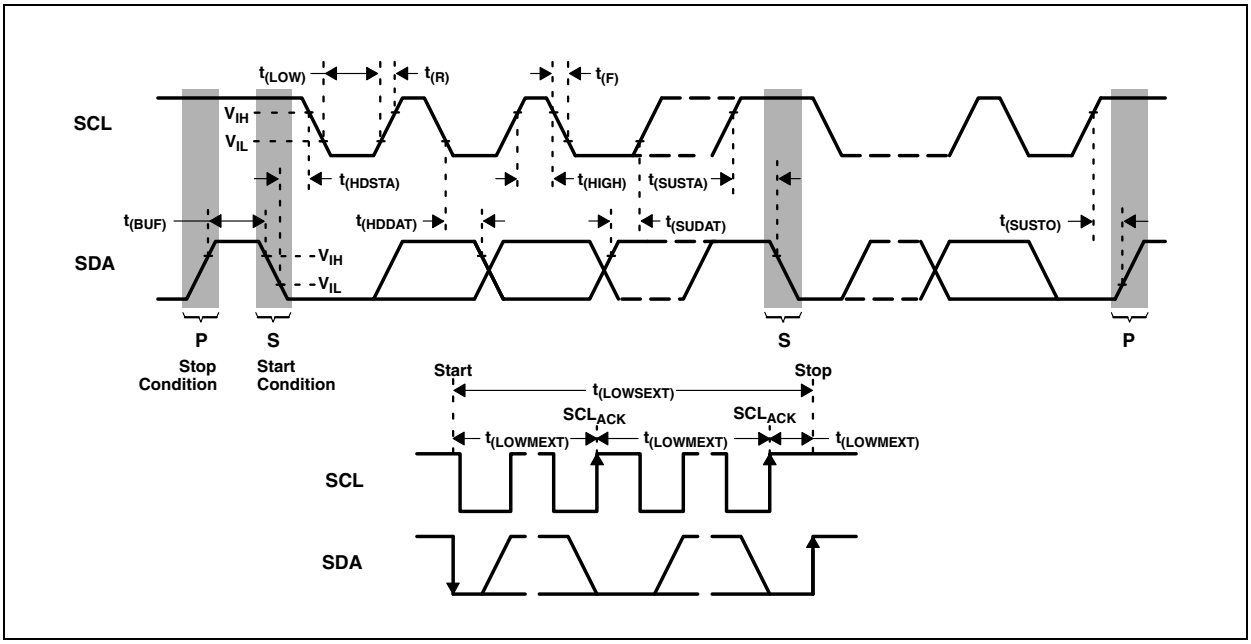


Figure 12:
Example Timing Diagram for SMBus Send Byte Format

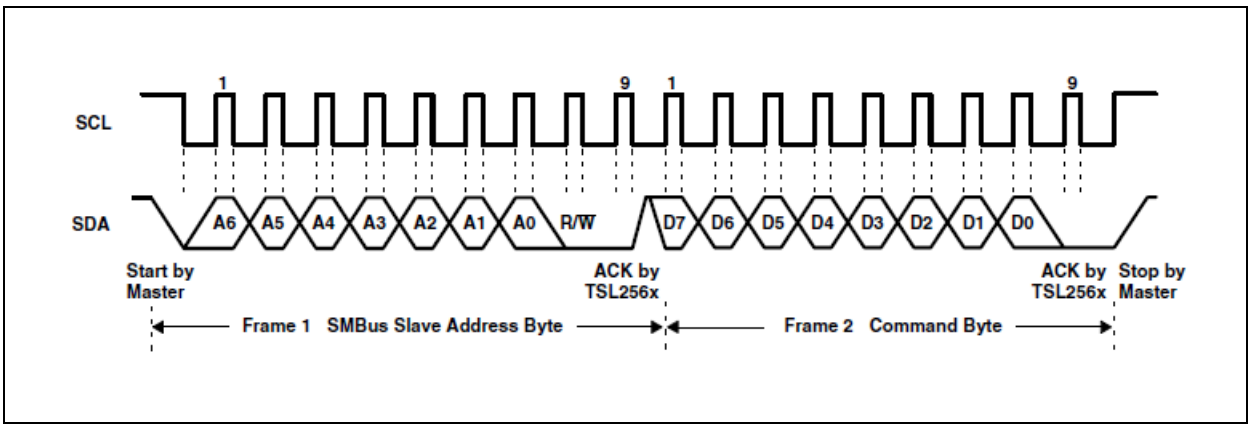
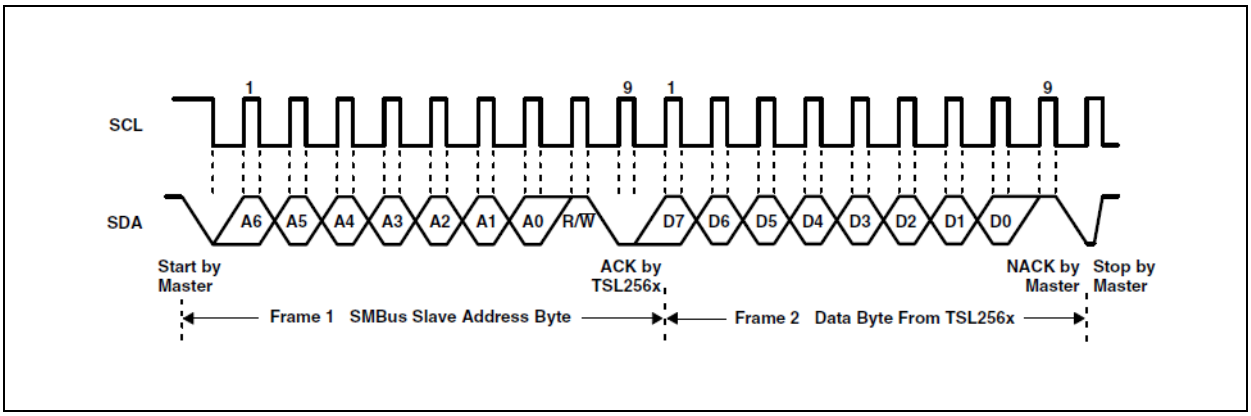


Figure 13:
Example Timing Diagram for SMBus Receive Byte Format



Typical Characteristics

Figure 14:
Spectral Responsivity

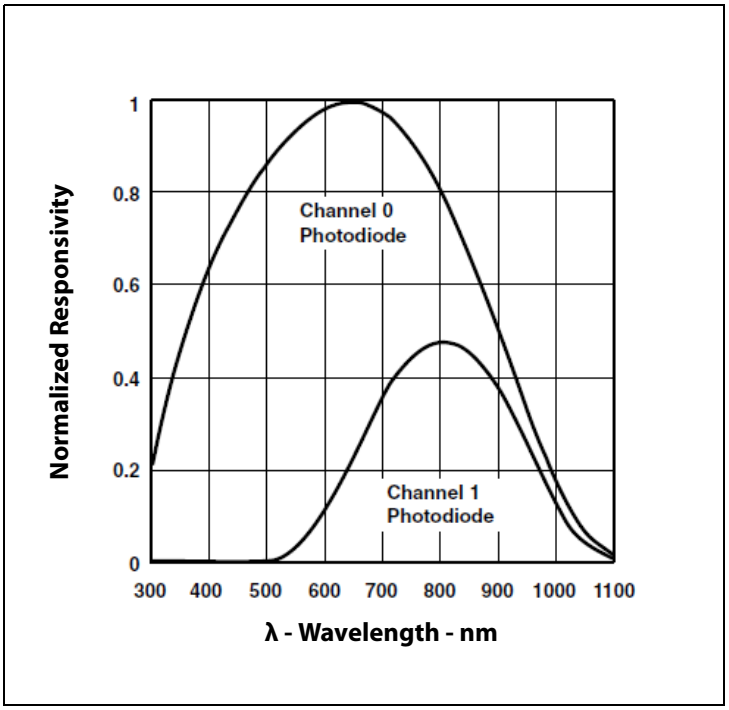


Figure 15:
Normalized Responsivity vs. Angular Displacement - CS Package

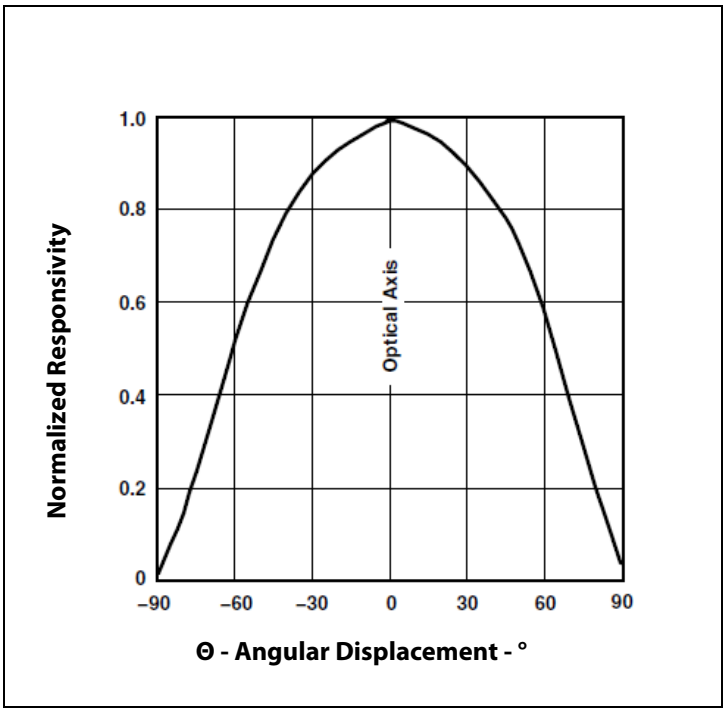
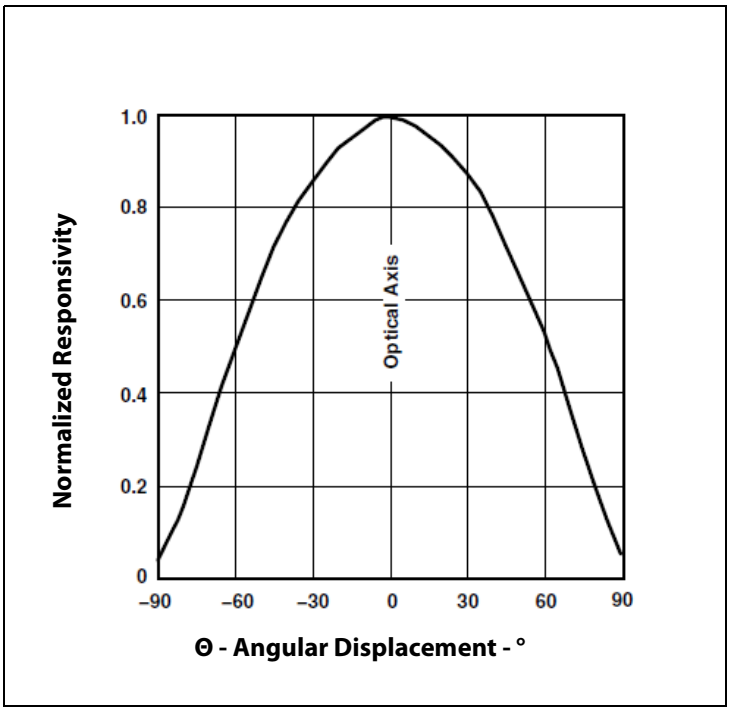


Figure 16:
Normalized Responsivity vs. Angular Displacement - TMB Package



Principles of Operation

Analog-to-Digital Converter

The TSL256x contains two integrating analog-to-digital converters (ADC) that integrate the currents from the channel 0 and channel 1 photodiodes. Integration of both channels occurs simultaneously, and upon completion of the conversion cycle the conversion result is transferred to the channel 0 and channel 1 data registers, respectively. The transfers are double buffered to ensure that invalid data is not read during the transfer. After the transfer, the device automatically begins the next integration cycle.

Digital Interface

Interface and control of the TSL256x is accomplished through a two-wire serial interface to a set of registers that provide access to device control functions and output data. The serial interface is compatible with System Management Bus (SMBus) versions 1.1 and 2.0, and I^2C bus Fast-Mode. The TSL256x offers three slave addresses that are selectable via an external pin (ADDR SEL). The slave address options are shown in Figure 17.

Figure 17:
Slave Address Selection

ADDR SEL Terminal Level	Slave Address	SMB Alert Address
GND	0101001	0001100
Float	0111001	0001100
V_{DD}	1001001	0001100

Note(s):

1. The Slave and SMB Alert Addresses are 7 bits. Please note the SMBus and I^2C protocols (see SMBus and I^2C Protocols). A read/write bit should be appended to the slave address by the master device to properly communicate with the TSL256X device.

SMBus and I²C Protocols

Each *Send* and *Write* protocol is, essentially, a series of bytes. A byte sent to the TSL256x with the most significant bit (MSB) equal to 1 will be interpreted as a COMMAND byte. The lower four bits of the COMMAND byte form the register select address (see Figure 27), which is used to select the destination for the subsequent byte(s) received. The TSL256x responds to any Receive Byte requests with the contents of the register specified by the stored register select address.

The TSL256X implements the following protocols of the SMB 2.0 specification:

- Send Byte Protocol
- Receive Byte Protocol
- Write Byte Protocol
- Write Word Protocol
- Read Word Protocol
- Block Write Protocol
- Block Read Protocol

The TSL256X implements the following protocols of the Philips Semiconductor I²C specification:

- I²C Write Protocol
- I²C Read (Combined Format) Protocol

When an SMBus Block Write or Block Read is initiated (see description of Command Register), the byte following the COMMAND byte is ignored but is a requirement of the SMBus specification. This field contains the byte count (i.e. the number of bytes to be transferred). The TSL2568 (SMBus) device ignores this field and extracts this information by counting the actual number of bytes transferred before the Stop condition is detected.

When an I²C Write or I²C Read (Combined Format) is initiated, the byte count is also ignored but follows the SMBus protocol specification. Data bytes continue to be transferred from the TSL2569 (I²C) device to Master until a NACK is sent by the Master.

The data formats supported by the TSL2568 and TSL2569 devices are:

- Master transmitter transmits to slave receiver (SMBus and I²C):
  - The transfer direction in this case is not changed.
- Master reads slave immediately after the first byte (SMBus only):
  - At the moment of the first acknowledgment (provided by the slave receiver) the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter.

- Combined format (SMBus and I²C):
  - During a change of direction within a transfer, the master repeats both a START condition and the slave address but with the R/W bit reversed. In this case, the master receiver terminates the transfer by generating a NACK on the last byte of the transfer and a STOP condition.

For a complete description of SMBus protocols, please review the SMBus Specification at www.smbus.org/specs. For a complete description of I²C protocols, please review the I²C Specification at www.nxp.com.

Figure 18:
SMBus and I²C Packet Protocol Element Key

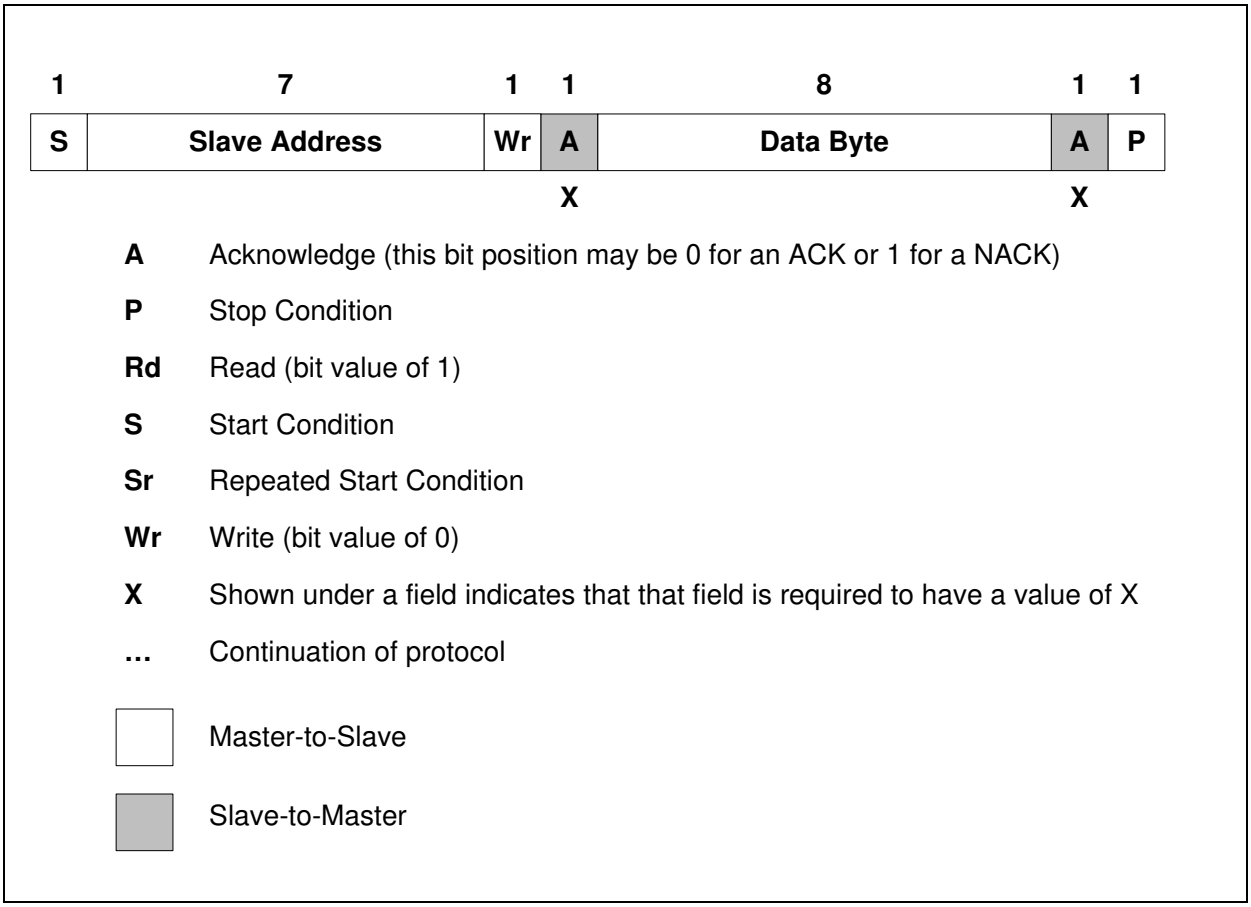


Figure 19:
SMBus Send Byte Protocol

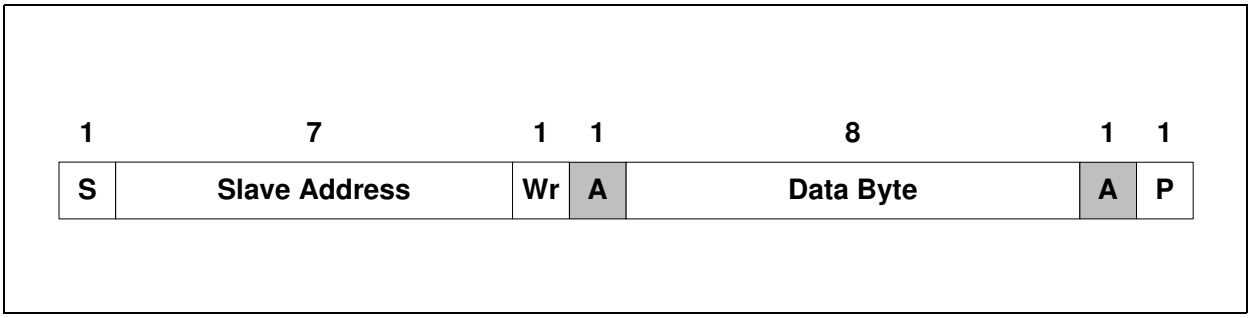


Figure 20:
SMBus Receive Byte Protocol

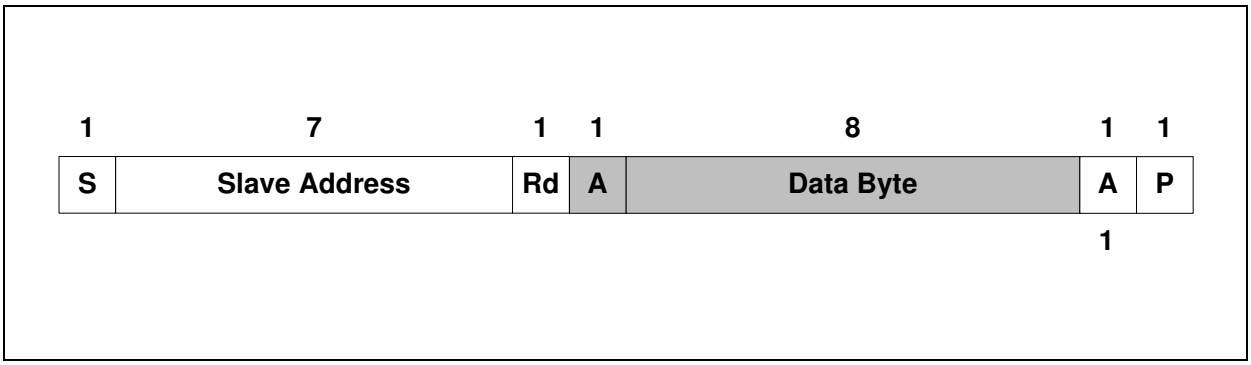


Figure 21:
SMBus Write Byte Protocol

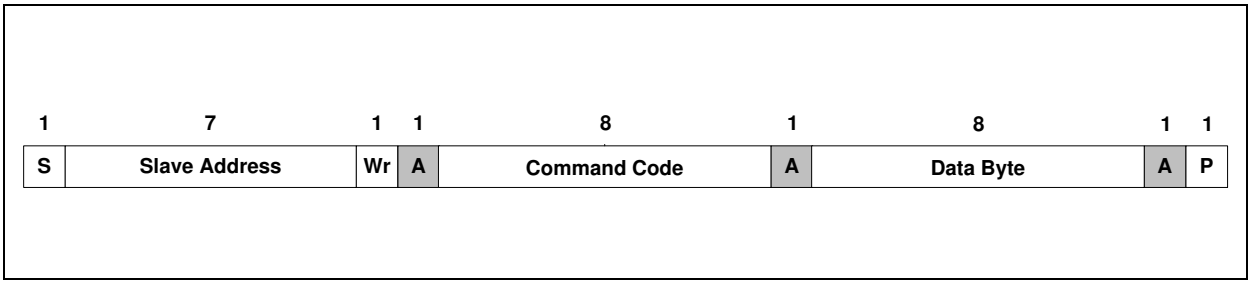


Figure 22:
SMBus Read Byte Protocol

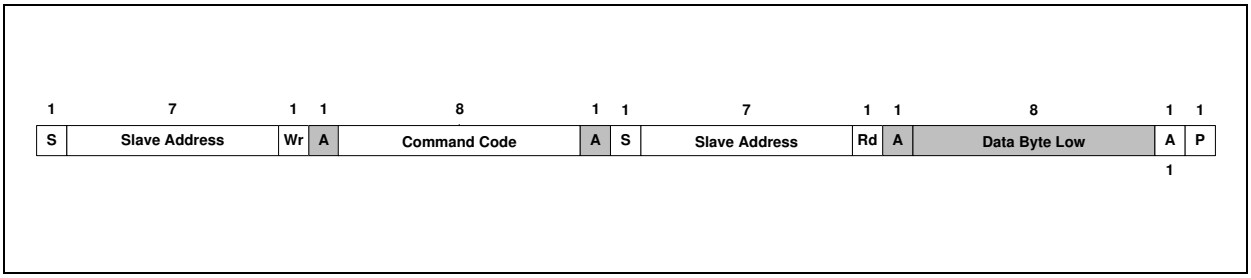


Figure 23:
SMBus Write Word Protocol

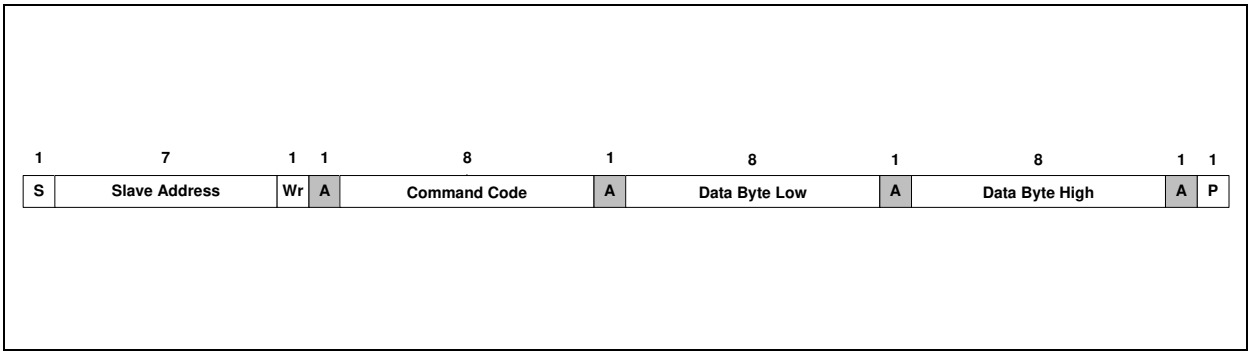


Figure 24:
SMBus Read Word Protocol

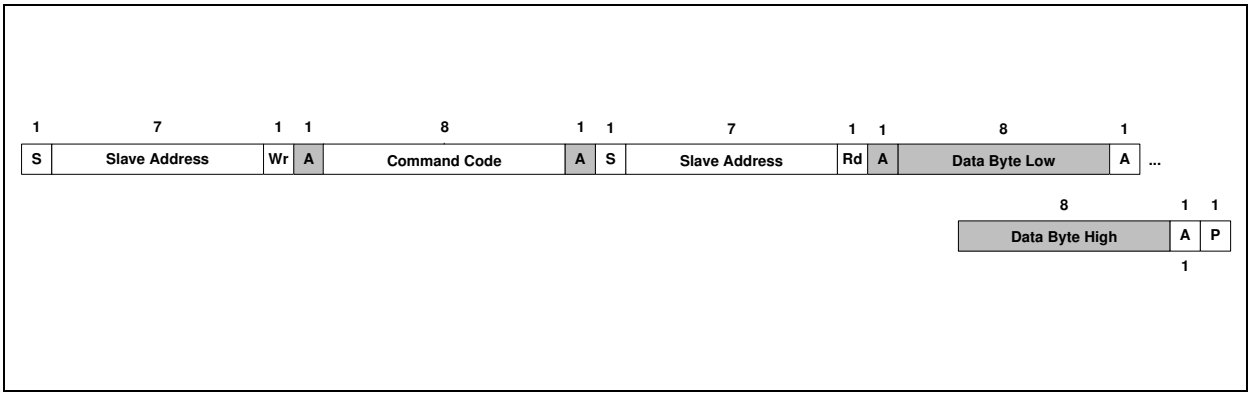
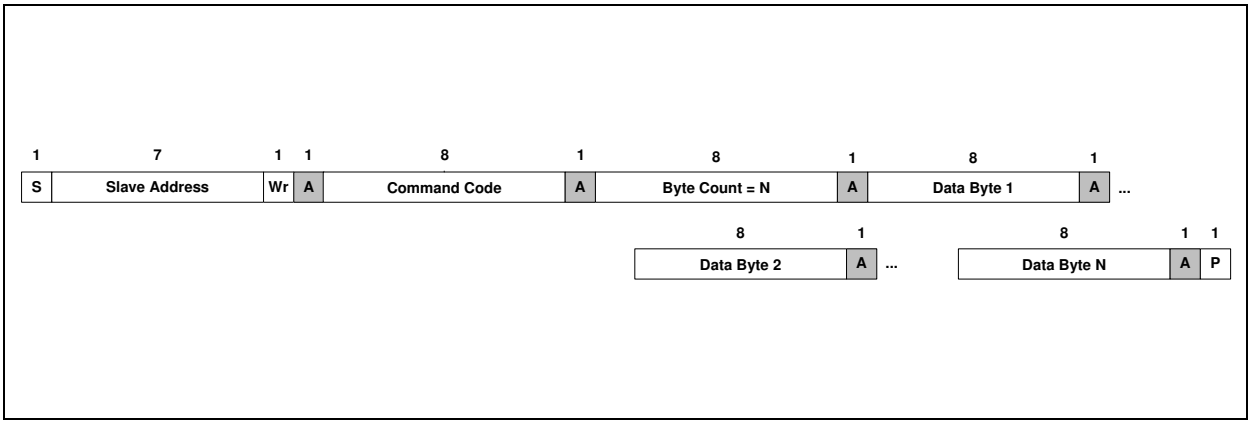


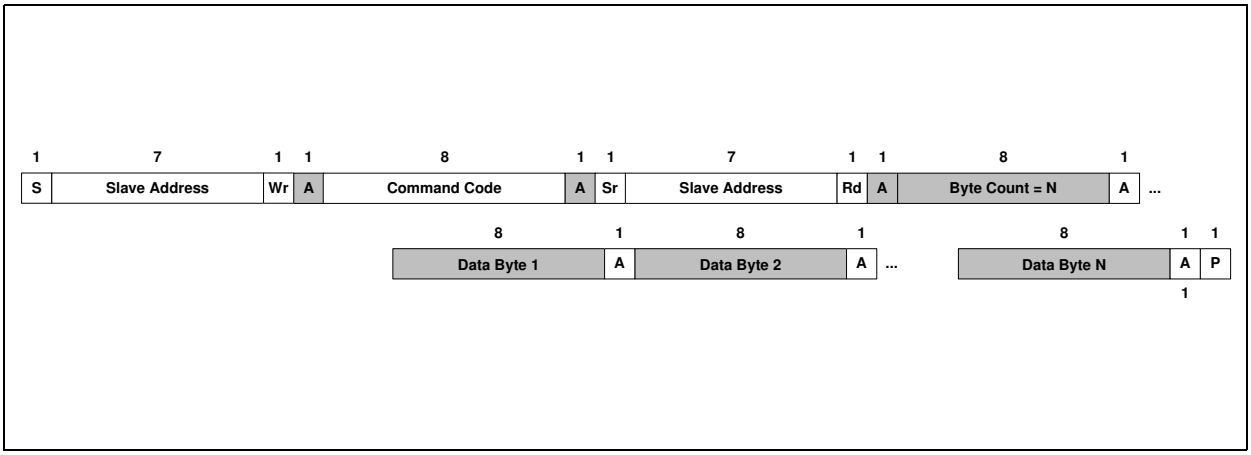
Figure 25:
SMBus Block Write or I²C Write Protocols



Note(s):

1. The I²C read protocol does not use the Byte Count packet, and the Master will continue receiving Data Bytes until the Master initiates a Stop Condition. See the Command Register for additional information regarding the Block Read/Write protocol.

Figure 26:
SMBus Block Read or I²C Read (Combined Format) Protocols



Note(s):

1. The I²C read protocol does not use the Byte Count packet, and the Master will continue receiving Data Bytes until the Master initiates a Stop Condition. See the Command Register for additional information regarding the Block Read/Write protocol.

Register Set

The TSL256x is controlled and monitored by sixteen registers (three are reserved) and a Command Register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The Register Set is summarized in Figure 27.

Figure 27:
Register Address

Address	Register Name	Register Function
--	COMMAND	Specifies register address
0h	CONTROL	Control of basic functions
1h	TIMING	Integration time/gain control
2h	THRESHLOWLOW	Low byte of low interrupt threshold
3h	THRESHLOWHIGH	High byte of low interrupt threshold
4h	THRESHHIGHLOW	Low byte of high interrupt threshold
5h	THRESHHIGHHIGH	High byte of high interrupt threshold
6h	INTERRUPT	Interrupt control
7h	--	Reserved
8h	CRC	Factory test - not a user register
9h	--	Reserved
Ah	ID	Part number/Rev ID
Bh	--	Reserved
Ch	DATA0LOW	Low byte of ADC channel 0
Dh	DATA0HIGH	High byte of ADC channel 0
Eh	DATA1LOW	Low byte of ADC channel 1
Fh	DATA1HIGH	High byte of ADC channel 1

The mechanics of accessing a specific register depends on the specific SMB protocol used. Refer to the section on SMBus protocols. In general, the Command Register is written first to specify the specific control/status register for following read/write operations.

Command Register

The Command Register specifies the address of the target register for subsequent read and write operations. The Send Byte protocol is used to configure the Command Register. The Command Register contains eight bits as described in Figure 28. The Command Register defaults to 00h at power on.

Figure 28:
Command Register

7	6	5	4	3	2	1	0
CMD	**CLEAR**	**WORD**	**BLOCK**	**ADDRESS**			

Field	Bit	Description
CMD	7	Select Command Register. Must write as 1.
CLEAR	6	Interrupt clear. Clears any pending interrupt. This bit is a write-one-to-clear bit. It is self clearing.
WORD	5	SMB Write/Read Word Protocol. 1 indicates that this SMB transaction is using either the SMB Write Word or Read Word protocol.
BLOCK	4	Block Write/Read Protocol. 1 indicates that this transaction is using either the Block Write or the Block Read protocol. (1)
ADDRESS	3:0	Register Address. This field selects the specific control or status register for following write and read commands according to Figure 27.

Note(s):

1. An I^2C block transaction will continue until the Master sends a stop condition. See Figure 25 and Figure 26. Unlike the I^2C protocol, the SMBus read/write protocol requires a Byte Count. All four ADC Channel Data Registers (Ch through Fh) can be read simultaneously in a single SMBus transaction. This is the only 32-bit data block supported by the TSL2568 SMBus protocol. The BLOCK bit must be set to 1, and a read condition should be initiated with a COMMAND CODE of 9Bh. By using a COMMAND CODE of 9Bh during an SMBus Block Read Protocol, the TSL2568 device will automatically insert the appropriate Byte Count (Byte Count = 4) as illustrated in Figure 26. A write condition should not be used in conjunction with the Bh register.

Control Register (0h)

The Control Register contains two bits and is primarily used to power the TSL256x device up and down as shown in Figure 29.

Figure 29:
Control Register

7	6	5	4	3	2	1	0
Resv	**Resv**	**Resv**	**Resv**	**Resv**	**Resv**	**POWER**	

Field	Bit	Description
Resv	7:2	Reserved. Write as 0.
POWER	1:0	Power up/power down. By writing a 03h to this register, the device is powered up. By writing a 00h to this register, the device is powered down.(1)

Note(s):

1. If a value of 03h is written, the value returned during a read cycle will be 03h. This feature can be used to verify that the device is communicating properly.

Timing Register (1h)

The Timing Register controls both the integration time and the gain of the ADC channels. A common set of control bits is provided that controls both ADC channels. The Timing Register defaults to 02h at power on.

Figure 30:
Timing Register

7	6	5	4	3	2	1	0
Resv			**GAIN**	**Manual**	**Resv**	**INTEG**	

Field	Bit	Description
Resv	7:5	Reserved. Write as 0.
GAIN	4	Switches gain between low gain and high gain modes. Writing a 0 selects low gain (1×); writing a 1 selects high gain (16×).
Manual	3	Manual timing control. Writing a 1 begins an integration cycle. Writing a 0 stops an integration cycle.(1)
Resv	2	Reserved. Write as 0.
INTEG	1:0	Integrate time. This field selects the integration time for each conversion.

Note(s):

1. This field only has meaning when INTEG = 11. It is ignored at all other times.

Integration time is dependent on the INTEG FIELD VALUE and the internal clock frequency. Nominal integration times and respective scaling between integration times scale proportionally as shown in Figure 31. See note 4 and note 5 for detailed information regarding how the scale values were obtained; see Calculating Lux and Simplified Lux Calculation for further information on how to calculate lux.

Figure 31:
Integration Time

INTEG Field Value	Scale	Nominal Integration Time
00	0.034	13.7ms
01	0.252	101ms
10	1	402ms
11	--	N/A

The manual timing control feature is used to manually start and stop the integration time period. If a particular integration time period is required that is not listed in Figure 31, then this feature can be used. For example, the manual timing control can be used to synchronize the TSL256x device with an external light source (e.g. LED). A start command to begin integration can be initiated by writing a 1 to this bit field. Correspondingly, the integration can be stopped by simply writing a 0 to the same bit field.