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TSL2571

Light-to-Digital Converter

General Description

The TSL2571 family of devices provides ambient light sensing (ALS) that approximates human eye response to light intensity under a variety of lighting conditions and through a variety of attenuation materials. While useful for general purpose light sensing, the device is particularly useful for display management with the purpose of extending battery life and providing optimum viewing in diverse lighting conditions. Display panel and keyboard backlighting can account for up to 30 to 40 percent of total platform power. The ALS features are ideal for use in notebook PCs, LCD monitors, flat-panel televisions, and cell phones.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TSL2571, Light-to-Digital Converter are listed below:

Figure 1:
Added Value Of Using TSL2571

Benefits	Features
• Enables Operation in IR Light Environments	• Patented Dual-Diode Architecture
• Enables Dark Room to High Lux Sunlight Operation	• 1M:1 Dynamic Range
• Digital Interface is Less Susceptible to Noise	• I^2C Digital Interface
• Enables Low Standby Power Consumption	• 2.5µA Quiescent Current (Sleep Mode)
• Reduces Board Space Requirements while Simplifying Designs	• Available in 2mm x 2mm Dual Flat No-Lead (FN) Packages

- Ambient Light Sensing (ALS)
  - Approximates Human Eye Response
  - Programmable Analog Gain
  - Programmable Integration Time
  - Programmable Interrupt Function with Upper and Lower Threshold
  - Resolution Up to 16 Bits
  - Very High Sensitivity — Operates Well Behind Darkened Glass
  - Up to 1,000,000:1 Dynamic Range

- Programmable Wait Timer
  - Programmable from 2.72 ms to > 8 Seconds
  - Wait State — 65μA Typical Current
- I²C Interface Compatible
  - Up to 400 kHz (I²C Fast Mode)
  - Dedicated Interrupt Pin
- Small 2 mm x 2 mm ODFN Package
- Sleep Mode — 2.5μA Typical Current

Applications

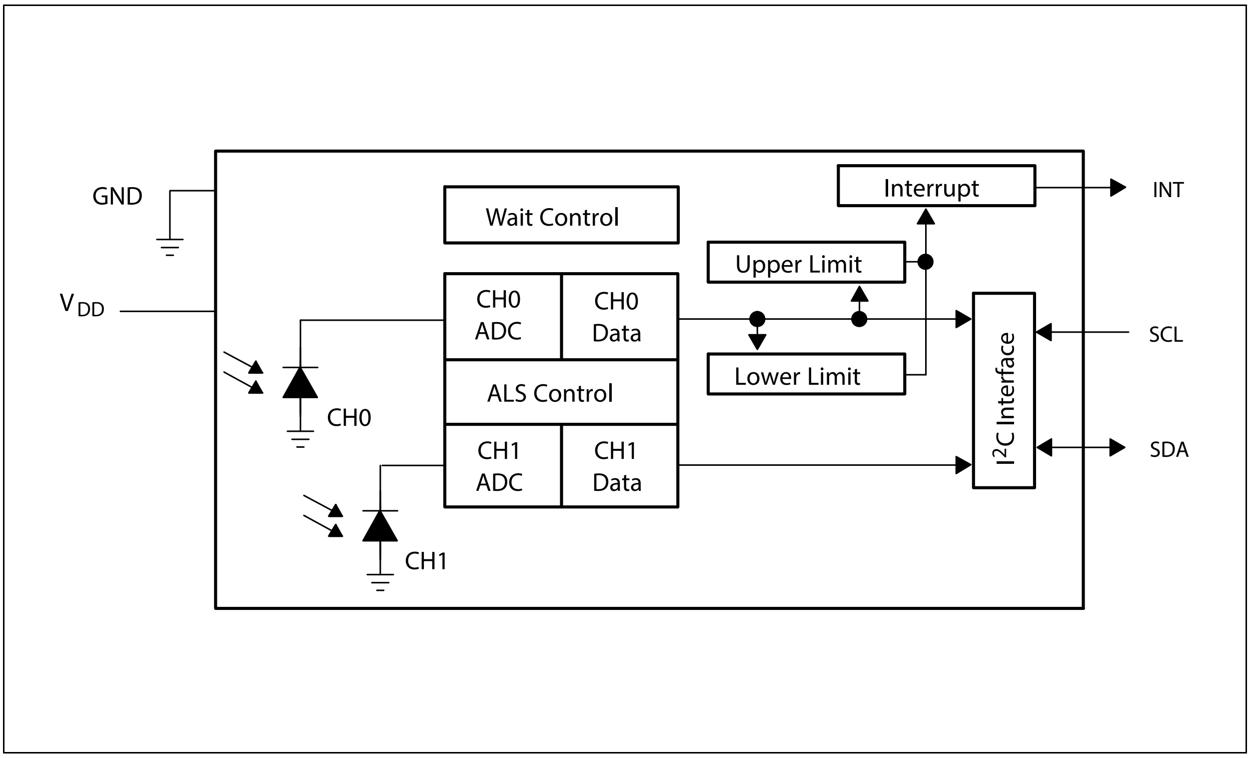
TSL2571, Light-to-Digital Converter is ideal for:

- Display Management
- Backlight Control
- Portable Device Power Optimization
- Cell Phones, PDA, GPS
- Notebooks and Monitors
- LCD TVs

Functional Block Diagram

The functional blocks of this device are shown below:

Figure 2:
TSL2571 Block Diagram



Pin Assignments

Figure 3:
Package FN Dual Flat No-Lead (Top View)

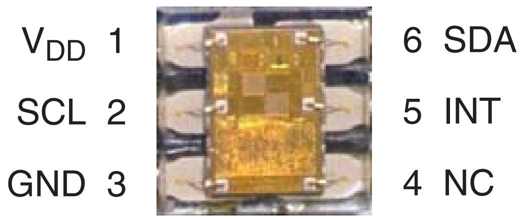


Figure 4:
Terminal Functions

Terminal		Type	Description
Name	No		
V_{DD}	1		Supply voltage.
SCL	2	I	I^2C serial clock input terminal — clock signal for I^2C serial data.
GND	3		Power supply ground. All voltages are referenced to GND.
NC	4		Do not connect.
INT	5	O	Interrupt — open drain (active low).
SDA	6	I/O	I^2C serial data I/O terminal — serial data I/O for I^2C .

Detailed Description

The TSL2571 light-to-digital device includes on-chip photodiodes, integrating amplifiers, ADCs, accumulators, clocks, buffers, comparators, a state machine, and an I^2C interface. The device combines one photodiode (CH0), which is responsive to both visible and infrared light, and one photodiode (CH1), which is responsive primarily to infrared light. Two integrating ADCs simultaneously convert the amplified photodiode currents into a digital value providing up to 16 bits of resolution. Upon completion of the conversion cycle, the conversion result is transferred to the data registers. This digital output can be read by a microprocessor through which the illuminance (ambient light level) in lux is derived using an empirical formula to approximate the human eye response.

Communication to the device is accomplished through a fast (up to 400 kHz), two-wire I^2C serial bus for easy connection to a microcontroller or embedded controller. The digital output of the device is inherently more immune to noise when compared to an analog interface.

The device provides a separate pin for level-style interrupts. When interrupts are enabled and a pre-set value is exceeded, the interrupt pin is asserted and remains asserted until cleared by the controlling firmware. The interrupt feature simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity value. An interrupt is generated when the value of an ALS conversion exceeds either an upper or lower threshold. In addition, a programmable interrupt persistence feature allows the user to determine how many consecutive exceeded thresholds are necessary to trigger an interrupt. Interrupt thresholds and persistence settings are configured independently.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)

Symbol	Parameter	Min	Max	Units
V_{DD} (1)	Supply voltage		3.8	V
V_O	Digital output voltage range	-0.5	3.8	V
I_O	Digital Output current	-1	+20	mA
T_{STRG}	Storage temperature range	-40	85	°C
ESD_{HBM}	ESD tolerance, human body model	±2000		V

Note(s):

1. All voltages are with respect to GND.

Electrical Characteristics

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Supply voltage	2.6	3	3.6	V
T_A	Operating free-air temperature	-30		70	°C

Figure 7:
Operating Characteristics; V_{DD} = 3V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Active		175	250	µA
		Wait mode		65		
		Sleep mode — no I^2C activity		2.5	4	
V_{OL}	INT SDA output low voltage	3 mA sink current	0		0.4	V
		6 mA sink current	0		0.6	
I_{LEAK}	Leakage current, SDA, SCL, INT pins		−5		5	µA
V_{IH}	SCL SDA input high voltage	TSL25711, TSL25715	0.7 V_{DD}			V
		TSL25713	1.25			
V_{IL}	SCL SDA input low voltage	TSL25711, TSL25715			0.3 V_{DD}	V
		TSL25713			0.54	

Figure 8:
ALS Characteristics; V_{DD} = 3V, T_A = 25°C, Gain = 16, AEN = 1 (unless otherwise noted)[1] [2] [3]

Parameter	Test Conditions	Channel	Min	Typ	Max	Unit
Dark ADC count value	E_e = 0, AGAIN = 120× ATIME = 0xDB (100 ms)	CH0	0	1	5	counts
		CH1	0	1	5	
ADC integration time step size	ATIME = 0xFF		2.58	2.72	2.9	ms
ADC Number of integration steps			1		256	steps
ADC counts per step	ATIME = 0xFF		0		1024	counts
ADC count value	ATIME = 0xC0		0		65535	counts
ADC count value	λ_p = 625 nm, E_e = 171.6 µW/cm^2 ATIME = 0xF6 (27 ms) [2]	CH0	4000	5000	6000	counts
		CH1		790		
	λ_p = 850 nm, E_e = 219.7 µW/cm^2 ATIME = 0xF6 (27 ms) [3]	CH0	4000	5000	6000	
		CH1		2800		
ADC count value ratio: CH1/CH0	λ_p = 625 ATIME 0xF6 (27 ms) [2]		10.8	15.8	20.8	%
	λ_p = 850 ATIME 0xF6 (27 ms) [3]		41	56	68	
R_e Irradiance responsivity	λ_p = 625 nm, ATIME = 0xF6 (27 ms) [2]	CH0		29.1		counts/ (µW/ cm^2)
		CH1		4.6		
	λ_p = 850 nm, ATIME = 0xF6 (27 ms) [3]	CH0		22.8		
		CH1		12.7		
Gain scaling, relative to 1× gain setting	8×		−10		10	%
	16×		−10		10	
	120×		−10		10	

Note(s):

1. Optical measurements are made using small-angle incident radiation from light-emitting diode optical sources. Visible 625 nm LEDs and infrared 850 nm LEDs are used for final product testing for compatibility with high-volume production.
2. The 625 nm irradiance E_e is supplied by an AlInGaP light-emitting diode with the following typical characteristics: peak wavelength λ_p = 625 nm and spectral halfwidth $\Delta\lambda½$ = 20 nm.
3. The 850 nm irradiance E_e is supplied by a GaAs light-emitting diode with the following typical characteristics: peak wavelength λ_p = 850 nm and spectral halfwidth $\Delta\lambda½$ = 42 nm.

Figure 9:
Wait Characteristics; V_{DD} = 3V, T_A = 25°C, WEN = 1 (unless otherwise noted)

Parameter	Test Conditions	Channel	Min	Typ	Max	Unit
Wait step size	WTIME = 0xFF		2.58	2.72	2.9	ms
Wait number of integration steps			1		256	steps

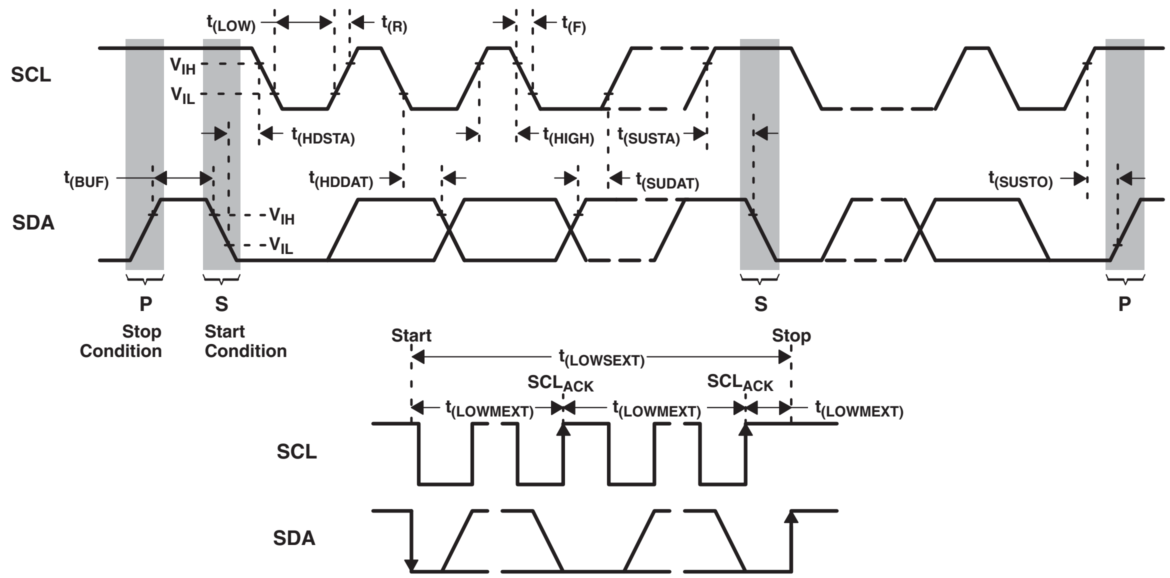
Figure 10:
AC Electrical Characteristics; V_{DD} = 3V, T_A = 25°C, (unless otherwise noted)

Symbol	Parameter[(1)]	Test Conditions	Min	Typ	Max	Unit
$f_{(SCL)}$	Clock frequency (I^2C only)		0		400	kHz
$t_{(BUF)}$	Bus free time between start and stop condition		1.3			μs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.		0.6			μs
$t_{(SUSTA)}$	Repeated start condition setup time		0.6			μs
$t_{(SUSTO)}$	Stop condition setup time		0.6			μs
$t_{(HDDAT)}$	Data hold time		0			μs
$t_{(SUDAT)}$	Data setup time		100			ns
$t_{(LOW)}$	SCL clock low period		1.3			μs
$t_{(HIGH)}$	SCL clock high period		0.6			μs
t_F	Clock/data fall time				300	ns
t_R	Clock/data rise time				300	ns
C_i	Input pin capacitance				10	pF

Note(s):

1. Specified by design and characterization; not production tested.

Figure 11:
Timing Diagrams - Parameter Measurement Information



Typical Characteristics

Figure 12:
Spectral Responsivity

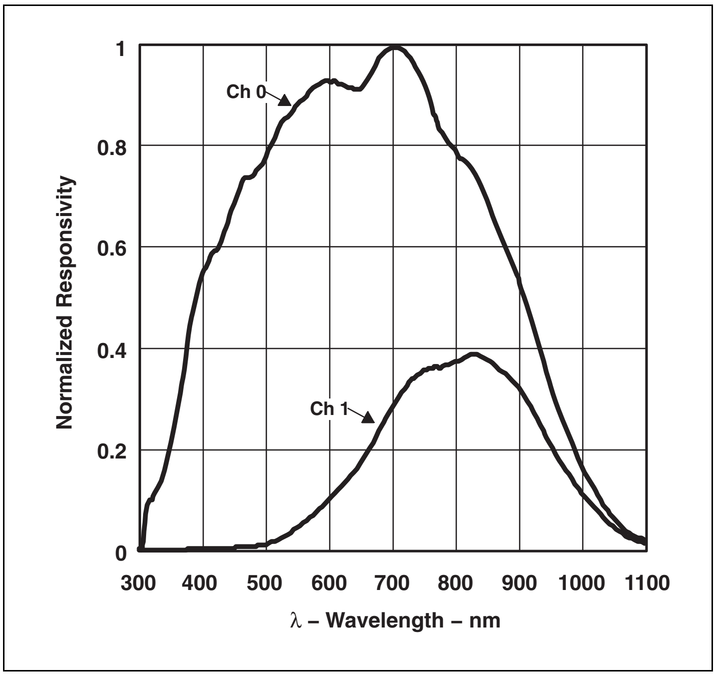


Figure 13:
Normalized I_{DD} vs. V_{DD} and Temperature

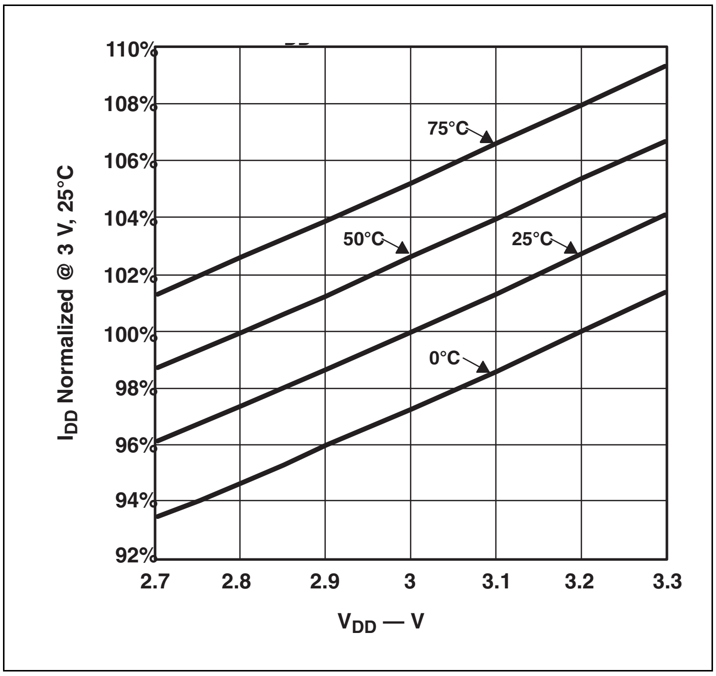
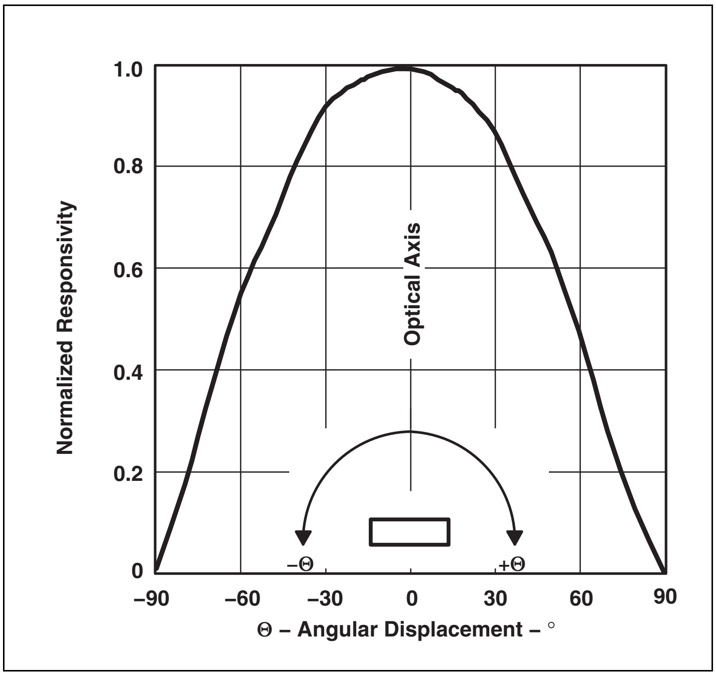


Figure 14:
Normalized Responsivity vs. Angular Displacement

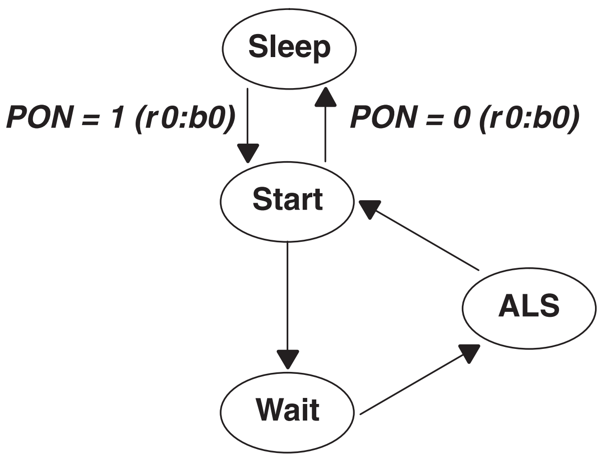


Principles of Operation

System State Machine

The device provides control of ALS and power management functionality through an internal state machine (see Figure 15). After a power-on-reset, the device is in the sleep mode. As soon as the PON bit is set, the device will move to the start state. It will then continue through the Wait and ALS states. If these states are enabled, the device will execute each function. If the PON bit is set to 0, the state machine will continue until all conversions are completed and then go into a low power sleep mode.

Figure 15:
Simplified State Diagram



Note(s): In this document, the nomenclature uses the bit field name in italic followed by the register number and bit number to allow the user to easily identify the register and bit that controls the function. For example, the power on (PON) is in register 0, bit 0. This is represented as *PON (r0:b0)*.

Photodiodes

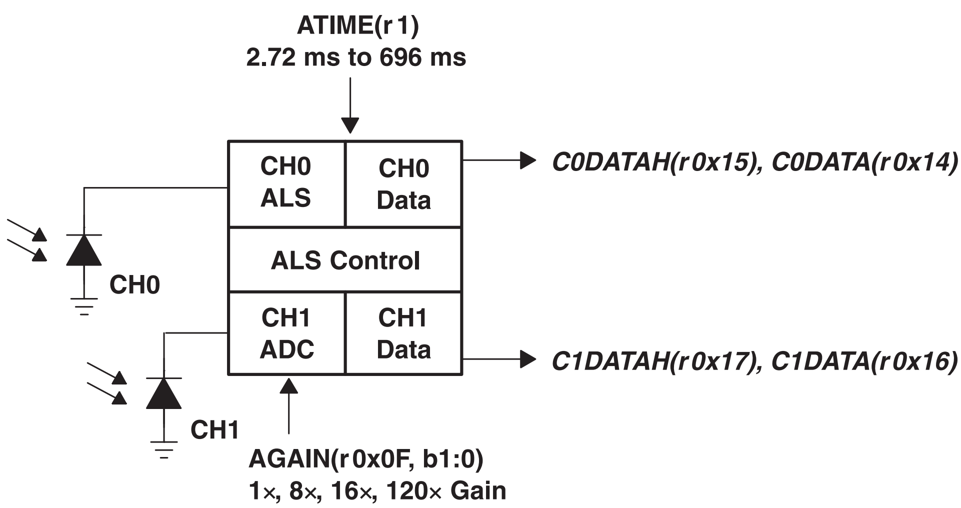
Conventional silicon detectors respond strongly to infrared light, which the human eye does not see. This can lead to significant error when the infrared content of the ambient light is high (such as with incandescent lighting) due to the difference between the silicon detector response and the brightness perceived by the human eye.

This problem is overcome through the use of two photodiodes. The channel 0 photodiode, referred to as the CH0 channel, is sensitive to both visible and infrared light, while the channel 1 photodiode, referred to as CH1, is sensitive primarily to infrared light. Two integrating ADCs convert the photodiode currents to digital outputs. The ADC digital outputs from the two channels are used in a formula to obtain a value that approximates the human eye response in units of lux.

ALS Operation

The ALS engine contains ALS gain control (AGAIN) and two integrating analog-to-digital converters (ADC) for the Channel 0 and Channel 1 photodiodes. The ALS integration time (ATIME) impacts both the resolution and the sensitivity of the ALS reading. Integration of both channels occurs simultaneously and upon completion of the conversion cycle, the results are transferred to the data registers (C0DATA and C1DATA). This data is also referred to as channel *count*. The transfers are double-buffered to ensure data integrity.

Figure 16:
ALS Operation



The registers for programming the integration and wait times are a 2's compliment values. The actual time can be calculated as follows:

ATIME = 256 - Integration Time / 2.72 ms

Inversely, the time can be calculated from the register value as follows:
Integration Time = 2.72 ms × (256 - ATIME)

In order to reject 50/60-Hz ripple strongly present in fluorescent lighting, the integration time needs to be programmed in multiples of 10 / 8.3 ms or the half cycle time. Both frequencies can be rejected with a programmed value of 50 ms (ATIME = 0xED) or multiples of 50 ms (i.e. 100, 150, 200, 400, 600).

The registers for programming the AGAIN hold a two-bit value representing a gain of 1×, 8×, 16×, or 120×. The gain, in terms of amount of gain, will be represented by the value AGAINx, i.e. AGAINx = 1, 8, 16, or 120.

Lux Equation

The lux calculation is a function of CH0 channel count (C0DATA), CH1 channel count (C1DATA), ALS gain (AGAINx), and ALS integration time in milliseconds (ATIME_ms). If an aperture, glass/plastic, or a light pipe attenuates the light equally across the spectrum (300 nm to 1100 nm), then a scaling factor referred to as glass attenuation (GA) can be used to compensate for attenuation. For a device in open air with no aperture or glass/plastic above the device, GA = 1. If it is not spectrally flat, then a custom lux equation with new coefficients should be generated. (See **ams** application note).

Counts per Lux (CPL) needs to be calculated only when ATIME or AGAIN is changed, otherwise it remains a constant. The first segment of the equation (Lux1) covers fluorescent and incandescent light. The second segment (Lux2) covers dimmed incandescent light. The final lux is the maximum of Lux1, Lux2, or 0.

CPL = (ATIME_ms × AGAINx) / (GA × 53)

Lux1 = (C0DATA - 2 × C1DATA) / CPL

Lux2 = (0.6 × C0DATA - C1DATA) / CPL

Lux = MAX(Lux1, Lux2, 0)

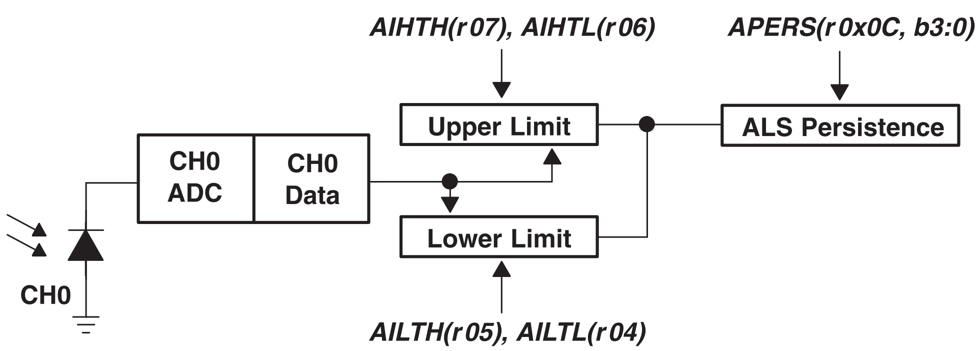
Interrupts

The interrupt feature simplifies and improves system efficiency by eliminating the need to poll the sensor for light intensity values outside of a user-defined range. While the interrupt function is always enabled and it's status is available in the status register (0x13), the output of the interrupt state can be enabled using the ALS interrupt enable (AIEN) field in the enable register (0x00).

Two 16-bit interrupt threshold registers allow the user to set limits below and above a desired light level range. An interrupt can be generated when the ALS CH0 data (C0DATA) falls outside of the desired light level range, as determined by the values in the ALS interrupt low threshold registers (AILTx) and ALS interrupt high threshold registers (AIHTx). It is important to note that the low threshold value must be less than the high threshold value for proper operation.

To further control when an interrupt occurs, the device provides a persistence filter. The persistence filter allows the user to specify the number of consecutive out-of-range ALS occurrences before an interrupt is generated. The persistence register (0x0C) allows the user to set the ALS persistence (APERS) value. See the persistence register for details on the persistence filter values. Once the persistence filter generates an interrupt, it will continue until a special function interrupt clear command is received (see Command Register).

Figure 17:
Programmable Interrupt



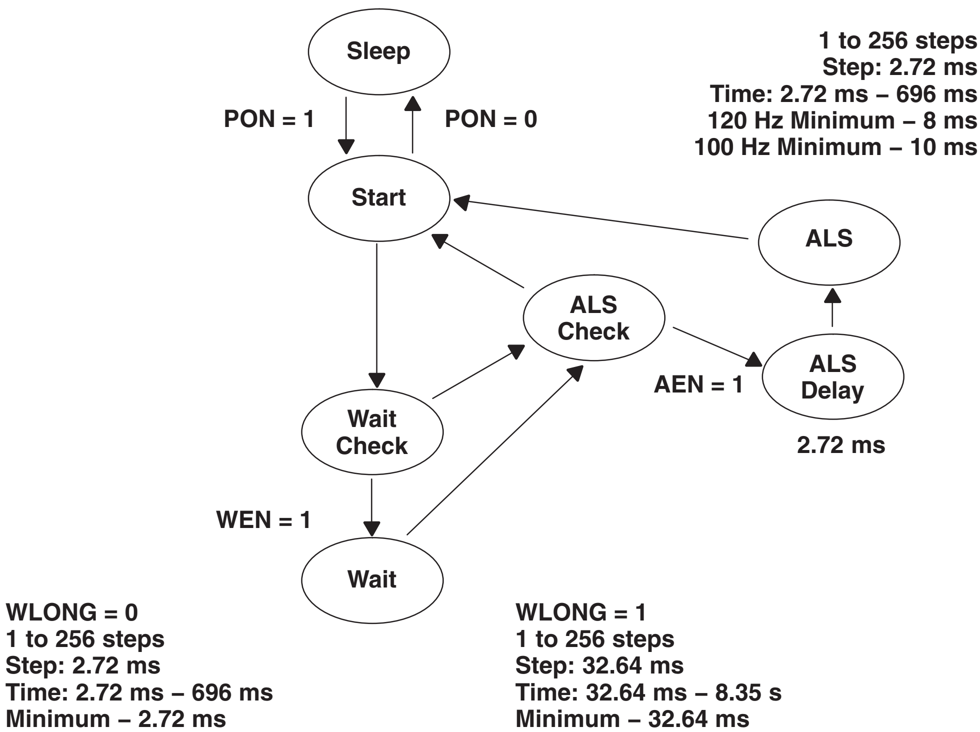
State Diagram

Figure 18 shows a more detailed flow for the state machine. The device starts in the sleep mode. The PON bit is written to enable the device. A 2.72-ms delay will occur before entering the start state.

If the WEN bit is set, the state machine will then cycle through the wait state. If the WLONG bit is set, the wait cycles are extended by 12× over normal operation. When the wait counter terminates, the state machine will step to the ALS state.

The AEN should always be set. In this case, a minimum of 1 integration time step should be programmed. The ALS state machine will continue until it reaches the terminal count at which point the data will be latched in the ALS register and the interrupt set, if enabled.

Figure 18:
Expanded State Diagram



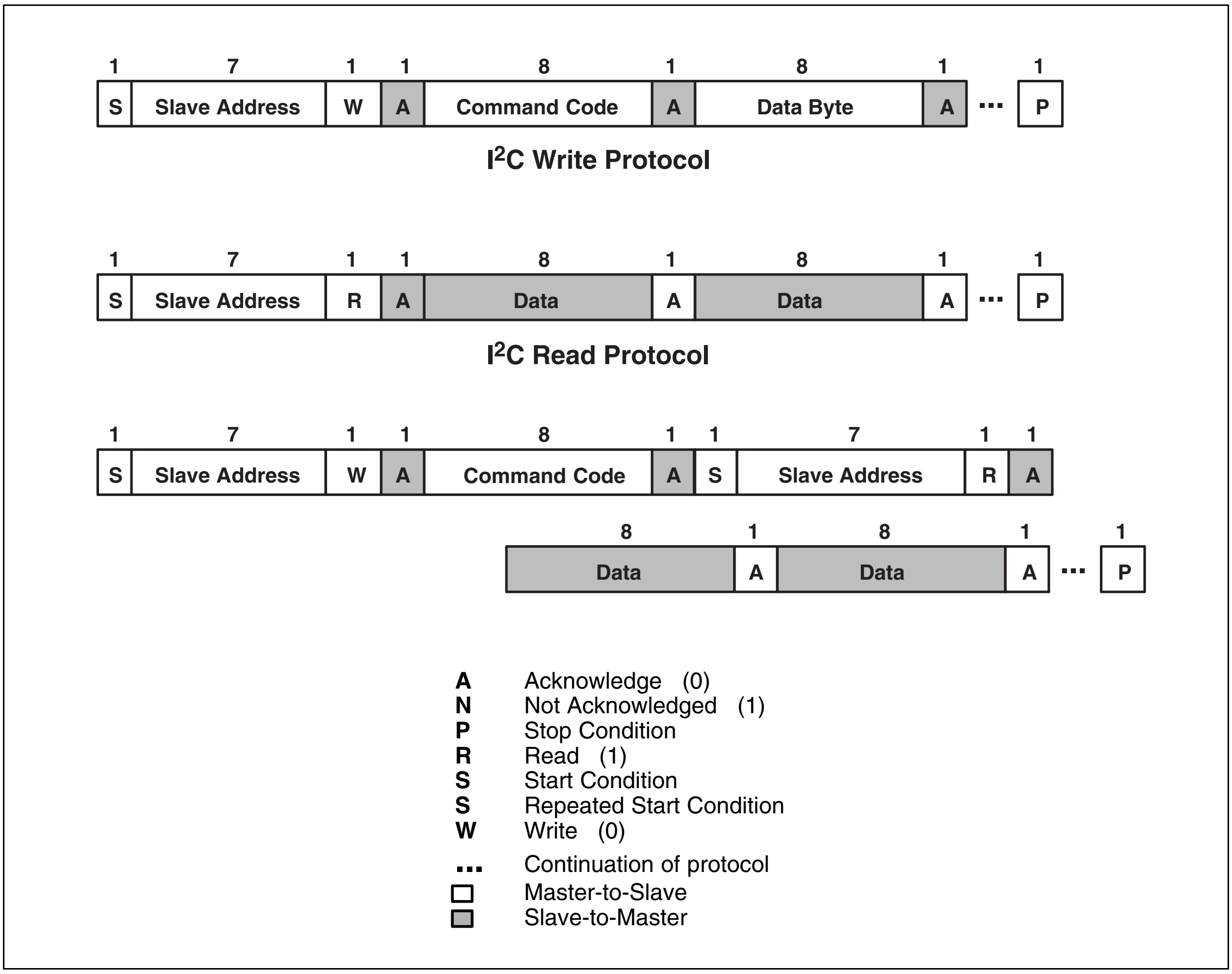
I^2C Protocol

Interface and control are accomplished through an I^2C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The devices support the 7-bit I^2C addressing protocol.

The I^2C standard provides for three types of bus transaction: read, write, and a combined protocol (see Figure 34). During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5-bit register address. The control commands can also be used to clear interrupts.

The I^2C bus protocol was developed by Philips (now NXP). For a complete description of the I^2C protocol, please review the NXP I^2C design specification at http://www.i2c-bus.org/references/.

Figure 19:
I^2C Protocols



Register Description

Register Set

The device is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Figure 20.

Figure 20:
Register Address

Address	Register Name	R/W	Register Function	Reset Value
--	COMMAND	W	Specifies register address	0x00
0x00	ENABLE	R/W	Enables states and interrupts	0x00
0x01	ATIME	R/W	ALS ADC time	0xFF
0x03	WTIME	R/W	Wait time	0xFF
0x04	AILTL	R/W	ALS interrupt low threshold low byte	0x00
0x05	AILTH	R/W	ALS interrupt low threshold high byte	0x00
0x06	AIHTL	R/W	ALS interrupt high threshold low byte	0x00
0x07	AIHTH	R/W	ALS interrupt high threshold high byte	0x00
0x0C	PERS	R/W	Interrupt persistence filters	0x00
0x0D	CONFIG	R/W	Configuration	0x00
0x0F	CONTROL	R/W	Control register	0x00
0x12	ID	R	Device ID	ID
0x13	STATUS	R	Device status	0x00
0x14	C0DATA	R	CH0 ADC low data register	0x00
0x15	C0DATAH	R	CH0 ADC high data register	0x00
0x16	C1DATA	R	CH1 ADC low data register	0x00
0x17	C1DATAH	R	CH1 ADC high data register	0x00

The mechanics of accessing a specific register depends on the specific protocol used. See the section on I^2C protocols on the previous pages. In general, the COMMAND register is written first to specify the specific control/status register for following read/write operations.

Command Register

The command registers specifies the address of the target register for future write and read operations.

Figure 21:
Command Register

	7	6	5	4	3	2	1	0	
COMMAND	COMMAND	TYPE		ADD					- -

<table>
<tr><th>Field</th><th>Bits</th><th colspan="2">Description</th></tr>
<tr><td>COMMAND</td><td>7</td><td colspan="2">Select Command Register. Must write as 1 when addressing COMMAND register.</td></tr>
<tr><td rowspan="7">TYPE</td><td rowspan="7">6:5</td><td colspan="2">Selects type of transaction to follow in subsequent data transfers.</td></tr>
<tr><td>FIELD VALUE</td><td>DESCRIPTION</td></tr>
<tr><td>00</td><td>Repeated byte protocol transaction</td></tr>
<tr><td>01</td><td>Auto-increment protocol transaction</td></tr>
<tr><td>10</td><td>Reserved — Do not use</td></tr>
<tr><td>11</td><td>Special function — See description below</td></tr>
<tr><td colspan="2">Transaction type 00 will repeatedly read the same register with each data access. Transaction type 01 will provide an auto-increment function to read successive register bytes.</td></tr>
<tr><td rowspan="6">ADD</td><td rowspan="6">4:0</td><td colspan="2">Address register/special function field. Depending on the transaction type, see above, this field either specifies a special function command or selects the specific control-status-register for following write and read transactions. The field values listed below apply only to special function commands:</td></tr>
<tr><td>FIELD VALUE</td><td>DESCRIPTION</td></tr>
<tr><td>00000</td><td>Normal — no action</td></tr>
<tr><td>00110</td><td>ALS interrupt clear</td></tr>
<tr><td>other</td><td>Reserved — do not write</td></tr>
<tr><td colspan="2">ALS interrupt clear — clears any pending ALS interrupt. This special function is self clearing.</td></tr>
</table>

Enable Register (0x00)

The ENABLE register is used to power the device ON/OFF, enable functions, and interrupts.

Figure 22:
Enable Register

	7	6	5	4	3	2	1	0	
ENABLE	Reserved			AIEN	WEN	Reserved	AEN	PON	Address 0x00

Field	Bits	Description
Reserved	7:5	Reserved. Write as 0.
AIEN	4	ALS interrupt mask. When asserted, permits ALS interrupts to be generated.
WEN	3	Wait enable. This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
Reserved	2	Reserved. Write as 0.
AEN	1	ALS Enable. Writing a 1 activates the ALS. Writing a 0 disables the ALS.
PON (1)	0	Power ON. This bit activates the internal oscillator to permit the timers and ADC channels to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator.

Note(s):

1. A minimum interval of 2.72 ms must pass after PON is asserted before ALS can be initiated. This required time is enforced by the hardware in cases where the firmware does not provide it.

ALS Timing Register (0x01)

The ALS timing register controls the internal integration time of the ALS ADCs in 2.72-ms increments.

Figure 23:
ALS Timing Register

Field	Bits	Description			
ATIME	7:0	**VALUE**	**INTEG_CYCLES**	**TIME**	**MAX COUNT**
		0xFF	1	2.72 ms	1024
		0xF6	10	27.2 ms	10240
		0xDB	37	101 ms	37888
		0xC0	64	174 ms	65535
		0x00	256	696 ms	65535

Wait Time Register (0x03)

Wait time is set 2.72 ms increments unless the WLONG bit is asserted in which case the wait times are 12× longer. WTIME is programmed as a 2's complement number.

Figure 24:
Wait Time Register

Field	Bits	Description			
WTIME	7:0	**REGISTER VALUE**	**WAIT TIME**	**TIME (WLONG = 0)**	**TIME (WLONG = 1)**
		0xFF	1	2.72 ms	0.032 s
		0xB6	74	201 ms	2.4 s
		0x00	256	696 ms	8.3 s

Note(s):

1. The Wait Time Register should be configured before AEN is asserted.

ALS Interrupt Threshold Registers (0x04 - 0x07)

The ALS interrupt threshold registers provides the values to be used as the high and low trigger points for the comparison function for interrupt generation. If C0DATA crosses below the low threshold specified, or above the higher threshold, an interrupt is asserted on the interrupt pin.

Figure 25:
ALS Interrupt Threshold Registers

Register	Address	Bits	Description
AILTL	0x04	7:0	ALS low threshold lower byte
AILTH	0x05	7:0	ALS low threshold upper byte
AIHTL	0x06	7:0	ALS high threshold lower byte
AIHTH	0x07	7:0	ALS high threshold upper byte

Persistence Register (0x0C)

The persistence register controls the filtering interrupt capabilities of the device. Configurable filtering is provided to allow interrupts to be generated after each ADC integration cycle or if the ADC integration has produced a result that is outside of the values specified by threshold register for some specified amount of time. ALS interrupts are generated using C0DATA.

Figure 26:
Persistence Register

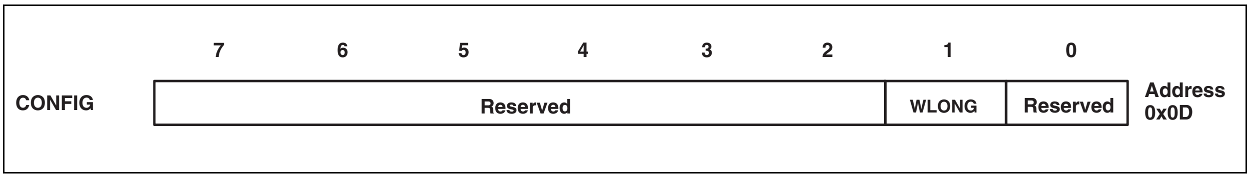
	7	6	5	4	3	2	1	0	
PERS	Reserved				APERS				Address 0x0C

<table>
<tr><th>Field</th><th>Bits</th><th colspan="3">Description</th></tr>
<tr><td>Reserved</td><td>7:4</td><td colspan="3">Reserved</td></tr>
<tr><td rowspan="18">APERS</td><td rowspan="18">3:0</td><td colspan="3">Interrupt persistence. Controls rate of interrupt to the host processor.</td></tr>
<tr><td>FIELD VALUE</td><td>MEANING</td><td>INTERRUPT PERSISTENCE FUNCTION</td></tr>
<tr><td>0000</td><td>Every</td><td>Every ALS cycle generates an interrupt</td></tr>
<tr><td>0001</td><td>1</td><td>1 value outside of threshold range</td></tr>
<tr><td>0010</td><td>2</td><td>2 consecutive values out of range</td></tr>
<tr><td>0011</td><td>3</td><td>3 consecutive values out of range</td></tr>
<tr><td>0100</td><td>5</td><td>5 consecutive values out of range</td></tr>
<tr><td>0101</td><td>10</td><td>10 consecutive values out of range</td></tr>
<tr><td>0110</td><td>15</td><td>15 consecutive values out of range</td></tr>
<tr><td>0111</td><td>20</td><td>20 consecutive values out of range</td></tr>
<tr><td>1000</td><td>25</td><td>25 consecutive values out of range</td></tr>
<tr><td>1001</td><td>30</td><td>30 consecutive values out of range</td></tr>
<tr><td>1010</td><td>35</td><td>35 consecutive values out of range</td></tr>
<tr><td>1011</td><td>40</td><td>40 consecutive values out of range</td></tr>
<tr><td>1100</td><td>45</td><td>45 consecutive values out of range</td></tr>
<tr><td>1101</td><td>50</td><td>50 consecutive values out of range</td></tr>
<tr><td>1110</td><td>55</td><td>55 consecutive values out of range</td></tr>
<tr><td>1111</td><td>60</td><td>60 consecutive values out of range</td></tr>
</table>

Configuration Register (0x0D)

The configuration register sets the wait long time.

Figure 27:
Configuration Register

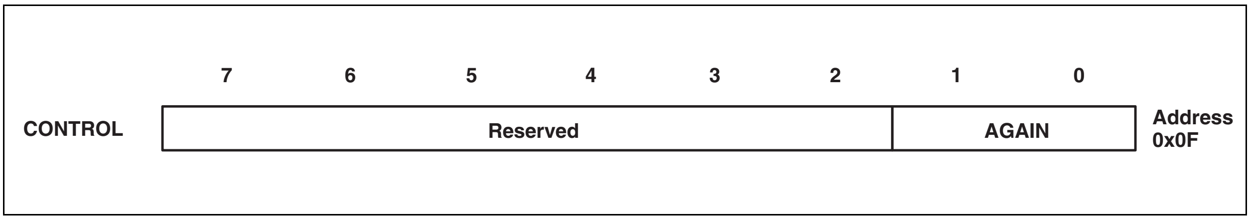


Field	Bits	Description
Reserved	7:2	Reserved. Write as 0.
WLONG	1	Wait Long. When asserted, the wait cycles are increased by a factor 12× from that programmed in the WTIME register.
Reserved	0	Reserved. Write as 0.

Control Register (0x0F)

The Control register provides eight bits of miscellaneous control to the analog block. These bits typically control functions such as gain settings and/or diode selection.

Figure 28:
Control Register

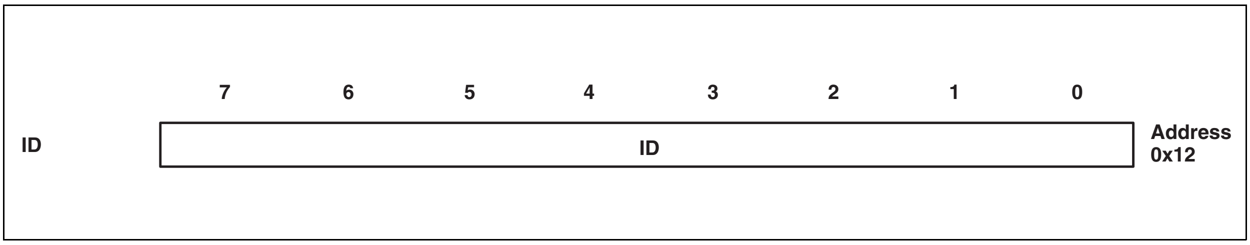


<table>
<tr><th>Field</th><th>Bits</th><th colspan="2">Description</th></tr>
<tr><td>Reserved</td><td>7:2</td><td colspan="2">Reserved. Write bits as 0</td></tr>
<tr><td rowspan="6">AGAIN</td><td rowspan="6">1:0</td><td colspan="2">ALS Gain Control.</td></tr>
<tr><td>FIELD VALUE</td><td>ALS GAIN VALUE</td></tr>
<tr><td>00</td><td>1× gain</td></tr>
<tr><td>01</td><td>8× gain</td></tr>
<tr><td>10</td><td>16× gain</td></tr>
<tr><td>11</td><td>120× gain</td></tr>
</table>

ID Register (0x12)

The ID Register provides the value for the part number. The ID register is a read-only register.

Figure 29:
ID Register

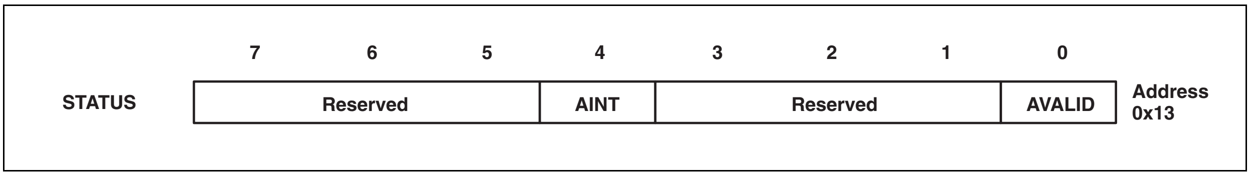


Field	Bits	Description	
ID	7:0	Part number identification	0x04 = TSL25711 and TSL25715
			0x0D = TSL25713

Status Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

Figure 30:
Status Register



Field	Bit	Description
Reserved	7:5	Reserved. Write as 0.
AINT	4	ALS Interrupt. Indicates that the device is asserting an ALS interrupt.
Reserved	3:1	Reserved.
AVALID	0	ALS Valid. Indicates that the ALS CH0 / CH1 channels have completed an integration cycle.