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# TSL2584TSV

## Light-to-Digital Device

## General Description

The TSL2584TSV is a very-high sensitivity light-to-digital converter that transforms light intensity into a digital signal output capable of direct $I^2C$ interface. The device combines one broadband photodiode (visible plus infrared), one infrared-responding photodiode, and a photopic infrared-blocking filter on a single CMOS integrated circuit. Two integrating ADCs convert the photodiode currents into a digital output that represents the irradiance measured on each channel. This digital output can be input to a microprocessor where illuminance (ambient light level) in lux is derived using an empirical formula to approximate the human eye response. The TSL2584TSV supports a traditional level style interrupt that remains asserted until the firmware clears it.

*Ordering Information and Content Guide appear at end of datasheet.*

## Key Benefits & Features

The benefits and features of TSL2584TSV, Light-to-Digital Device are listed below:

**Figure 1:**
**Added Value of Using TSL2584TSV**

| Benefits | Features |
|---|---|
| • Approximates Human Eye Response | • Dual Diode with Photopic Filter |
| • Flexible Operation | • Programmable Analog Gain and Integration Time |
| • Suited for Operation Behind Dark Glass | • 1000000: 1 Dynamic Range |
| • Low Operating Overhead | • Programmable Upper and Lower Thresholds<br>• Programmable Persistence Filter |
| • Low Power | • 3.0 µA Sleep State |
| • Industry Standard Two-Wire Interface | • $I^2C$ Fast Mode Compatible Interface<br>  • Data Rates up to 400 kbit/s<br>  • Input Voltage Levels Compatible with1.8–V Bus |
| • Ultra-Small Foot-Print | • 1.145 mm x 1.660 mm TSV (Through Silicon Via)<br>• 0.218 mm Height w/o Solder Balls |
| • Unlimited Manufacturing Floor Life | • MSL1 Rated |

## Applications

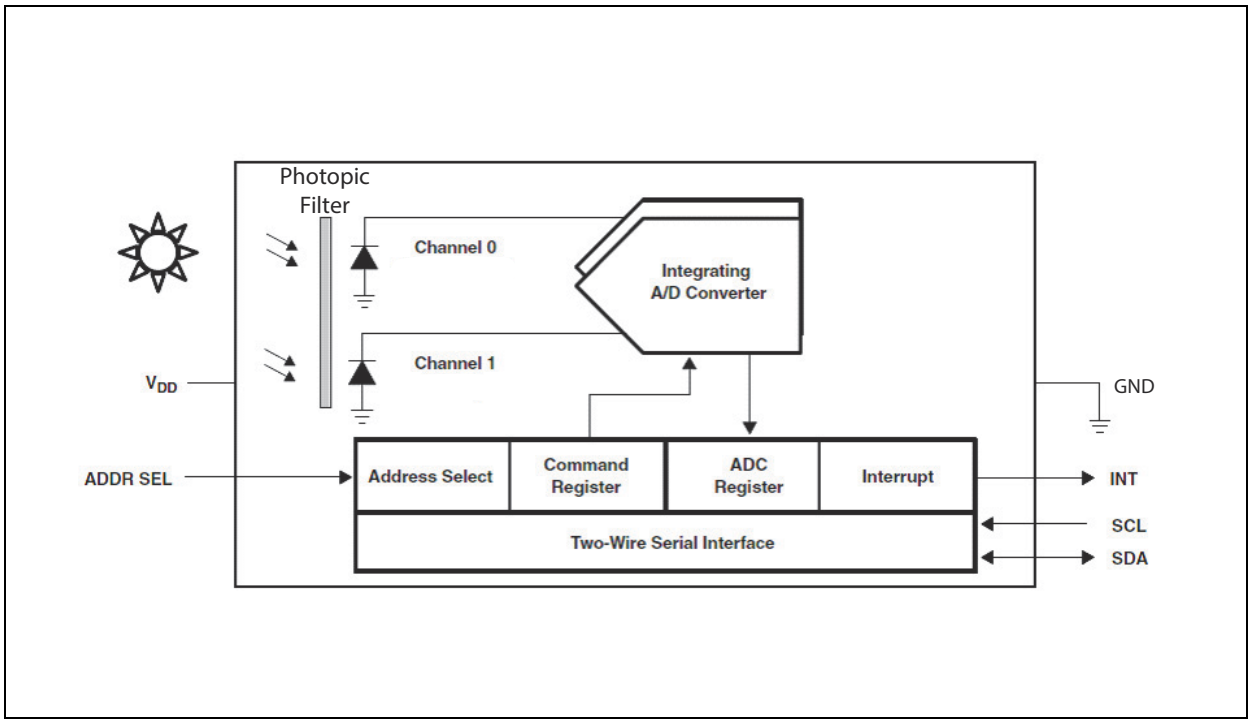
The TSL2584TSV applications include:

- Display Backlight Control
- Keyboard Illumination Control
- Printer Paper Detection
- Medical Diagnostics

## Block Diagram

The functional blocks of this device are shown below:

**Figure 2:**
**TSL2584TSV Block Diagram**



## Detailed Description

The TSL2584TSV contains two integrating analog-to-digital converters (ADC) that integrate currents from two photodiodes. Integration of both channels occurs simultaneously. Upon completion of the conversion cycle, the conversion result is transferred to the Channel 0 and Channel 1 data registers. The transfers are double-buffered to ensure that the integrity of the data is maintained. After the transfer, the device automatically begins the next integration cycle.

Communication with the device is accomplished through a standard, two-wire $I^2C$ serial bus. Consequently, the TSL2584TSV can be easily connected to a microcontroller or embedded controller. No external circuitry is required for signal conditioning. Because the output of the device is digital, the output is effectively immune to noise when compared to an analog signal.

The TSL2584TSV also supports an interrupt feature that simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity value. The primary purpose of the interrupt function is to detect a meaningful change in light intensity. The concept of a meaningful change can be defined by the user both in terms of light intensity and time, or persistence, of that change in intensity. The device has the ability to define thresholds above and below the current light level. An interrupt is generated when the value of a conversion exceeds either of these limits.

## Pin Assignment

The TSL2584TSV pin assignments are described below.

**Figure 3:**
**Pin Diagram**

**Package TSV - 6 Lead Through - Silicon VIA (Top View):** Package drawing is not to scale.

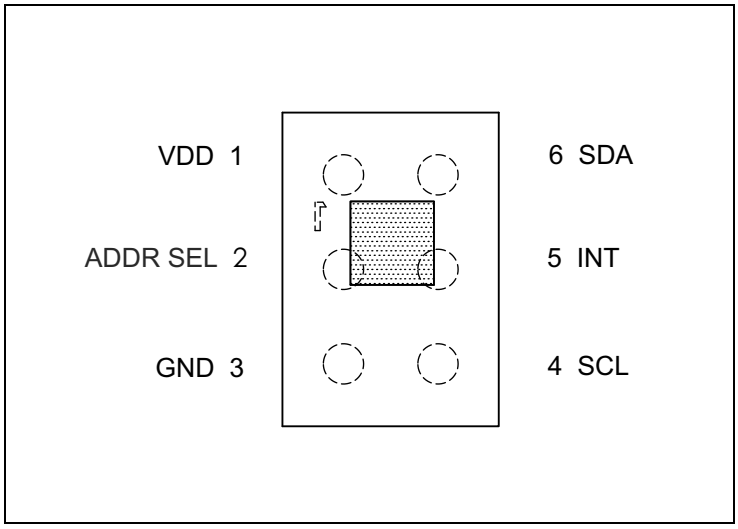



**Figure 4:**
**Pin Description**

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | $V_{DD}$ | Supply voltage |
| 2 | ADDR_SEL | Address select – three-state. |
| 3 | GND | Power supply ground. All voltages are referenced to GND. |
| 4 | SCL | $I^2C$ serial clock input terminal |
| 5 | INT | Interrupt — open drain output (active low). |
| 6 | SDA | $I^2C$ serial data I/O terminal |

## Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 5:**
**Absolute Maximum Ratings**

| Parameter | Min | Max | Units | Comments |
|---|---|---|---|---|
| Supply voltage, $V_{DD}$ | | 3.8 | V | All voltages are with respect to GND |
| Output terminal voltage $V_O$ | -0.5 | 3.8 | V | |
| Output terminal current $I_O$ | -1 | 20 | mA | |
| Storage temperature range, $T_{STRG}$ | -40 | 85 | °C | |
| ESD tolerance, human body model | ±2000 | | V | |

## Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

**Figure 6:**
**Recommended Operating Conditions**

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 2.7 | 3 | 3.6 | V |
| $T_A$ | Operating free-air temperature | -40 | | 85 | °C |

**Figure 7:**
**Operating Characteristics, $V_{DD}$=3V, $T_A$=25°C (unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current | Active | | 175 | 250 | µA |
| | | Sleep state - no $I^2C$ activity | | 3 | 10 | |
| $V_{OL}$ | INT, SDA output low voltage | 3mA sink current | 0 | | 0.4 | V |
| | | 6mA sink current | 0 | | 0.6 | |
| $I_{LEAK}$ | Leakage current, SDA, SCL, INT pins | | -5 | | 5 | µA |
| $V_{IH}$ | SCL, SDA input high voltage | | 1.25 | | | V |
| $V_{IL}$ | SCL, SDA input low voltage | | | | 0.54 | V |

**Figure 8:**
**ALS Characteristics, $V_{DD}$=3V, $T_A$=25°C, GAIN=16x, AEN=1(unless otherwise noted) (1)**

| Parameter | Conditions | Channel | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Dark ADC count value | $E_e$ = 0, GAIN = 111x, ATIME=0xB6 (200ms) | CH0<br>CH1 | 0<br>0 | 1<br>1 | 3<br>3 | counts |
| ADC integration time step size | ATIME = 0xFF | | 2.58 | 2.73 | 2.90 | ms |
| ADC integration time steps (4) | | | 1 | | 256 | steps |
| Full scale ADC count value | ATIME = 0xDB (100ms)<br>ATIME = 0x6C (400ms) | | | | 37887<br>65535 | counts |
| ADC count value | White light<br>$E_e$ = 218 µW/cm$^2$<br>ATIME = 0xF6 (27ms) (2) | CH0<br>CH1 | 2480 | 3100<br>223 | 3720 | counts |
| | $\lambda_p$ = 850 nm<br>$E_e$ = 220 µW/cm$^2$,<br>ATIME = 0xF6 (27ms) (3) | CH0 | | | 400 | counts |
| ADC count value ratio: CH1/CH0 | White light (2) | | 0.036 | 0.072 | 0.108 | |
| $R_e$ irradiance responsivity | White light,<br>ATIME = 0xF6 (27 ms) (2) | CH0<br>CH1 | 11.4 | 14.2<br>1.0 | 17.1 | counts/ (µW/cm$^2$) |
| Gain scaling, relative to 1x gain setting | GAIN = 8x | CH0<br>CH1 | 7<br>7 | 8<br>8 | 9<br>9 | x |
| | GAIN = 16x | CH0<br>CH1 | 15<br>15 | 16<br>16 | 17<br>17 | |
| | GAIN = 111x<br>Decoupling capacitor 25 mm from VDD pin (5) | CH0<br>CH1 | 97<br>100 | 107<br>115 | 115<br>125 | |

**Note(s):**

1. Optical measurements are made using small-angle incident radiation from light-emitting diode optical sources. Visible white LEDs and infrared 850 nm LEDs are used for final product testing for compatibility with high-volume production.
2. The white LED irradiance is supplied by a white light-emitting diode with a nominal color temperature of 4000 K.
3. The 850 nm irradiance $E_e$ is supplied by a GaAs light-emitting diode with the following typical characteristics: peak wavelength $\lambda_p$ = 850 nm and spectral halfwidth $\Delta\lambda$½ = 42 nm.
4. The integration time $T_{int}$, is dependent on the internal oscillator frequency ($f_{OSC}$) and on the number of integration cycles (ATIME) in the Timing Register as described in the register section. For nominal $f_{OSC}$ = 750 kHz, nominal Tint = 2.7 ms x ATIME.
5. 111x gain is affected by the line inductance between the VDD pin and the decoupling capacitor.

## Timing Characteristics

The timing characteristics of TSL2584TSV are given below.

**Figure 9:**
**AC Electrical Characteristics, $V_{DD}$ = 3 V, $T_A$ = 25°C (unless otherwise noted)**

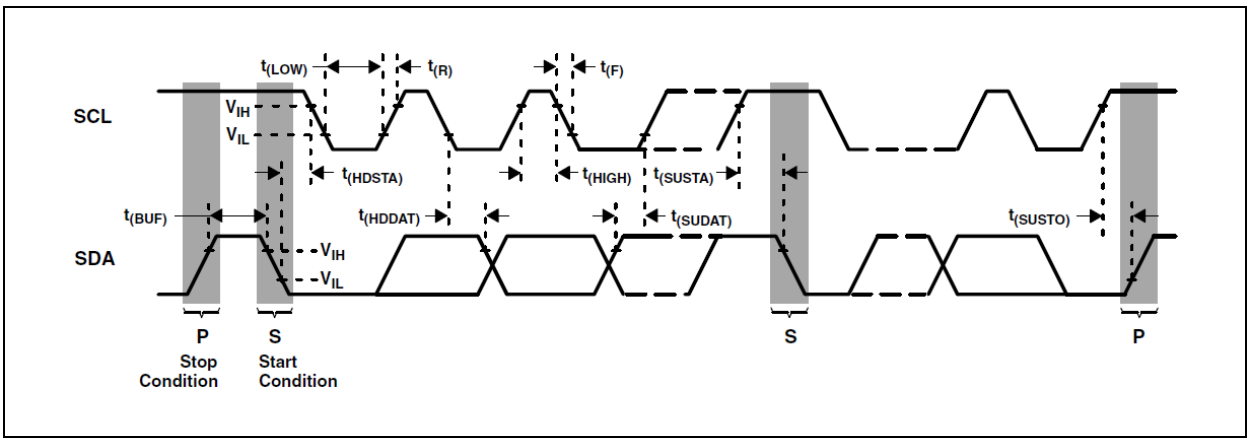
| Parameter(1) | Description | Min | Max | Units |
|---|---|---|---|---|
| $t_{(CONV)}$ | Conversion time | 2.7 | 688 | ms |
| $f_{(SCL)}$ | Clock frequency | 0 | 400 | kHz |
| $t_{(BUF)}$ | Bus free time between start and stop condition | 1.3 | | µs |
| $t_{(HDSTA)}$ | Hold time after (repeated) start condition. After this period, the first clock is generated. | 0.6 | | µs |
| $t_{(SUSTA)}$ | Repeated start condition setup time | 0.6 | | µs |
| $t_{(SUSTO)}$ | Stop condition setup time | 0.6 | | µs |
| $t_{(HDDAT)}$ | Data hold time | 0.043 | 0.9 | µs |
| $t_{(SUDAT)}$ | Data setup time | 100 | | ns |
| $t_{(LOW)}$ | SCL clock low period | 1.3 | | µs |
| $t_{(HIGH)}$ | SCL clock high period | 0.6 | | µs |
| $t_F$ | Clock/data fall time | | 300 | ns |
| $t_R$ | Clock/data rise time | | 300 | ns |
| $C_i$ | Input pin capacitance | | 10 | pF |

**Note(s):**

1. Specified by design and characterization; not production tested.

## Timing Diagrams

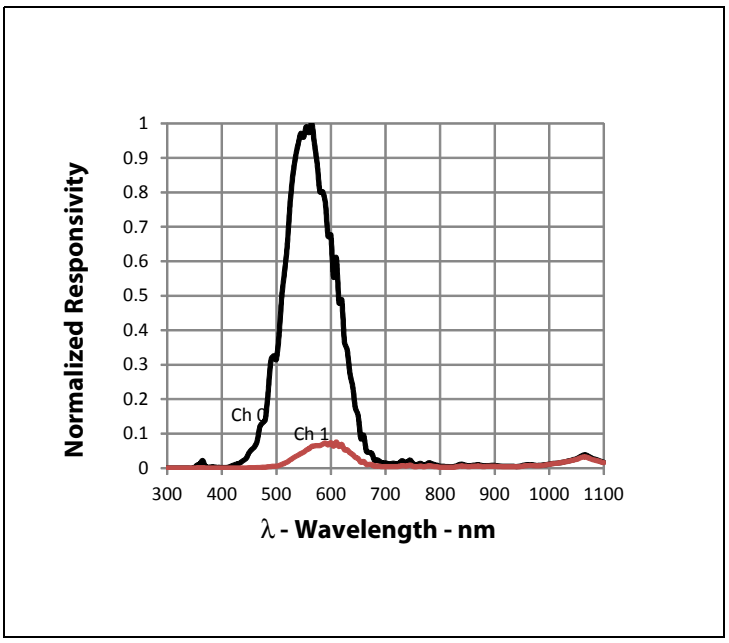
**Figure 10:**
**Parameter Measurement Information**



# Typical Operating Characteristics

**Spectral Responsivity:** Two channel response allows for tunable illuminance (lux) calculation regardless of transmissivity of glass.

Figure 11:
Spectral Responsivity




**111x Gain Scale vs. Line Inductance:** High gain mode (111x) dependency on the line inductance between the VDD pin and the decoupling capacitor.

Figure 12:
111x Gain Scale vs. Line Inductance

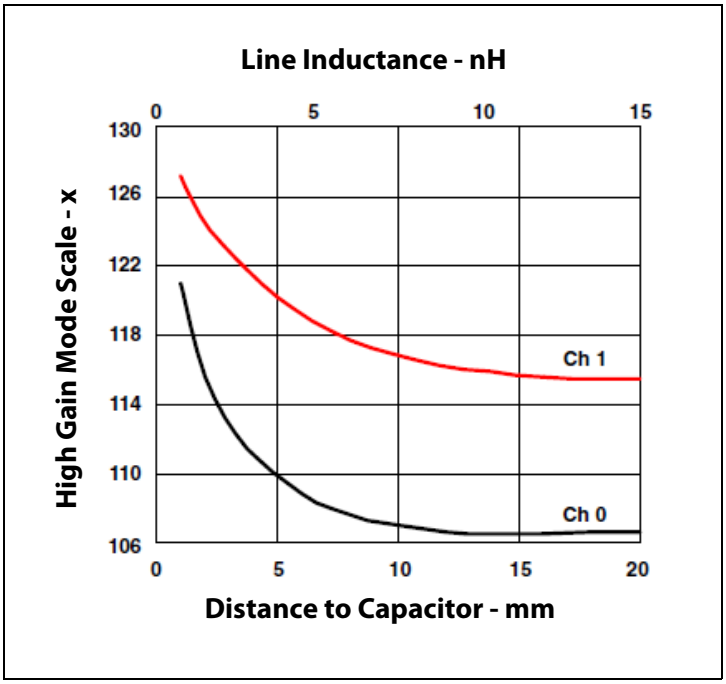
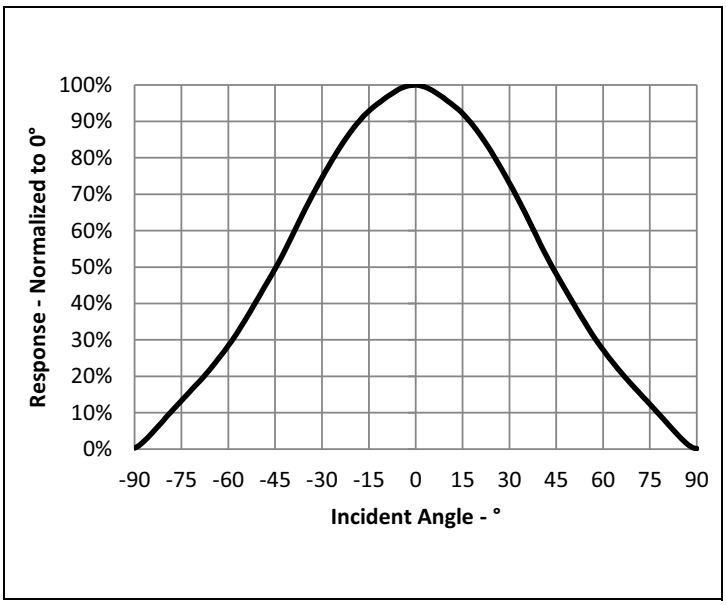


**Figure 13:**
**Ch0 Response to White LED (CCT = 4000K) vs. Incident Angle**



## Digital Interface

Interface and control of the device is accomplished through a two-wire serial interface to a set of registers that provide access to device control functions and output data. The serial interface is compatible with the $I^2C$ bus, Fast-Mode. The device offers three slave addresses that are selectable via an external pin (ADDR SEL). The slave address options are shown in Figure 14.

**Figure 14:**
**Slave Address Selection**

| ADDR SEL Terminal Level | 7-BIT Slave Address | |
|---|---|---|
| GND | 0101001 | 0x29 |
| Float | 0111001 | 0x39 |
| $V_{DD}$ | 1001001 | 0x49 |

**Note(s):**

1. The slave addresses are 7 bits. A read/write bit should be appended to the slave address by the master device to properly communicate with the slave device.

## Register Description

The device is controlled and monitored by sixteen registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Figure 15.

**Figure 15:**
**Register Map**

| Address | Register Name | R/W | Register Function |
|---|---|---|---|
| –– | COMMAND | W | Specifies register address |
| 00h | CONTROL | R/W | Control of basic functions |
| 01h | TIMING | | Integration time/gain control |
| 02h | INTERRUPT | | Interrupt control |
| 03h | THLLOW | | Low byte of low interrupt threshold |
| 04h | THLHIGH | | High byte of low interrupt threshold |
| 05h | THHLOW | | Low byte of high interrupt threshold |
| 06h | THHHIGH | | High byte of high interrupt threshold |
| 07h | ANALOG | | Analog control register |
| 12h | ID | R | Part number / Rev ID |
| 14h | DATA0LOW | | ADC Channel 0 - LOW data register |
| 15h | DATA0HIGH | | ADC Channel 0 - HIGH data register |
| 16h | DATA1LOW | | ADC Channel 1- LOW data register |
| 17h | DATA1HIGH | | ADC Channel 1 - HIGH data register |
| 18h | TIMERLOW | | Manual integration timer LOW register |
| 19h | TIMERHIGH | | Manual integration timer HIGH register |
| 1Eh | ID2 | R/W | Supplemental identification |

The mechanics of accessing a specific register depends on the specific $I^2C$ protocol used. See the section on $I^2C$ protocols, above. In general, the Command Register is written first to specify the specific control/status register for following read/write operations.

## Command Register

The Command Register specifies the address of the target register for subsequent read and write operations and contains eight bits as described in Figure 16. The command register defaults to 00h at power on.

**Figure 16:**
**Command Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CMD | TRANSACTION | | ADDRESS | | | | |

| Fields | Bits | Description (Reset - 00h) | |
|---|---|---|---|
| CMD | 7 | Select command register. Must write as 1 when addressing COMMAND register. | |
| TRANSACTION | 6:5 | Select type of transaction to follow in subsequent data transfers: | |
| | | **FIELD VALUE** | **DESCRIPTION** |
| | | 00 | Repeated byte protocol transaction |
| | | 01 | Auto - increment protocol transaction |
| | | 10 | Reserved - Do not use |
| | | 11 | Special function - See description below |
| | | Transaction type 00 will repeatedly read the same register with each data access. Transaction type 01 will provide an auto-increment function to read successive register bytes. | |

<table>
<tr><th>Fields</th><th>Bits</th><th colspan="3">Description (Reset - 00h)</th></tr>
<tr><td rowspan="7">ADDRESS</td><td rowspan="7">4:0</td><td colspan="3">Register Address/Special Function. This field selects the specific control or status register for following write and read commands according to Figure 15. When the TRANSACTION field is set to 11b, this field specifies a special command function as outlined below.</td></tr>
<tr><td>FIELD VALUE</td><td>SPECIAL FUNCTION</td><td>DESCRIPTION</td></tr>
<tr><td>00000</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>00001</td><td>Interrupt clear</td><td>Clear any pending interrupt and is a write-once-to-clear bit</td></tr>
<tr><td>00010</td><td>Stop manual integration</td><td>When the Timing Register is set to 00h, a Byte command with the ADDRESS field set to 0010b will stop a manual integration. The actual length of the integration cycle may be read in the MANUAL INTEGRATION TIMER Register.</td></tr>
<tr><td>00011</td><td>Start manual integration</td><td>When the Timing Register is set to 00h, a Byte command with the ADDRESS field set to 0011b will start a manual integration. The actual length of the integration cycle may be read in the MANUAL INTEGRATION TIMER Register.</td></tr>
<tr><td>x11xx</td><td>Reserved</td><td>Reserved</td></tr>
</table>

## Control Register (00h)

The Control Register is used primarily to power the device up and down as shown in Figure 17.

**Figure 17:**
**Control Register.**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | ADC_INTR | ADC_VALID | Reserved | | ADC_EN | POWER |

| Field | Bits | Description (Reset - 00h) |
|---|---|---|
| Reserved | 7:6 | Reserved. Write as 0. |
| ADC_INTR | 5 | ADC Interrupt. Read only. Indicates that the device is asserting an interrupt. |
| ADC_VALID | 4 | ADC Valid. Read only. Indicates that the ADC Channel has completed an integration cycle. |
| Reserved | 3:2 | Reserved. Write as 0. |
| ADC_EN | 1 | ADC Enable. This field enables the two ADC Channels to begin integration. Writing a 1 activates the ADC Channels, and writing a 0 disables the ADCs. |
| POWER | 0 | Power On. Writing a 1 powers on the device, and writing a 0 turns it off. |

**Note(s):**

1. ADC_EN and POWER must be asserted before the ADC changes will operate correctly. After POWER is asserted, a 2-ms delay is required before asserting ADC_EN.
2. The device registers should be configured before ADC_EN is asserted.

## Timing Register (01h)

The Timing Register controls the internal integration time of the ADC Channels in 2.7 ms increments. The TIMING register defaults to 00h at power on.

**Figure 18:**
**Timing Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ATIME | | | | | | | |

| Field | Bits | Description (Reset = 00h) |
|---|---|---|
| ATIME | 7:0 | Integration Cycles. Specifies the integration time in 2.7-ms intervals. Time is expressed as a 2's complement number. So, to quickly work out the correct value to write:<br>• (Step 1) Determine the number of 2.7-ms intervals required<br>• (Step 2) Take the 2's complement.<br>Example: For a 1 × 2.7-ms interval, 0xFF should be written. For 2 × 2.7-ms intervals, 0xFE should be written. The maximum integration time is 688.5 ms (00000001b).<br><br>Writing a 0x00 to this register is a special case and indicates manual timing mode. See CONTROL and MANUAL INTEGRATION TIMER Registers for other device options related to manual integration. |

| INTEG_CYCLES | TIME | VALUE |
|---|---|---|
| – | Manual integration | 00000000 |
| 1 | 2.7 ms | 11111111 |
| 2 | 5.4 ms | 11111110 |
| 19 | 51.3 ms | 11101101 |
| 37 | 99.9 ms | 11011011 |
| 74 | 199.8 ms | 10110110 |
| 148 | 399.6 ms | 01101100 |
| 255 | 688.5 ms | 00000001 |

**Note(s):**

1. The Byte protocol cannot be used when ATIME is greater than 127 (for example ATIME[7] = 1) since the upper bit is set aside for write transactions in the COMMAND register.

## Interrupt Register (02h)

The Interrupt Register controls the extensive interrupt capabilities of the device. The open-drain interrupt pin is active low and requires a pull-up resistor to $V_{DD}$ in order to pull high in the inactive state. The Interrupt Register provides control over when a meaningful interrupt will occur. The concept of a meaningful change can be defined by the user both in terms of light intensity and time, or persistence of that change in intensity. The value must cross the threshold (as configured in the Threshold Registers 03h through 06h) and persist for some period of time as outlined in Figure 19.

When a level Interrupt is selected, an interrupt is generated whenever the last conversion results in a value outside of the programmed threshold window. The interrupt is active-low and remains asserted until cleared by writing an 11 in the TRANSACTION field in the COMMAND register.

**Figure 19:**
**Interrupt Control Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | INTR_STOP | INTR | | PERSIST | | | |

| Field | Bits | Description (Reset = 00h) |
|---|---|---|
| Reserved | 7 | Reserved. Write as 0. |
| INTR_STOP (2) | 6 | Stop ADC Integration on Interrupt. When high, ADC integration will stop once an interrupt is asserted. To resume operation (1) de-assert ADC_EN using CONTROL register, (2) clear interrupt using COMMAND register, and (3) re-assert ADC_EN using CONTROL register. |
| INTR | 5:4 | INTR Control Select. This field determines mode of interrupt logic according to Figure 20, below. |
| PERSIST | 3:0 | Interrupt Persistence. Controls rate of interrupts to the host processor as shown in Figure 21, below. |

**Note(s):**

1. Interrupts are based on the value of Channel 0 only.
2. Use this bit to isolate a particular condition when the sensor is continuously integrating.

**Figure 20:**
**Interrupt Control Select**

| INTR Field Value | Read Value |
|---|---|
| 00 | Interrupt output disabled |
| 01 | Level interrupt |
| 10 | Reserved |
| 11 | Reserved |

**Note(s):**

1. Field value of 11 may be used to test interrupt connectivity in a system or to assist in debugging interrupt service routine software.

**Figure 21:**
**Interrupt Persistence Select**

| Persist Field Value | Interrupt Persist Function |
|---|---|
| 0000 | Every ADC cycle generates interrupt |
| 0001 | Any value outside of threshold range |
| 0010 | 2 integration time periods out of range |
| 0011 | 3 integration time periods out of range |
| 0100 | 4 integration time periods out of range |
| 0101 | 5 integration time periods out of range |
| 0110 | 6 integration time periods out of range |
| 0111 | 7 integration time periods out of range |
| 1000 | 8 integration time periods out of range |
| 1001 | 9 integration time periods out of range |
| 1010 | 10 integration time periods out of range |
| 1011 | 11 integration time periods out of range |
| 1100 | 12 integration time periods out of range |
| 1101 | 13 integration time periods out of range |
| 1110 | 14 integration time periods out of range |
| 1111 | 15 integration time periods out of range |

## Interrupt Threshold Registers (03h-06h)

The Interrupt Threshold Registers store the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by Channel 0 crosses below or is equal to the low threshold specified, an interrupt is asserted on the interrupt pin. If the value generated by Channel 0 crosses above the high threshold specified, an interrupt is asserted on the interrupt pin. Registers THLLOW and THLHIGH provide the low byte and high byte, respectively, of the lower interrupt threshold. Registers THHLOW and THHHIGH provide the low and high bytes, respectively, of the upper interrupt threshold. The high and low bytes from each set of registers are combined to form a 16-bit threshold value. The interrupt threshold registers default to 00h on power up.

**Figure 22:**
**Interrupt Threshold Registers**

| Register | Address | Bits | Description |
|---|---|---|---|
| THLLOW | 3h | 7:0 | ADC Channel 0 lower byte of the low threshold |
| THLHIGH | 4h | 7:0 | ADC Channel 0 upper byte of the low threshold |
| THHLOW | 5h | 7:0 | ADC Channel 0 lower byte of the high threshold |
| THHHIGH | 6h | 7:0 | ADC Channel 0 upper byte of the high threshold |

**Note(s):**

1. Since two 8-bit values are combined for a single 16-bit value for each of the high and low interrupt thresholds, the Byte protocol should not be used to write to these registers. Any values transferred by the Byte protocol with the MSB set would be interpreted as the COMMAND field and stored as an address for subsequent read/write operations and not as the interrupt threshold information as desired. The Write Word protocol should be used to write byte-paired registers. For example, the THLLOW and THLHIGH registers (as well as the THHLOW and THHHIGH registers) can be written together to set the 16-bit ADC value in a single transaction.

## Analog Register (07h)

The Analog Register provides eight bits of control to the analog block. These bits control the analog gain settings of the device.

**Figure 23:**
**Analog Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | GAIN | |

| Field | Bits | Description (Reset = 00h) | |
|---|---|---|---|
| Reserved | 7:2 | Reserved. Write as 0. | |
| GAIN | 1:0 | Gain Control. Sets the analog gain of the device according to the following Figure 24. | |
| | | **FIELD VALUE** | **GAIN VALUE** |
| | | 00 | 1× |
| | | 01 | 8× |
| | | 10 | 16× |
| | | 11 | 111× |

## ID Register (12h)

The ID Register provides the value for both the part number and silicon revision number for that part number. It is a read-only register whose value never changes.

**Figure 24:**
**ID Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PARTNO | | | | REVNO | | | |

| Field | Bits | Description |
|---|---|---|
| PARTNO | 7:4 | Part Number Identification: field value 1001b |
| REVNO | 3:0 | Revision number identification |

## ADC Channel Data Registers (14h-17h)

The ADC Channel data are expressed as 16-bit values spread across two registers. The ADC Channel 0 data registers, DATA0LOW and DATA0HIGH provide the lower and upper bytes, respectively, of the ADC value of Channel 0. Registers DATA1LOW and DATA1HIGH provide the lower and upper bytes, respectively, of the ADC value of Channel 1. All Channel data registers are read-only and default to 00h on power up.

**Figure 25:**
**ADC Channel Data Registers**

| Register | Address | Bits | Description |
|---|---|---|---|
| DATA0LOW | 14h | 7:0 | ADC Channel 0 lower byte |
| DATA0HIGH | 15h | 7:0 | ADC Channel 0 upper byte |
| DATA1LOW | 16h | 7:0 | ADC Channel 1 lower byte |
| DATA1HIGH | 17h | 7:0 | ADC Channel 1 upper byte |

**Note(s):**

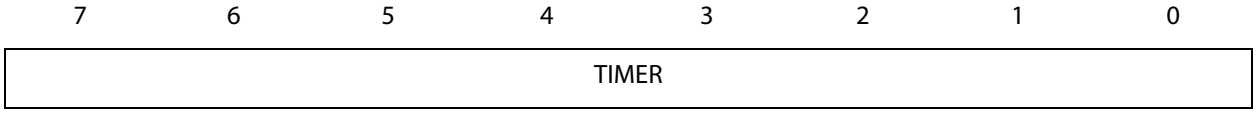
1. The Read Word protocol can be used to read byte-paired registers. For example, the DATA0LOW and DATA0HIGH registers (as well as the DATA1LOW and DATA1HIGH registers) may be read together to obtain the 16-bit ADC value in a single transaction.

The upper byte data registers can only be read following a read to the corresponding lower byte register. When the lower byte register is read, the upper eight bits are strobed into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

## Manual Integration Timer Registers (18h-19h)

The Manual Integration Timer Registers provide the number of cycles in 10.9 µs increments that occurred during a manual start/stop integration period. The timer is expressed as a 16-bit value across two registers. See CONTROL and TIMING Registers for further instructions in configuring a manual integration. The maximum time that can be derived without an overflow is 714.3ms.

**Figure 26:**
**Manual Integration Timer Registers**

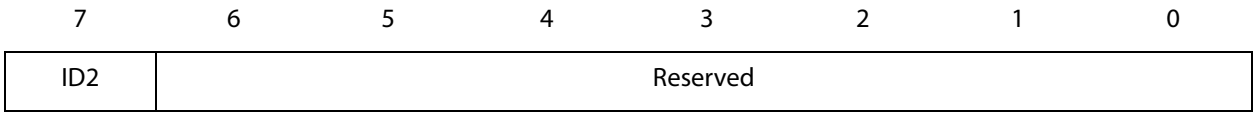



| Register | Address | Bits | Description (Reset = 00h) |
|---|---|---|---|
| TIMERLOW | 18h | 7:0 | Manual Integration Timer lower byte |
| TIMERHIGH | 19h | 7:0 | Manual Integration Timer upper byte |

## ID2 Register (1Eh)

The ID2 Register provides the means to identify the device as TSL2584TSV. Although this is a W/R register, it is strongly advised that this register not be written to. Any value written to this register could adversely affect the performance of the device.

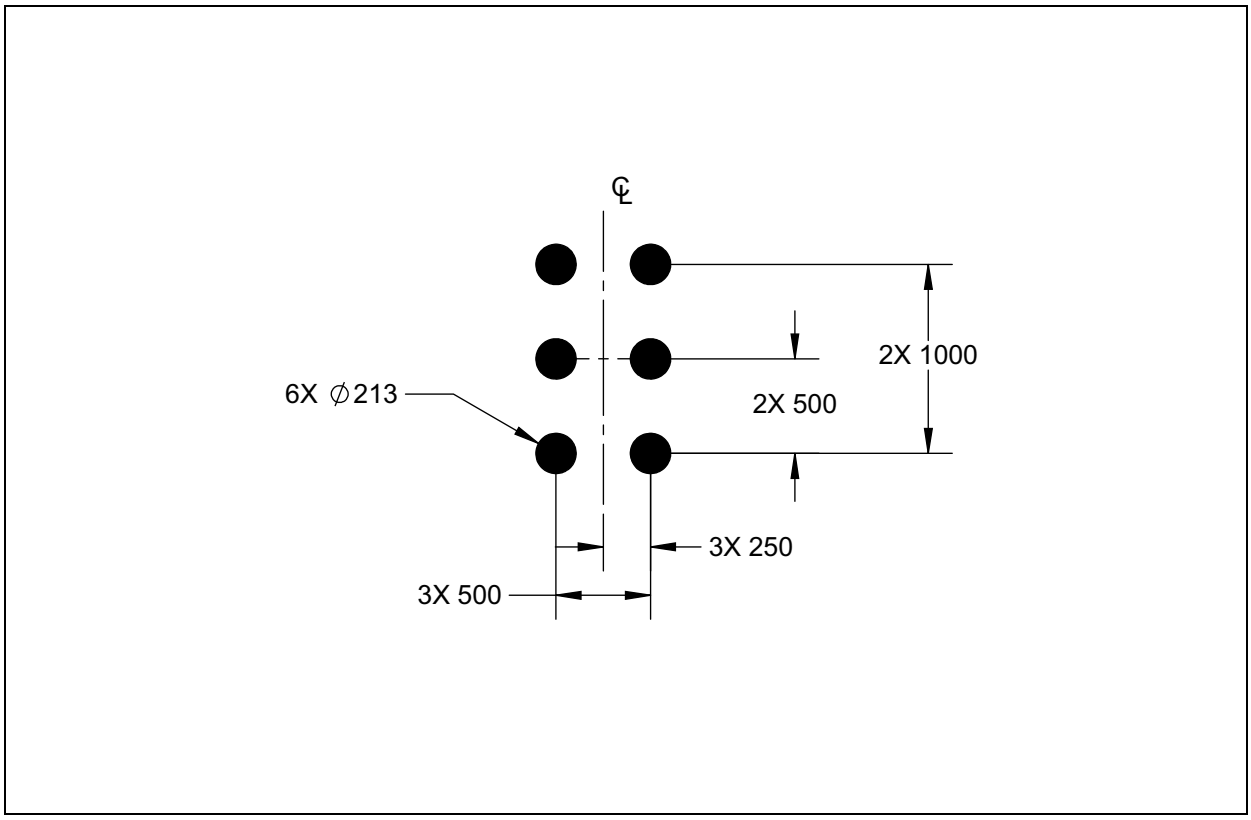
**Figure 27:**
**ID2 Register**




| Field | Bits | Description |
|---|---|---|
| ID2 | 7 | This bit will be set (1) for all TSL2584TSV devices |
| Reserved | 6:0 | Reserved |

# PCB Pad Layout

**Figure 28:**
**Suggested TSV Package PCB Layout**

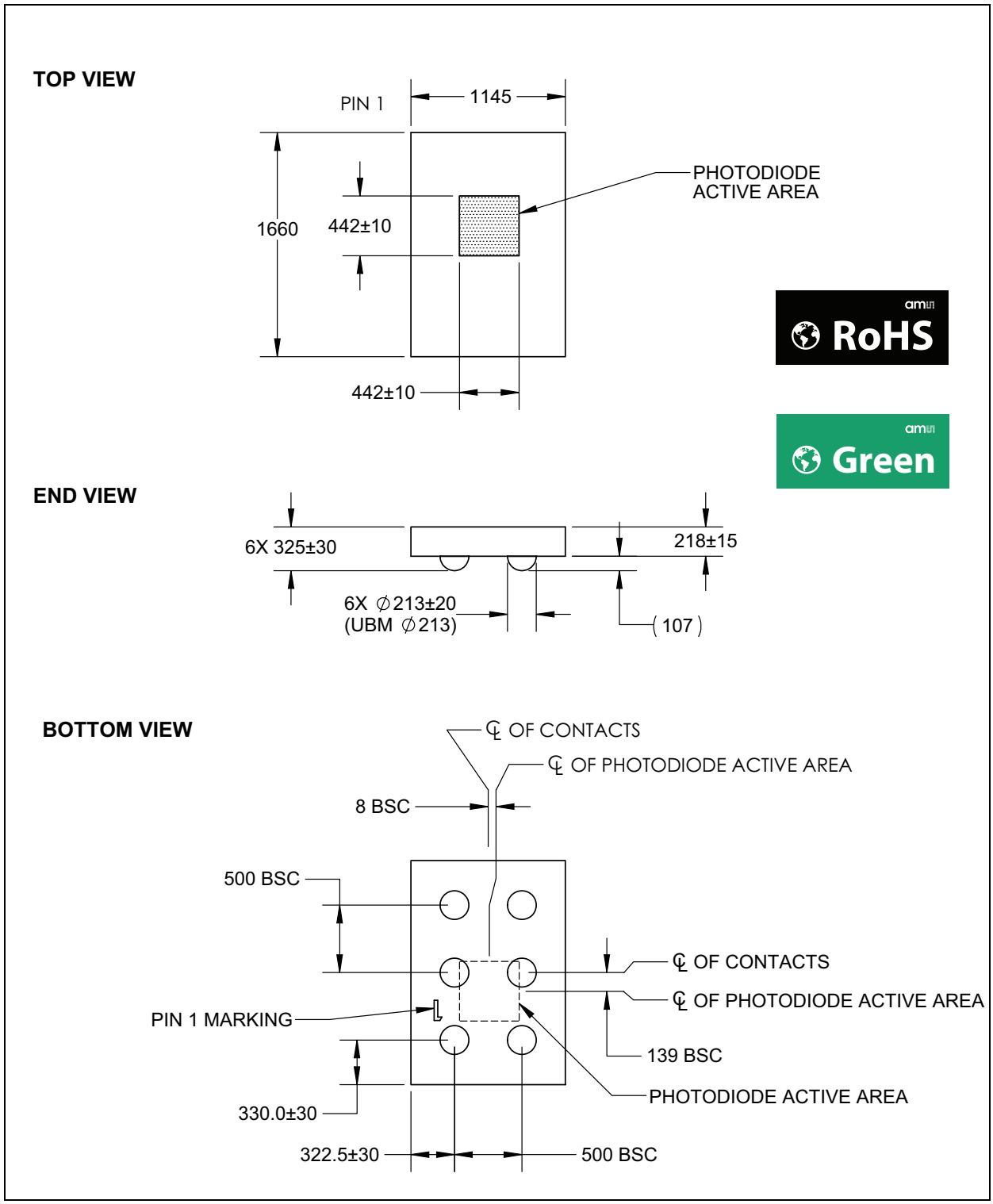



**Note(s):**

1. All linear dimensions are in microns.

## Package Drawings & Markings

**Figure 29:**
**Package TSV - Six-Lead Chipscale Packing Configuration**

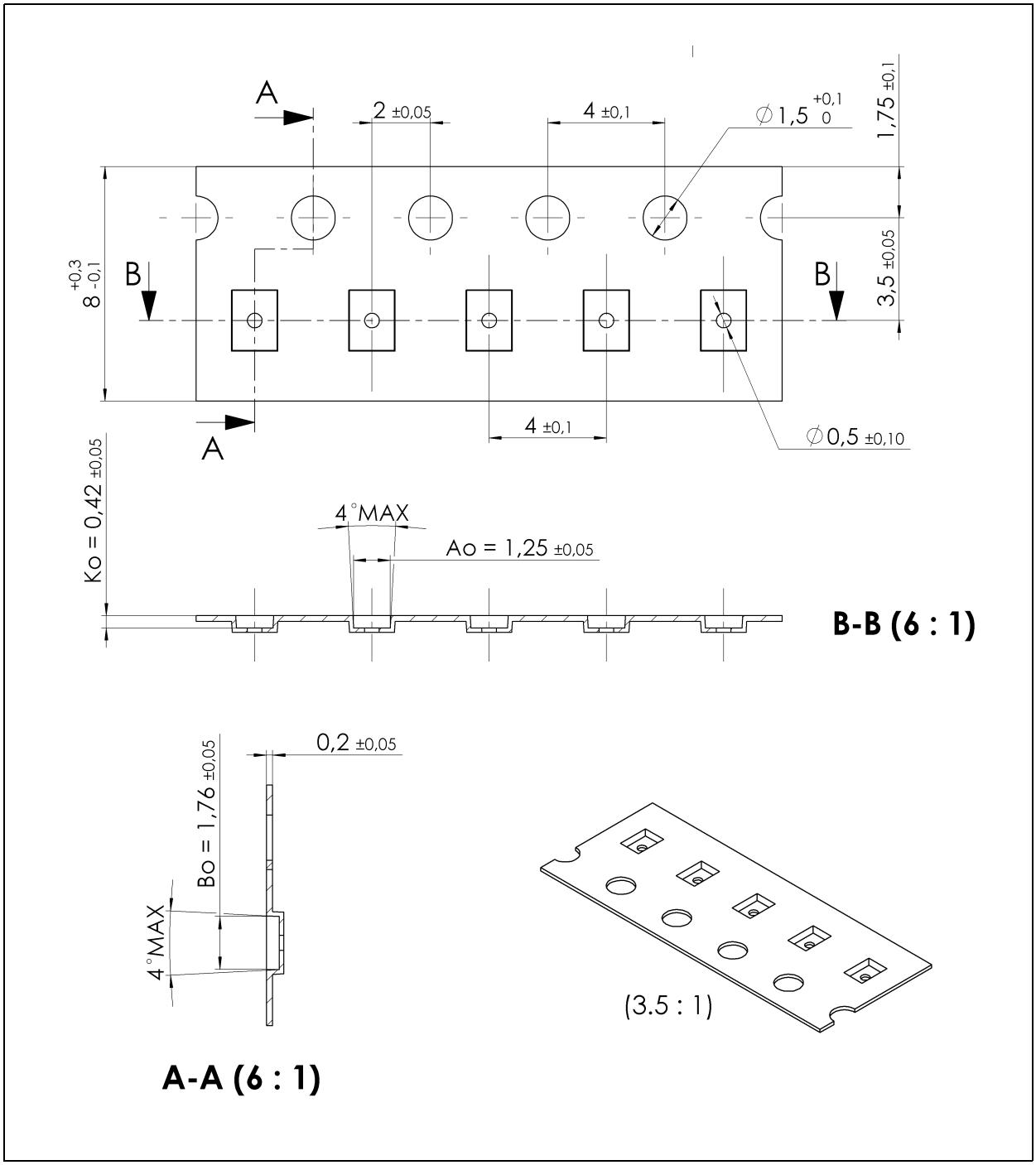



**Note(s):**

1. Dimensions are in microns.
2. Dimension tolerance is ±25µm unless otherwise noted.
3. This drawing is subject to change without notice.
4. UBM (under ball metalization) is Ø 213µm.

# Tape & Reel Information

**Figure 30:**
**TSL2584TSV – Carrier Tape & Reel Information**




**Note(s):**

1. All linear dimensions are in millimeters.
2. The dimensions in this drawing are for illustration purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing $A_0$, $B_0$, and $K_0$ are defined in ANSI EIA standard 481-B 2001.
4. Each reel is 178 millimeters in diameter and contains either 1000 or 5000 parts.
5. Packaging tape and reel conform to the requirements of EIA 481-B.
6. In accordance with EIA standard, device pin1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.