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TSL2591

Light-to-Digital Converter

General Description

The TSL2591 is a very-high sensitivity light-to-digital converter that transforms light intensity into a digital signal output capable of direct I²C interface. The device combines one broadband photodiode (visible plus infrared) and one infrared-responding photodiode on a single CMOS integrated circuit. Two integrating ADCs convert the photodiode currents into a digital output that represents the irradiance measured on each channel. This digital output can be input to a microprocessor where illuminance (ambient light level) in lux is derived using an empirical formula to approximate the human eye response. The TSL2591 supports a traditional level style interrupt that remains asserted until the firmware clears it.

Ordering Information and Content Guide appear at end of datasheet.

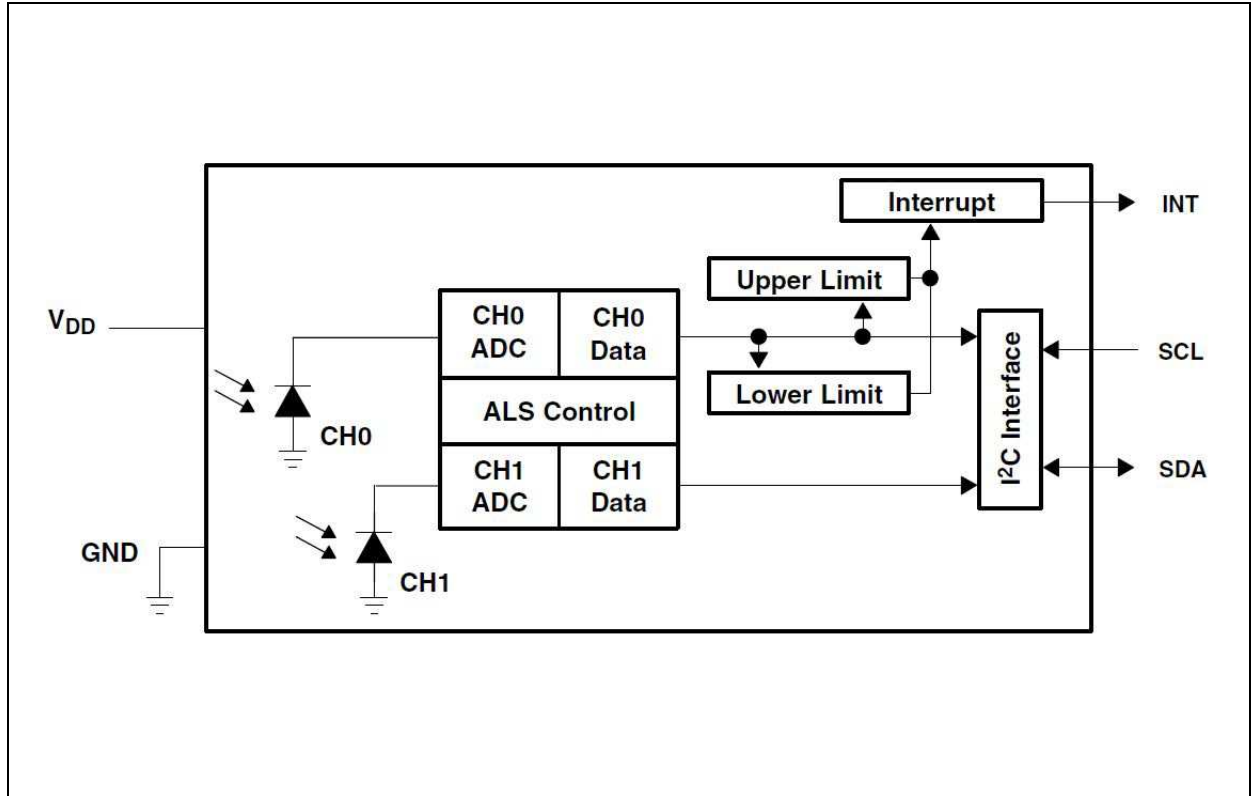
Figure 1:
Added Value of Using TSL2591

| Benefits | Features |
|---|---|
| <ul style="list-style-type: none"> • Approximates Human Eye Response | <ul style="list-style-type: none"> • Dual Diode |
| <ul style="list-style-type: none"> • Flexible Operation | <ul style="list-style-type: none"> • Programmable Analog Gain and Integration Time |
| <ul style="list-style-type: none"> • Suited for Operation Behind Dark Glass | <ul style="list-style-type: none"> • 600M:1 Dynamic Range |
| <ul style="list-style-type: none"> • Low Operating Overhead | <ul style="list-style-type: none"> • Two Internal Interrupt Sources • Programmable Upper and Lower Thresholds • One Interrupt Includes Programmable Persistence Filter |
| <ul style="list-style-type: none"> • Low Power 3.0 μA Sleep State | <ul style="list-style-type: none"> • User Selectable Sleep Mode |
| <ul style="list-style-type: none"> • I²C Fast Mode Compatible Interface | <ul style="list-style-type: none"> • Data Rates up to 400 kbit/s • Input Voltage Levels Compatible with 3.0V Bus |

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Block Diagram



Detailed Description

The TSL2591 contains two integrating analog-to-digital converters (ADC) that integrate currents from two photodiodes. Integration of both channels occurs simultaneously. Upon completion of the conversion cycle, the conversion result is transferred to the Channel 0 and Channel 1 data registers, respectively. The transfers are double-buffered to ensure that the integrity of the data is maintained. After the transfer, the device automatically begins the next integration cycle.

Communication with the device is accomplished through a standard, two-wire I²C serial bus. Consequently, the TSL2591 can be easily connected to a microcontroller or embedded controller. No external circuitry is required for signal conditioning. Because the output of the device is digital, the output is effectively immune to noise when compared to an analog signal.

The TSL2591 also supports an interrupt feature that simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity value. The primary purpose of the interrupt function is to detect a meaningful change in light intensity. The concept of a meaningful change can be defined by the user both in terms of light intensity and time, or persistence, of that change in intensity. The device has the ability to define two sets of thresholds, both above and below the current light level. An interrupt is generated when the value of a conversion exceeds either of these limits. One set of thresholds can be configured to trigger an interrupt only when the ambient light exceeds them for a configurable amount of time (persistence) while the other set can be configured to trigger an immediate interrupt.

Pin Assignment

The TSL2591 pin assignments are described below.

Figure 3:
Pin Diagram

Package FN Dual Flat No-Lead (Top View): Package drawing is not to scale.

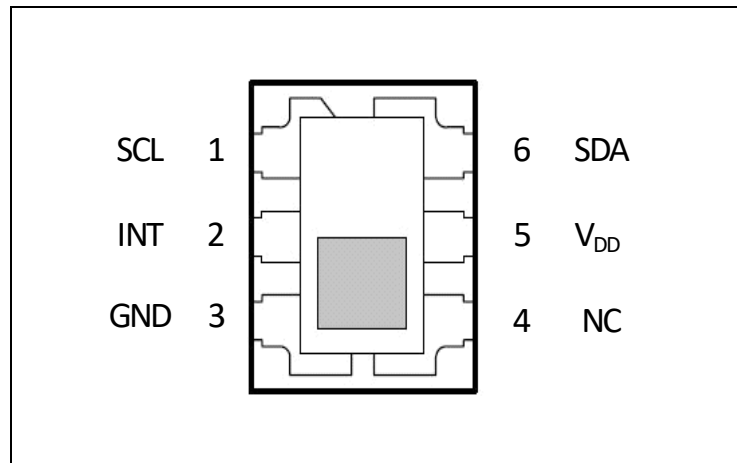


Figure 4:
Pin Description

| Pin Number | Pin Name | Description |
|------------|-----------------|--|
| 1 | SCL | I ² C serial clock input terminal |
| 2 | INT | Interrupt — open drain output (active low). |
| 3 | GND | Power supply ground. All voltages are referenced to GND. |
| 4 | NC | No connect — do not connect. |
| 5 | V _{DD} | Supply voltage |
| 6 | SDA | I ² C serial data I/O terminal |

Absolute Maximum Ratings

Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

| Parameter | Min | Max | Units | Comments |
|--|-------|-----|-------|--------------------------------------|
| Supply voltage, V_{DD} | | 3.8 | V | All voltages are with respect to GND |
| Input terminal voltage | -0.5 | 3.8 | V | |
| Output terminal voltage | -0.5 | 3.8 | V | |
| Output terminal current | -1 | 20 | mA | |
| Storage temperature range, T_{stg} | -40 | 85 | °C | |
| ESD tolerance, human body model | ±2000 | | V | JESD22-A114-B |
| ESD tolerance, charge device model (CDM) | ±500 | | V | JESD22-C101 |

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. Device parameters are guaranteed at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Figure 6:
Recommended Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Units |
|----------|--------------------------------|-----|-----|-----|------------------|
| V_{DD} | Supply voltage | 2.7 | 3 | 3.6 | V |
| T_A | Operating free-air temperature | -30 | | 70 | $^\circ\text{C}$ |

Figure 7:
Operating Characteristics, $V_{DD}=3\text{V}$, $T_A=25^\circ\text{C}$ (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|------------|-------------------------------------|--|--------------|------------|--------------|---------------|
| I_{DD} | Supply current | Active Sleep state - no I ² C activity | | 275 2.3 | 325 4 | μA |
| V_{OL} | INT, SDA output low voltage | 3mA sink current 6mA sink current | 0 0 | | 0.4 0.6 | V |
| I_{LEAK} | Leakage current, SDA, SCL, INT pins | | -5 | | 5 | μA |
| V_{IH} | SCL, SDA input high voltage | TSL25911 ($V_{bus} = V_{DD}$) | $0.7 V_{DD}$ | | | V |
| | | TSL25913 ($V_{bus} = 1.8$) | 1.26 | | | |
| V_{IL} | SCL, SDA input low voltage | TSL25911 ($V_{bus} = V_{DD}$) | | | $0.3 V_{DD}$ | V |
| | | TSL25913 ($V_{bus} = 1.8$) | | | 0.54 | |

Figure 8:

ALS Characteristics, $V_{DD}=3V$, $T_A=25^\circ C$, AGAIN = High, AEN=1, (unless otherwise noted)^{(1) (2) (3)}

| Parameter | Conditions | Channel | Min | Typ | Max | Units |
|--|---|------------|--------|----------------|----------|-----------------------------|
| Dark ADC count value | $E_e = 0$, AGAIN = Max, ATIME=000b (100ms) | CH0 CH1 | 0 0 | | 20 20 | counts |
| ADC integration time step size | ATIME = 000b (100ms) | | 95 | 100 | 105 | ms |
| ADC number of integration steps ⁽⁴⁾ | | | 1 | | 6 | steps |
| Max ADC count | ATIME = 000b (100ms) | | 0 | | 36863 | counts |
| Max ADC count | ATIME = 001b (200ms), 010b (300ms), 011b (400ms), 100b (500ms), 101b (600ms) | | 0 | | 65535 | counts |
| ADC count value | White light ⁽²⁾ $E_e = 4.98 \mu W/cm^2$ ATIME = 000b (100 ms) | CH0 CH1 | 1120 | 1315 174 | 1510 | counts |
| | $\lambda_p = 850 \text{ nm}$ ⁽³⁾ $E_e = 5.62 \mu W/cm^2$, ATIME = 000b (100 ms) | CH0 CH1 | 1230 | 1447 866 | 1665 | counts |
| ADC count value ratio: CH1/CH0 | White light ⁽²⁾ | | 0.092 | 0.132 | 0.172 | |
| | $\lambda_p = 850 \text{ nm}$ ⁽³⁾ | | 0.558 | 0.598 | 0.638 | |
| R_e Irradiance responsivity | White light ⁽²⁾ ATIME = 000b (100 ms) | CH0 CH1 | | 264.1 34.9 | | counts/ ($\mu W/cm^2$) |
| | $\lambda_p = 850 \text{ nm}$ ⁽³⁾ ATIME = 000b (100 ms) | CH0 CH1 | | 257.5 154.1 | | |
| Noise ⁽⁴⁾ | White light ⁽²⁾ $E_e = 4.98 \mu W/cm^2$ ATIME = 000b (100 ms) | CH0 | | 1 | 2 | 1 standard deviation |

| Parameter | Conditions | Channel | Min | Typ | Max | Units |
|---|--------------|------------|--------------|--------------|---------------|-------|
| Gain scaling, relative to 1× gain setting (AGAIN = Low) | AGAIN = Med | CH0 CH1 | 22 22 | 24.5 24.5 | 27 27 | × |
| | AGAIN = High | CH0 CH1 | 360 360 | 400 400 | 440 440 | |
| | AGAIN = Max | CH0 CH1 | 8500 9100 | 9200 9900 | 9900 10700 | |

Note(s):

- Optical measurements are made using small-angle incident radiation from light-emitting diode optical sources. Visible white LEDs and infrared 850 nm LEDs are used for final product testing for compatibility with high-volume production
- The white LED irradiance is supplied by a white light-emitting diode with a nominal color temperature of 4000 K.
- The 850 nm irradiance is supplied by a GaAs light-emitting diode with the following typical characteristics: peak wavelength $\lambda_p = 850$ nm and spectral halfwidth $\Delta\lambda_{1/2} = 42$ nm.
- Parameter ensured by design and is not 100% tested.

Timing Characteristics

The timing characteristics of TSL2591 are given below.

Figure 9:
AC Electrical Characteristics, $V_{DD} = 3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

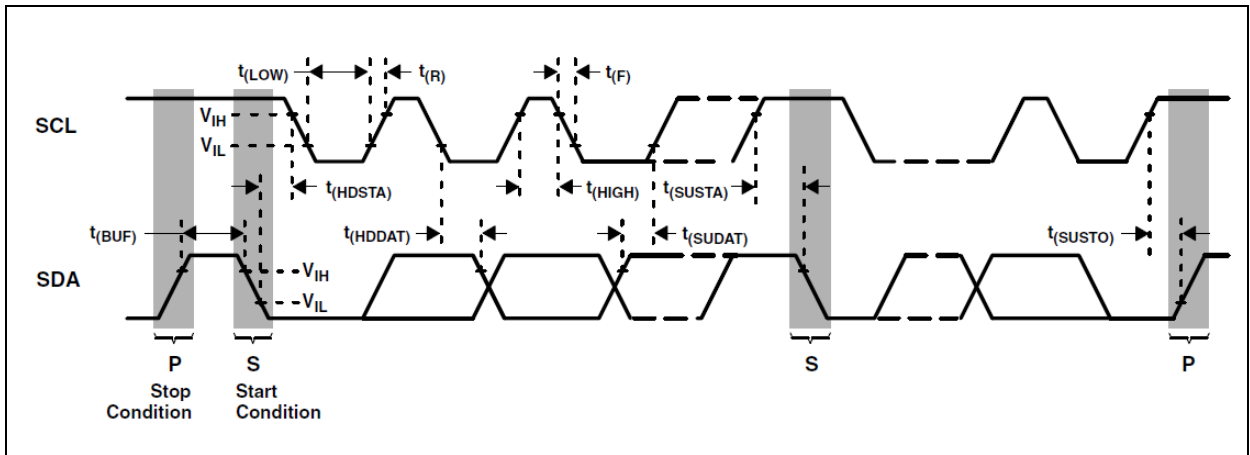
| Parameter ⁽¹⁾ | Description | Min | Typ | Max | Units |
|--------------------------|--|-----|-----|-----|---------------|
| $f_{(SCL)}$ | Clock frequency (I ² C only) | 0 | | 400 | kHz |
| $t_{(BUF)}$ | Bus free time between start and stop condition | 1.3 | | | μs |
| $t_{(HDSTA)}$ | Hold time after (repeated) start condition. After this period, the first clock is generated. | 0.6 | | | μs |
| $t_{(SUSTA)}$ | Repeated start condition setup time | 0.6 | | | μs |
| $t_{(SUSTO)}$ | Stop condition setup time | 0.6 | | | μs |
| $t_{(HDDAT)}$ | Data hold time | 0 | | | μs |
| $t_{(SUDAT)}$ | Data setup time | 100 | | | ns |
| $t_{(LOW)}$ | SCL clock low period | 1.3 | | | μs |
| $t_{(HIGH)}$ | SCL clock high period | 0.6 | | | μs |
| t_F | Clock/data fall time | | | 300 | ns |
| t_R | Clock/data rise time | | | 300 | ns |
| C_i | Input pin capacitance | | | 10 | pF |

Note(s):

1. Specified by design and characterization; not production tested.

Timing Diagrams

Figure 10:
Parameter Measurement Information



Typical Operating Characteristics

Spectral Responsivity: Two channel response allows for tunable illuminance (lux) calculation regardless of transmissivity of glass.

Figure 11: Spectral Responsivity

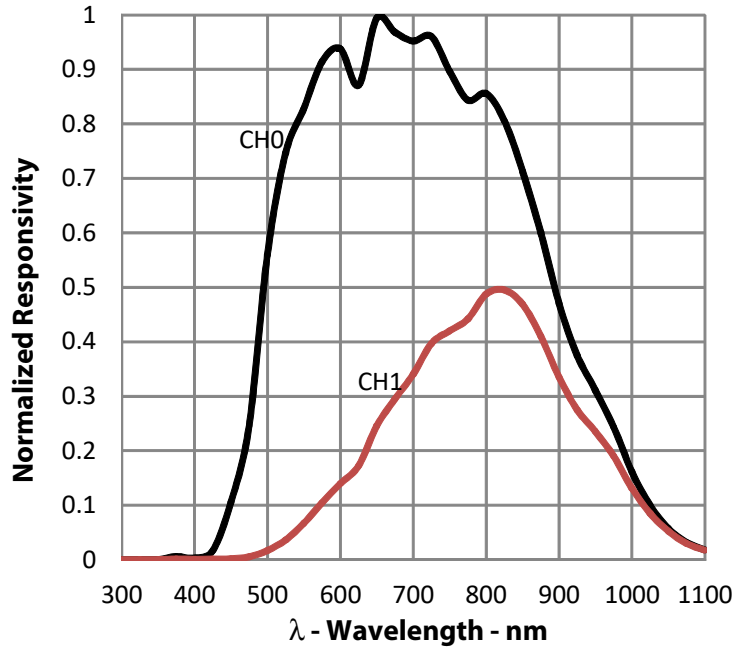
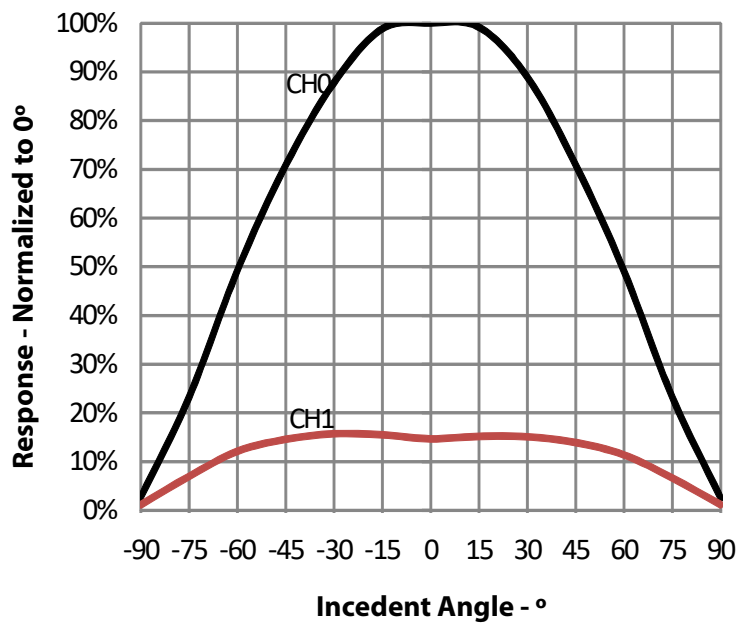


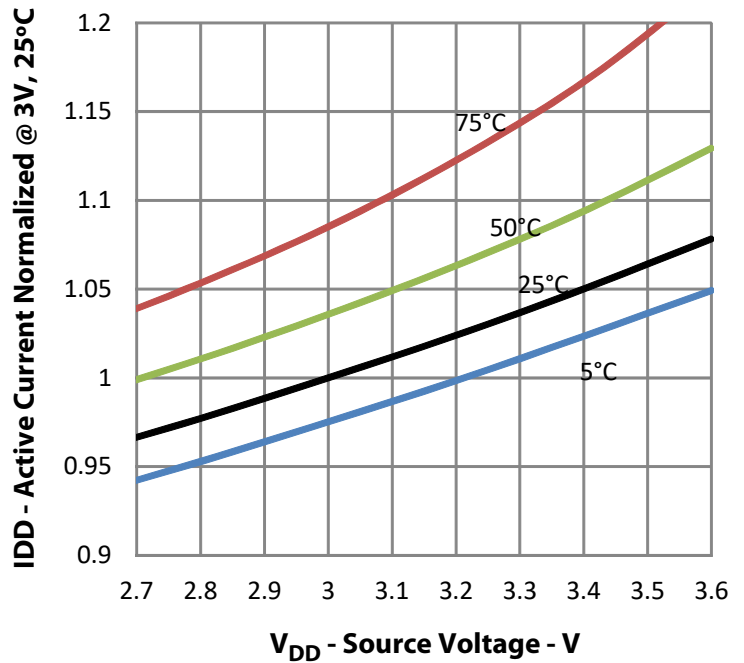
Figure 12: White Normalized Responsivity vs. Angular Displacement

White LED Angular Response: Near cosine angular response for broadband white light sources.



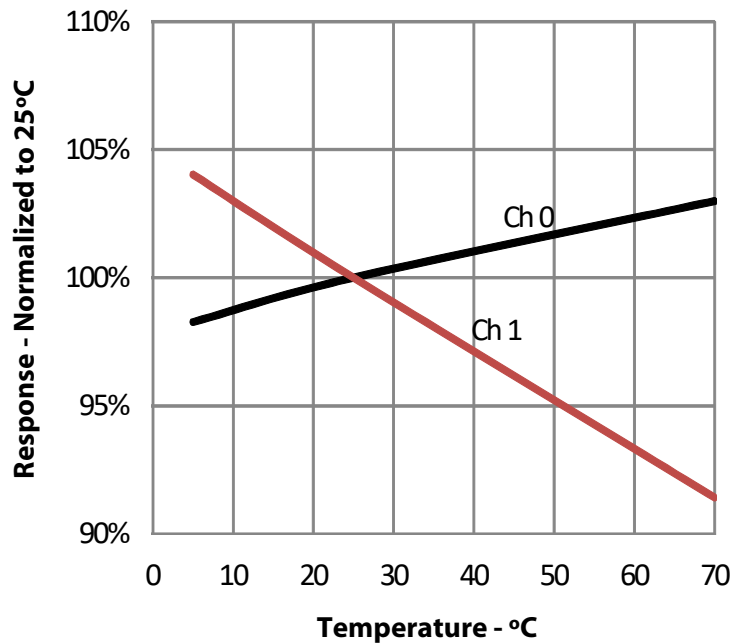
I_{DD} vs. V_{DD} and Temp: Effect of supply voltage and temperature on active current.

Figure 13:
Normalized I_{DD} vs. V_{DD} and Temperature



White LED Response vs. Temp: Effect of temperature on the device response for a broadband white light source.

Figure 14:
Response to White LED vs. Temperature



Register Description

The device is controlled and monitored by registers accessed through the I²C serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in [Figure 15](#).

Figure 15:
Register Description

| Address | Register Name | R/W | Register Function | Reset Value |
|---------|---------------|-----|---|-------------|
| -- | COMMAND | W | Specifies Register Address | 0x00 |
| 0x00 | ENABLE | R/W | Enables states and interrupts | 0x00 |
| 0x01 | CONFIG | R/W | ALS gain and integration time configuration | 0x00 |
| 0x04 | AILTL | R/W | ALS interrupt low threshold low byte | 0x00 |
| 0x05 | AILTH | R/W | ALS interrupt low threshold high byte | 0x00 |
| 0x06 | AIHTL | R/W | ALS interrupt high threshold low byte | 0x00 |
| 0x07 | AIHTH | R/W | ALS interrupt high threshold high byte | 0x00 |
| 0x08 | NPAILTL | R/W | No Persist ALS interrupt low threshold low byte | 0x00 |
| 0x09 | NPAILTH | R/W | No Persist ALS interrupt low threshold high byte | 0x00 |
| 0x0A | NPAIHTL | R/W | No Persist ALS interrupt high threshold low byte | 0x00 |
| 0x0B | NPAIHTH | R/W | No Persist ALS interrupt high threshold high byte | 0x00 |
| 0x0C | PERSIST | R/W | Interrupt persistence filter | 0x00 |
| 0x11 | PID | R | Package ID | -- |
| 0x12 | ID | R | Device ID | ID |
| 0x13 | STATUS | R | Device status | 0x00 |
| 0x14 | C0DATAL | R | CH0 ADC low data byte | 0x00 |
| 0x15 | C0DATAH | R | CH0 ADC high data byte | 0x00 |
| 0x16 | C1DATAL | R | CH1 ADC low data byte | 0x00 |
| 0x17 | C1DATAH | R | CH1 ADC high data byte | 0x00 |

Note(s):

1. Devices with a primary I²C address of 0x29 also have a secondary I²C address of 0x28 that can be used for read only registers to quickly read in a single block I²C transaction.

Command Register

The COMMAND register specifies the address of the target register for future read and write operations, as well as issues special function commands.

| | | | | | | | |
|-----|-------------|---|---------|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMD | TRANSACTION | | ADDR/SF | | | | |

| Fields | Bits | Description | | | | | | | | | | | | |
|--|--|--|---|-------------|-------|-------------------------------------|-------|----------------------|-------|---|-------|--|-------|-------------------------|
| CMD | 7 | Select Command Register. Must write as 1 when addressing COMMAND register. | | | | | | | | | | | | |
| TRANSACTION | 6:5 | Select type of transaction to follow in subsequent data transfers | | | | | | | | | | | | |
| | | <table border="1"> <thead> <tr> <th>FIELD VALUE</th> <th>DESCRIPTION</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>Reserved - Do not use</td> </tr> <tr> <td>01</td> <td>Normal Operation</td> </tr> <tr> <td>10</td> <td>Reserved – Do not use</td> </tr> <tr> <td>11</td> <td>Special Function – See description below</td> </tr> </tbody> </table> | FIELD VALUE | DESCRIPTION | 00 | Reserved - Do not use | 01 | Normal Operation | 10 | Reserved – Do not use | 11 | Special Function – See description below | | |
| | | FIELD VALUE | DESCRIPTION | | | | | | | | | | | |
| | | 00 | Reserved - Do not use | | | | | | | | | | | |
| | | 01 | Normal Operation | | | | | | | | | | | |
| 10 | Reserved – Do not use | | | | | | | | | | | | | |
| 11 | Special Function – See description below | | | | | | | | | | | | | |
| ADDR/SF | 4:0 | Address field/special function field. Depending on the transaction type, see above, this field either specifies a special function command or selects the specific control-status-data register for subsequent read and write transactions. The field values listed below apply only to special function commands. | | | | | | | | | | | | |
| | | <table border="1"> <thead> <tr> <th>FIELD VALUE</th> <th>DESCRIPTION</th> </tr> </thead> <tbody> <tr> <td>00100</td> <td>Interrupt set – forces an interrupt</td> </tr> <tr> <td>00110</td> <td>Clears ALS interrupt</td> </tr> <tr> <td>00111</td> <td>Clears ALS and no persist ALS interrupt</td> </tr> <tr> <td>01010</td> <td>Clears no persist ALS interrupt</td> </tr> <tr> <td>other</td> <td>Reserved – Do not write</td> </tr> </tbody> </table> | FIELD VALUE | DESCRIPTION | 00100 | Interrupt set – forces an interrupt | 00110 | Clears ALS interrupt | 00111 | Clears ALS and no persist ALS interrupt | 01010 | Clears no persist ALS interrupt | other | Reserved – Do not write |
| | | FIELD VALUE | DESCRIPTION | | | | | | | | | | | |
| | | 00100 | Interrupt set – forces an interrupt | | | | | | | | | | | |
| | | 00110 | Clears ALS interrupt | | | | | | | | | | | |
| | | 00111 | Clears ALS and no persist ALS interrupt | | | | | | | | | | | |
| | | 01010 | Clears no persist ALS interrupt | | | | | | | | | | | |
| other | Reserved – Do not write | | | | | | | | | | | | | |
| The interrupt set special function command sets the interrupt bits in the status register (0x13). For the interrupt to be visible on the INT pin, one of the interrupt enable bits in the enable register (0x00) must be asserted. | | | | | | | | | | | | | | |
| The interrupt set special function must be cleared with an interrupt clear special function. The ALS interrupt clear special functions clear any pending interrupt(s) and are self-clearing. | | | | | | | | | | | | | | |

Enable Register (0x00)

The ENABLE register is used to power the device on/off, enable functions and interrupts.

| | | | | | | | |
|-------|-----|----------|------|----------|---|-----|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NPIEN | SAI | Reserved | AIEN | Reserved | | AEN | PON |

| Fields | Bits | Description |
|----------|------|--|
| NPIEN | 7 | No Persist Interrupt Enable. When asserted NP Threshold conditions will generate an interrupt, bypassing the persist filter. |
| SAI | 6 | Sleep after interrupt. When asserted, the device will power down at the end of an ALS cycle if an interrupt has been generated. |
| Reserved | 5 | Reserved. Write as 0. |
| AIEN | 4 | ALS Interrupt Enable. When asserted permits ALS interrupts to be generated, subject to the persist filter. |
| Reserved | 3:2 | Reserved. Write as 0. |
| AEN | 1 | ALS Enable. This field activates ALS function. Writing a one activates the ALS. Writing a zero disables the ALS. |
| PON | 0 | Power ON. This field activates the internal oscillator to permit the timers and ADC channels to operate. Writing a one activates the oscillator. Writing a zero disables the oscillator. |

Control Register (0x01)

The CONTROL register is used to configure the ALS gain and integration time. In addition, a system reset is provided. Upon power up, the CONTROL register resets to 0x00.

| | | | | | | | |
|--------|----------|-------|----------|-------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SRESET | Reserved | AGAIN | Reserved | ATIME | | | |

| Fields | Bits | Description | | |
|----------|------|---|------------------|-----------|
| SRESET | 7 | System reset. When asserted, the device will reset equivalent to a power-on reset. SRESET is self-clearing. | | |
| Reserved | 6 | Reserved. Write as 0. | | |
| AGAIN | 5:4 | ALS gain sets the gain of the internal integration amplifiers for both photodiode channels. | | |
| | | FIELD VALUE | DESCRIPTION | |
| | | 00 | Low gain mode | |
| | | 01 | Medium gain mode | |
| | | 10 | High gain mode | |
| Reserved | 3 | Reserved. Write as 0. | | |
| | | ALS time sets the internal ADC integration time for both photodiode channels. | | |
| | | FIELD VALUE | INTEGRATION TIME | MAX COUNT |
| ATIME | 2:0 | 000 | 100 ms | 36863 |
| | | 001 | 200 ms | 65535 |
| | | 010 | 300 ms | 65535 |
| | | 011 | 400 ms | 65535 |
| | | 100 | 500 ms | 65535 |
| | | 101 | 600 ms | 65535 |

ALS Interrupt Threshold Register (0x04 – 0x0B)

The ALS interrupt threshold registers provide the values to be used as the high and low trigger points for the comparison function for interrupt generation. If C0DATA crosses below the low threshold specified, or above the higher threshold, an interrupt is asserted on the interrupt pin.

If the C0DATA exceeds the persist thresholds (registers: 0x04 – 0x07) for the number of persist cycles configured in the PERSIST register an interrupt will be triggered. If the C0DATA exceeds the no-persist thresholds (registers: 0x08 – 0x0B) an interrupt will be triggered immediately following the end of the current integration.

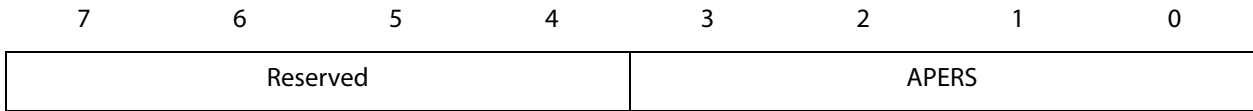
Note that while the interrupt is observable in the STATUS register (0x13), it is visible only on the INT pin when AIEN or NPIEN are enabled in the ENABLE register (0x00).

Upon power up, the interrupt threshold registers default to 0x00.

| Register | Address | Bits | Description |
|----------|---------|------|--|
| AILTL | 0x04 | 7:0 | ALS low threshold lower byte |
| AILTH | 0x05 | 7:0 | ALS low threshold upper byte |
| AIHTL | 0x06 | 7:0 | ALS high threshold lower byte |
| AIHTH | 0x07 | 7:0 | ALS high threshold upper byte |
| NPAILTL | 0x08 | 7:0 | No Persist ALS low threshold lower byte |
| NPAILTH | 0x09 | 7:0 | No Persist ALS low threshold upper byte |
| NPAIHTL | 0x0A | 7:0 | No Persist ALS high threshold lower byte |
| NPAIHTH | 0x0B | 7:0 | No Persist ALS high threshold upper byte |

PERSIST Register (0x0C)

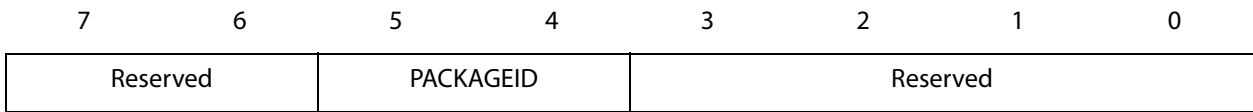
The Interrupt persistence filter sets the number of consecutive out-of-range ALS cycles necessary to generate an interrupt. Out-of-range is determined by comparing C0DATA (0x14 and 0x15) to the interrupt threshold registers (0x04 - 0x07). Note that the no-persist ALS interrupt is not affected by the interrupt persistence filter. Upon power up, the interrupt persistence filter register resets to 0x00.



| Field | Bits | Description | |
|----------|------------------------------------|----------------------------------|--|
| Reserved | 7:4 | Reserved. Write as 0. | |
| APERS | 3:0 | ALS interrupt persistence filter | |
| | | FIELD VALUE | PERSISTENCE |
| | | 0000 | Every ALS cycle generates an interrupt |
| | | 0001 | Any value outside of threshold range |
| | | 0010 | 2 consecutive values out of range |
| | | 0011 | 3 consecutive values out of range |
| | | 0100 | 5 consecutive values out of range |
| | | 0101 | 10 consecutive values out of range |
| | | 0110 | 15 consecutive values out of range |
| | | 0111 | 20 consecutive values out of range |
| | | 1000 | 25 consecutive values out of range |
| | | 1001 | 30 consecutive values out of range |
| | | 1010 | 35 consecutive values out of range |
| | | 1011 | 40 consecutive values out of range |
| | | 1100 | 45 consecutive values out of range |
| | | 1101 | 50 consecutive values out of range |
| | | 1110 | 55 consecutive values out of range |
| 1111 | 60 consecutive values out of range | | |

PID Register (0x11)

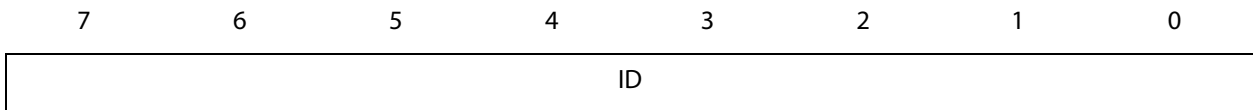
The PID register provides an identification of the devices package. This register is a read-only register whose value never changes.



| Field | Bits | Description |
|----------|------|-----------------------------|
| Reserved | 7:6 | Reserved. |
| PID | 5:4 | Package Identification = 00 |
| Reserved | 3:0 | Reserved. |

ID Register (0x12)

The ID register provides the device identification. This register is a read-only register whose value never changes.



| Field | Bits | Description |
|-------|------|------------------------------|
| ID | 7:0 | Device Identification = 0x50 |

Status Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

| | | | | | | | |
|----------|---|--------|------|----------|---|---|--------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | NPINTR | AINT | Reserved | | | AVALID |

| Field | Bits | Description |
|----------|------|--|
| Reserved | 7:6 | Reserved. Write at zero. |
| NPINTR | 5 | No-persist Interrupt. Indicates that the device has encountered a no-persist interrupt condition. |
| AINT | 4 | ALS Interrupt. Indicates that the device is asserting an ALS interrupt. |
| Reserved | 3:1 | Reserved. |
| AVALID | 0 | ALS Valid. Indicates that the ADC channels have completed an integration cycle since the AEN bit was asserted. |

ALS Data Register (0x14 - 0x17)

ALS data is stored as two 16-bit values; one for each channel. When the lower byte of either channel is read, the upper byte of the same channel is latched into a shadow register. The shadow register ensures that both bytes are the result of the same ALS integration cycle, even if additional integration cycles occur between the lower byte and upper byte register readings.

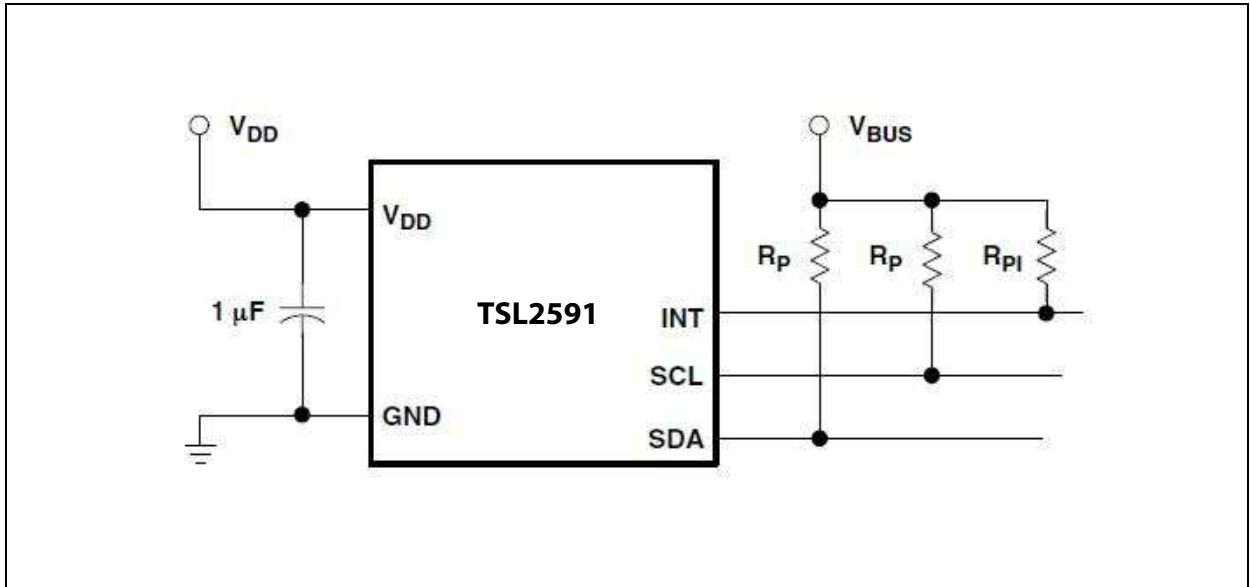
Each channel independently operates the upper byte shadow register. So to minimize the potential for skew between CH0 and CH1 data, it is recommended to read all four ADC bytes in sequence.

| Register | Address | Bits | Description |
|----------|---------|------|------------------------|
| C0DATAL | 0x14 | 7:0 | ALS CH0 data low byte |
| C0DATAH | 0x15 | 7:0 | ALS CH0 data high byte |
| C1DATAL | 0x16 | 7:0 | ALS CH1 data low byte |
| C1DATAH | 0x17 | 7:0 | ALS CH1 data high byte |

Application Information

Figure 16 shows a typical hardware application circuit. A 1- μF low-ESR decoupling capacitor should be placed as close as possible to the V_{DD} pin. V_{BUS} in this figure refers to the I²C bus voltage, which is equal to V_{DD} .

Figure 16:
Typical Application Hardware Circuit

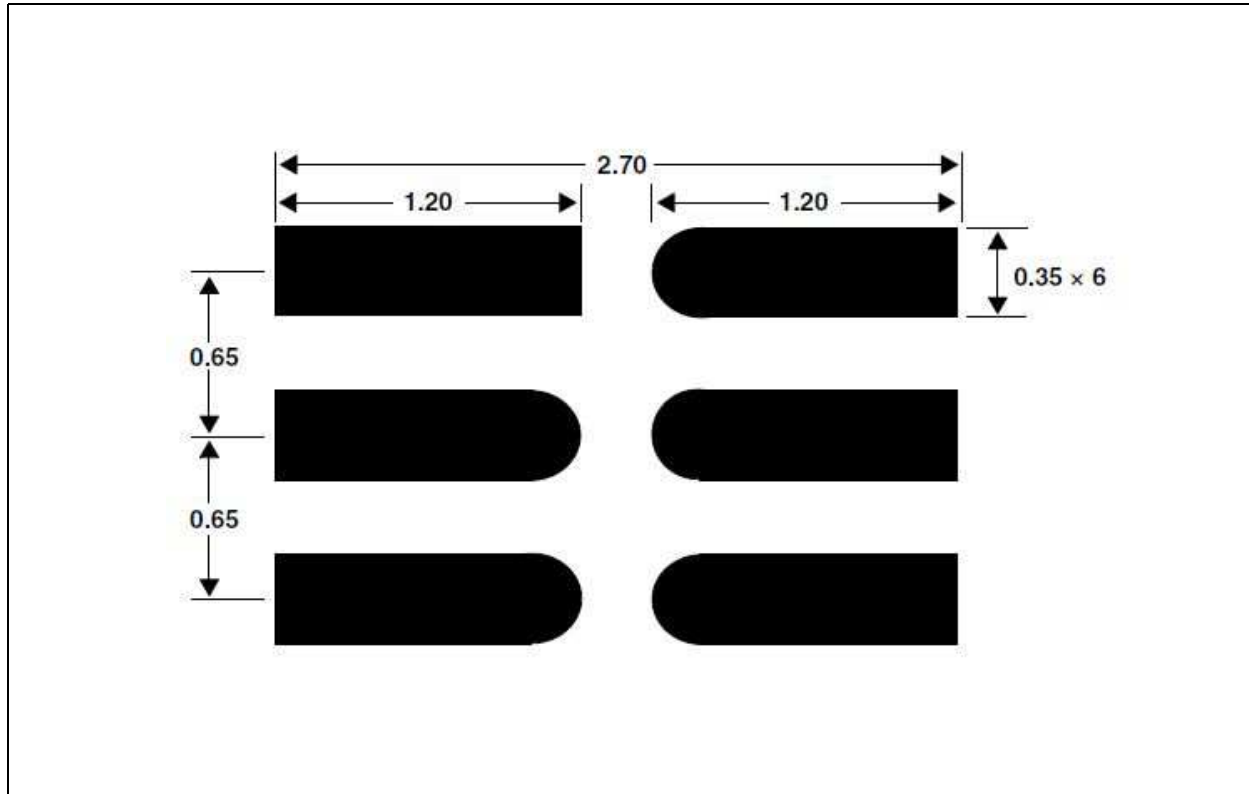


The I²C signals and the Interrupt are open-drain outputs and require pull-up resistors. The pull-up resistor (R_p) value is a function of the I²C bus speed, the I²C bus voltage, and the capacitive load. The **ams** EVM running at 400 kbps, uses 1.5-k Ω resistors. A 10-k Ω pull-up resistor (R_{pi}) can be used for the interrupt line.

PCB Pad Layout

Suggested land pattern based on the IPC-7351B Generic Requirements for Surface Mount Design and Land Pattern Standard (2010) for the small outline no-lead (SON) package is shown in [Figure 17](#).

Figure 17:
Suggested FN Package PCB Layout (Top View)

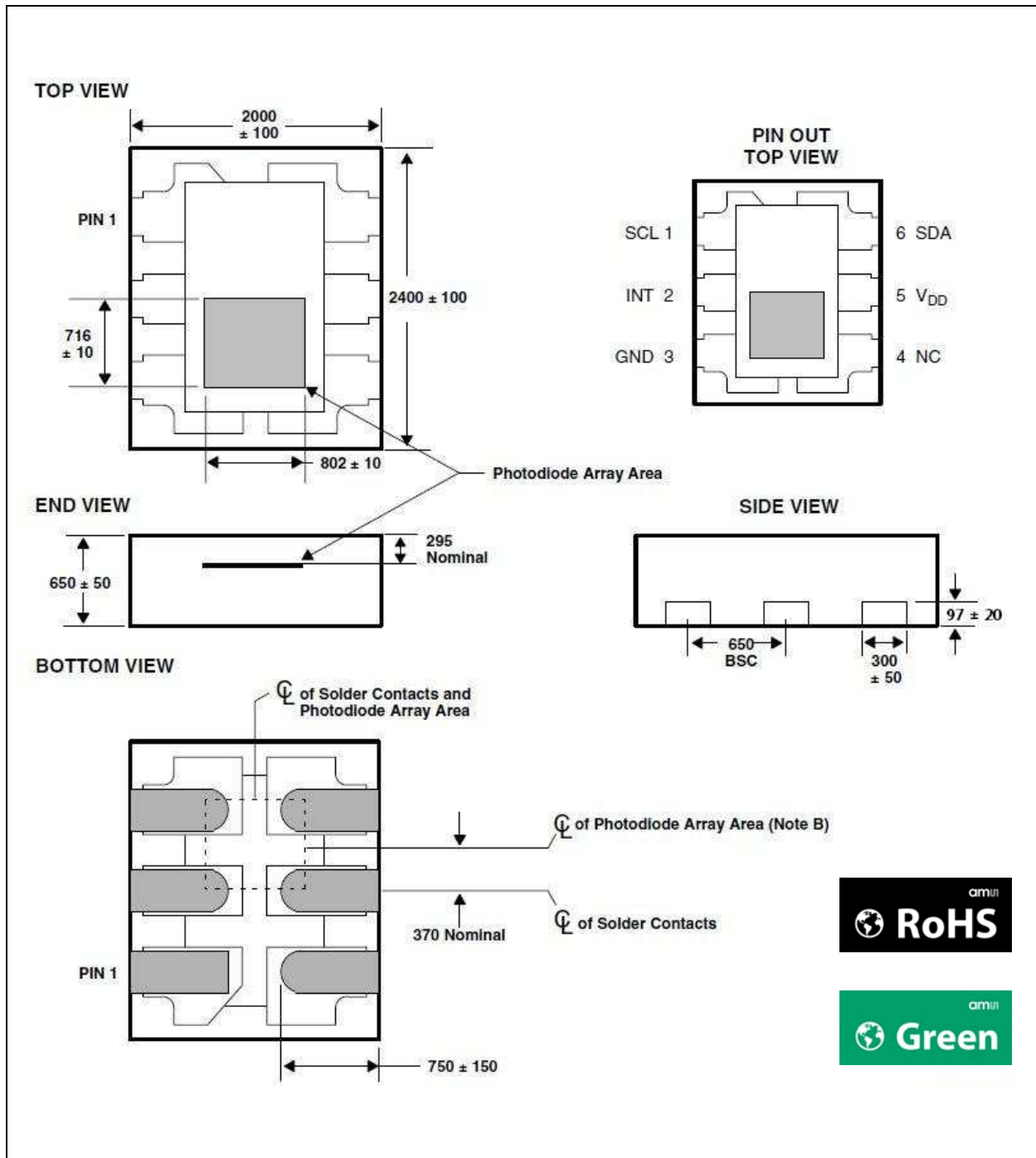


Note(s):

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

Package Drawings & Markings

Figure 18:
FN Package – Dual Flat No-Lead Packaging Configuration

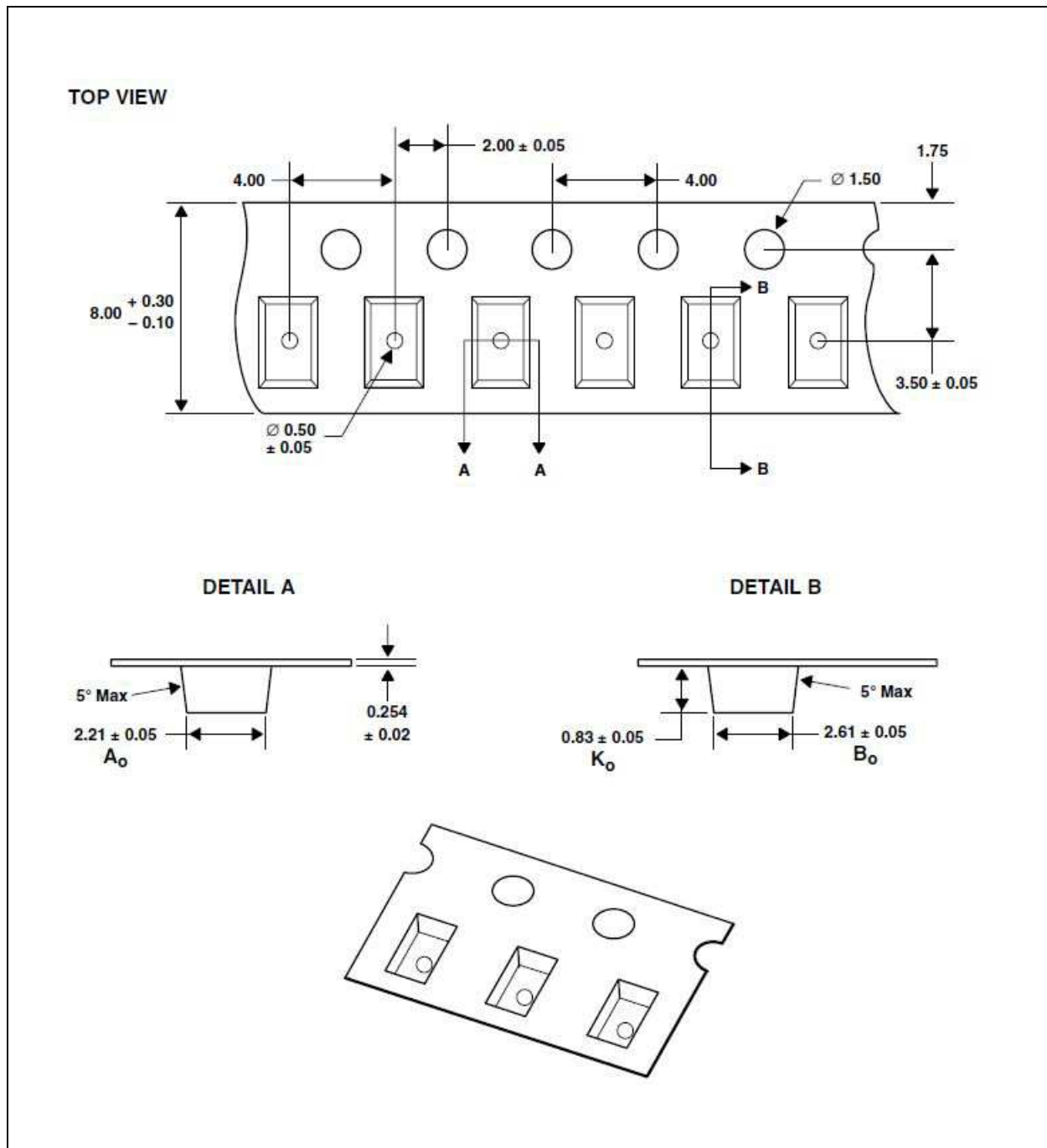


Note(s):

1. All linear dimensions are in micrometers.
2. The die is centered within the package within a tolerance of $\pm 75 \mu\text{m}$.
3. Package top surface is molded with an electrically non-conductive clear plastic compound having an index of refraction of 1.55.
4. Contact finish is copper alloy A194 with pre-plated NiPdAu lead finish.
5. This package contains no lead (Pb).
6. This drawing is subject to change without notice.

Mechanical Data

Figure 19:
FN Package Carrier Tape and Reel Information



Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing A_0 , B_0 and K_0 are defined in ANSI EIA Standard 481-B 2001.
4. Each reel is 178 millimeters in diameter and contains 3500 parts.
5. ams packaging tape and reel conform to the requirements of EIA Standard 481 - B.
6. In accordance with EIA Standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.