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TSL2740

ALS and Proximity Light-to-Digital Sensor

General Description

The TSL2740 device features advanced proximity measurement and digital ambient light sensing (ALS). The proximity detection feature provides object detection (e.g. mobile device screen to user's ear) by photodiode detection of reflected IR energy. Detect/release events are interrupt driven, and occur when proximity result crosses upper and/or lower threshold settings. The proximity engine features offset adjustment registers to compensate for unwanted IR energy reflection at the sensor. Proximity results are further improved by automatic ambient light subtraction. The ALS sensor features 2 output channels, a visible channel and an IR channel. The visible channel has a photodiode with a UV and IR blocking filter whereas the IR channel has a photodiode with an IR pass filter. Each channel has a dedicated data converter producing a 16-bit output. This architecture allows applications to accurately measure ambient light which enables devices to calculate illuminance to control a display backlight.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TSL2740, ALS and Proximity Light-to-Digital Sensor are listed below:

Figure 1:
Added Value of Using TSL2740

Benefits	Features
• Single device integrated optical solution	• 2.0mm x 2.0mm x 0.5mm • Power management features • I^2C fast mode interface compatible
• Accurate ambient light sensing	• Photopic ambient light sense (ALS) • UV / IR blocking filter • Programmable gain and integration time
• Reduced power consumption	• 1.8V power supply with 1.8V I^2C bus
• Compensates for unwanted IR system crosstalk reflection • Compensates for unwanted ambient light photodiode current	• Programmable proximity offset adjustment register • Proximity automatic ambient light subtraction

Applications

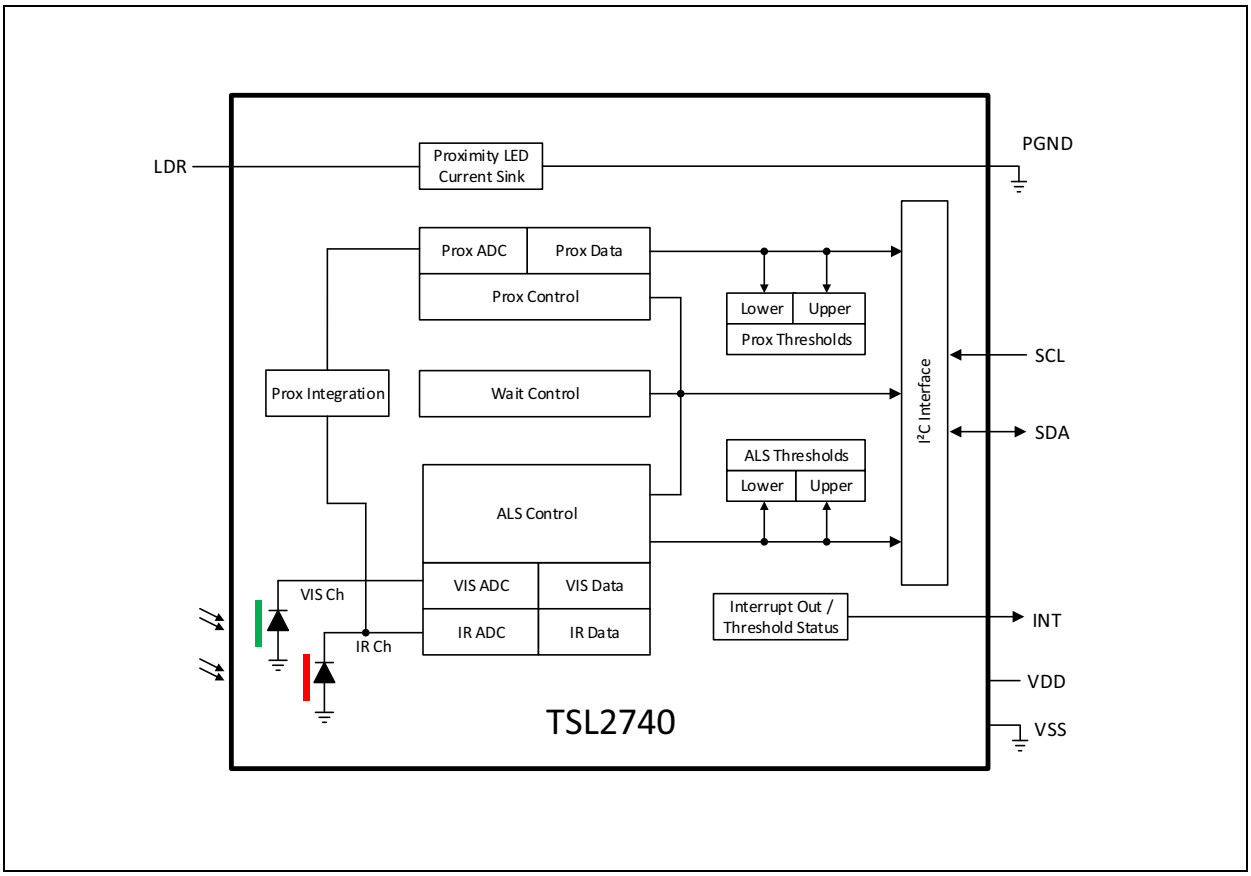
The TSL2740 applications include:

- Ambient light sensing
- Display backlight control

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of TSL2740



Pin Assignment

Figure 3:
Pin Diagram of TSL2740

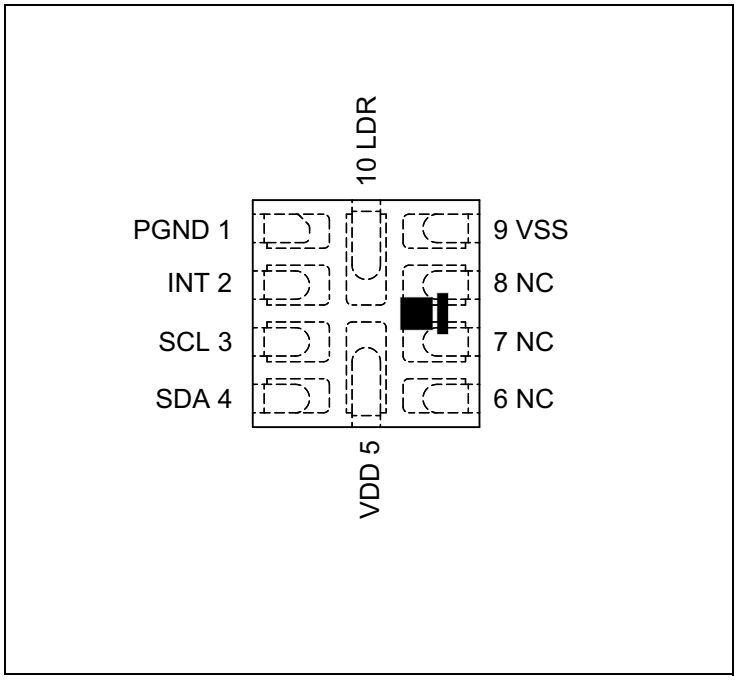


Figure 4:
Pin Description of TSL2740 (10-Pin QFN)

Pin Number	Pin Name	Description
1	PGND	Power ground
2	INT	Interrupt. Open drain output (active low)
3	SCL	I^2C serial clock input terminal
4	SDA	I^2C serial data I/O terminal
5	VDD	Supply voltage
6	NC	No connection
7	NC	No connection
8	NC	No connection
9	VSS	Ground. All voltages are referenced to VSS
10	LDR	LED drive. Current sink for LED

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
V_{DD}	Supply voltage	-0.3	2.2	V	All voltages are with respect to GND
V_{IO}	Digital I/O terminal voltage	-0.3	3.6	V	INT, SCL and SDA
I_{out}	Output terminal current	-1	20	mA	INT and SDA
T_{strg}	Storage temperature range	-40	85	°C	
I_{SCR}	Input current (latch up immunity) JEDEC JESD78D	± 100		mA	Class II
ESD_{HBM}	Electrostatic discharge HBM JS-001-2014	± 2000		V	
ESD_{CDM}	Electrostatic discharge CDM JEDEC JESD22-C101F	± 500		V	

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Supply voltage	1.7	1.8	2.0	V
	Supply voltage accuracy, V_{DD} total error including transients	-3		3	%
T_A	Operating free-air temperature (1)	-30		85	°C

Note(s):

1. While the device is operational across the temperature range, performance will vary with temperature. Specifications are stated at 25°C unless otherwise noted.

Figure 7:
Operating Characteristics, V_{DD} = 1.8V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{OSC}	Oscillator frequency			8.107		MHz
I_{DD}	Supply current	Active ALS State (PON=AEN=1) (1)	50	90	150	µA
		Idle State (PON=1,AEN=0) (2)		30	60	
		Sleep State (3)		0.7	5	
V_{OL}	INT, SDA output low voltage	6mA sink current			0.6	V
I_{LEAK}	Leakage current, INT, SCL and SDA		-5		5	µA
V_{IH}	SCL, SDA input high voltage (4)		1.26			V
V_{IL}	SCL, SDA input low voltage				0.54	V
T_{Active}	Time from power-on to ready to receive I^2C commands			1.5		ms

Note(s):

1. This parameter indicates the supply current during periods of ALS integration. If Wait is enabled (WEN=1), the supply current is lower during the Wait period.
2. Idle state occurs when PON=1 and all functions are not enabled.
3. Sleep state occurs when PON = 0 and I^2C bus is idle. If Sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.
4. Digital pins: SDA, SCL, INT, are tolerant to a communication voltage up to 3.0V.

Typical Operating Characteristics

Figure 8:
ALS Operating Characteristics, V_{DD} = 1.8V, T_A = 25°C

Parameter	Conditions	Min	Typ	Max	Units
Integration time step size		2.68	2.78	2.90	ms
Number of integration steps (1)		1		256	steps
Dark ADC count value	E_e = 0 µW/ cm^2; AGAIN = 64x; ATIME = 100ms (0x23)	0	1	3	counts
R_e Irradiance responsivity Settings: AGAIN = 16x ATIME = 400ms	**Visible Channel**				
	White LED, 2700K	309	363	417	counts/ (µW/cm^2)
	IR Channel				
	λ_D = 950 nm LED		352		counts/ (µW/cm^2)
Gain scaling, relative to 1x gain setting	AGAIN = 4x		4		x
	AGAIN = 16x		16		
	AGAIN = 64x		67		
	AGAIN = 128x		140		
ADC noise	AGAIN = 16x		0.005		% full scale

Note(s):

1. Specified by design and characterization; not production tested.

Figure 9:
Proximity Characteristics, VDD = 1.8V, T_A =25°C

Parameter	Conditions		Min	Typ	Max	Units
ADC conversion time step size				88		µs
ADC number of integration steps (1)			1		256	steps
ADC counts (1)			0		255	counts
Gain scaling, relative to 1x gain setting	PGAIN = 1 (2x)			2		x
	PGAIN = 2 (4x)			4		
	PGAIN = 3 (8x)			8		
LED pulse count (1)			1		64	pulses
LED pulse width	PPULSE_LEN = 0			4		µs
	PPULSE_LEN = 1			8		
	PPULSE_LEN = 2			16		
	PPULSE_LEN = 3			32		
LED drive current	I_{SINK} (sink current) @ 1.6 V, LDR pin	PLDRIVE = 31 (192mA)		192		mA
		PLDRIVE = 16 (102mA)	91.8	102	112.2	
		PLDRIVE = 7 (48mA)		48		
		PLDRIVE = 3 (24mA)		24		
		PLDRIVE = 1 (12mA)		12		
		PLDRIVE = 0 (6mA)		6		

Note(s):

1. Specified by design and characterization; not production tested.

Figure 10:
Spectral Responsivity

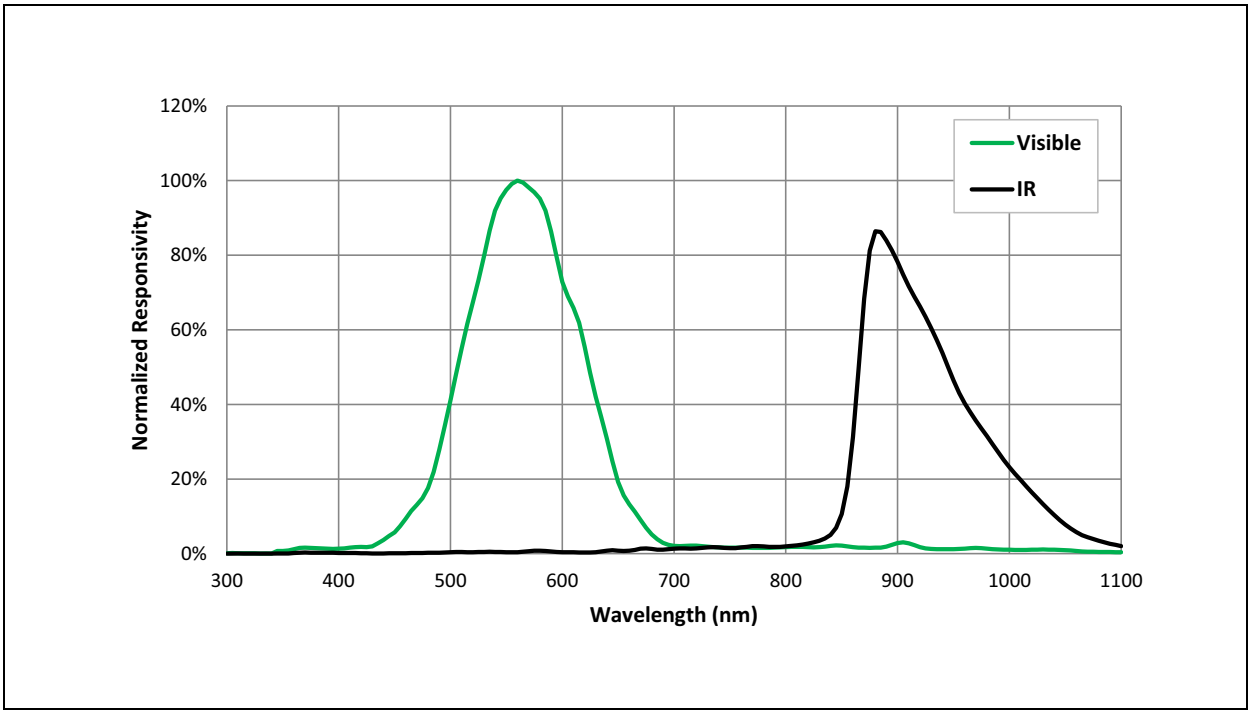


Figure 11:
ALS Responsivity vs Angular Displacement

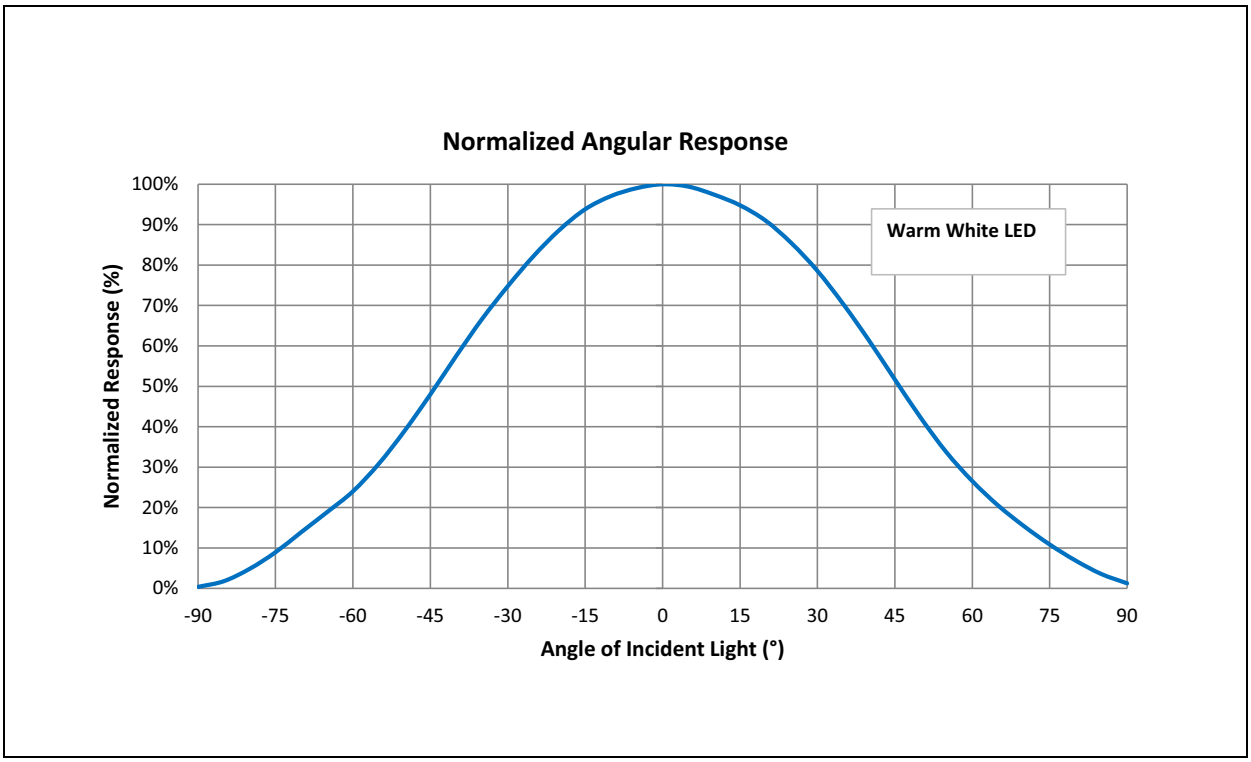
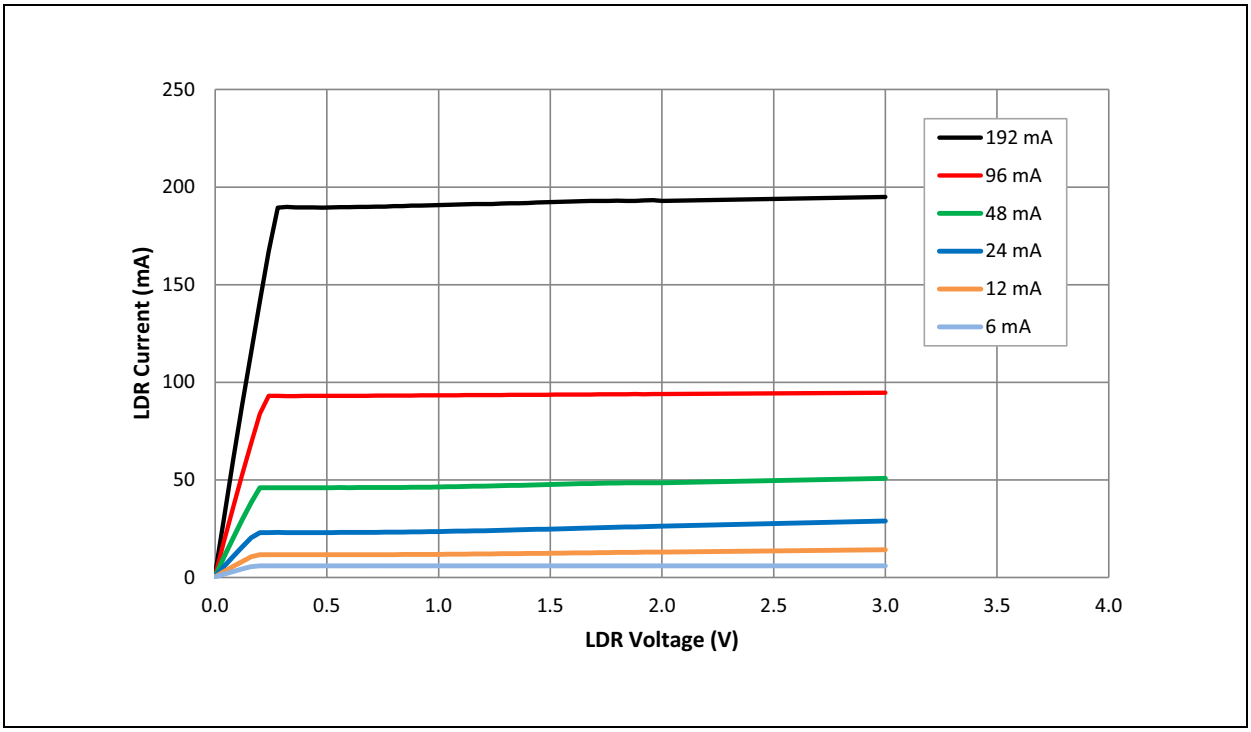


Figure 12:
Typical LDR Current vs Voltage



Detailed Description

Proximity

Proximity results are affected by three fundamental factors: the IR LED emission, IR reception, and environmental factors, including target distance and surface reflectivity.

The IR reception signal path begins with IR detection from a photodiode and ends with the 8-bit proximity result in PDATA register. Signal from the photodiode is amplified, and offset adjusted to optimize performance. Offset correction or cross-talk compensation is accomplished by adjustment to the POFFSET register.

The analog circuitry of the device applies the offset value as a subtraction to the signal accumulation; therefore a positive offset value has the effect of decreasing the results.

Ambient Light Sensing

The ALS reception signal path begins as photodiodes receive filtered light and ends with the 16-bit results in the VISDATAL/H and IRDATAL/H registers. The visible channel's photodiode is filtered with a UV and IR filter to receive only visible light. The IR channel's photodiode is filtered to receive only IR. Signals from the photodiodes simultaneously accumulate for a period of time set by the value in ATIME before the results are available. Gain is adjustable from 1x to 128x to facilitate operation over a wide range of lighting conditions. Custom Lux equations can be created for specific applications and system designs.

I^2C Characteristics

The device uses I^2C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and fast clock frequency modes with a chip address of 0x39. Read and Write transactions comply with the standard set by Philips (now NXP).

Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (i.e. valid even after the master issues a STOP command and the I^2C bus is released).

During consecutive Read transactions, the future/repeated I^2C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address + 1.

I^2C Write Transaction

A Write transaction consists of a START, CHIP-ADDRESS$_{WRITE}$, REGISTER-ADDRESS, DATA BYTE(S), and STOP. Following each byte (9^{th} clock pulse) the slave places an ACKNOWLEDGE/ NOT-ACKNOWLEDGE (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

I²C Read Transaction

A Read transaction consists of a START, CHIP-ADDRESS$_{WRITE}$, REGISTER-ADDRESS, START, CHIP-ADDRESS$_{READ}$, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

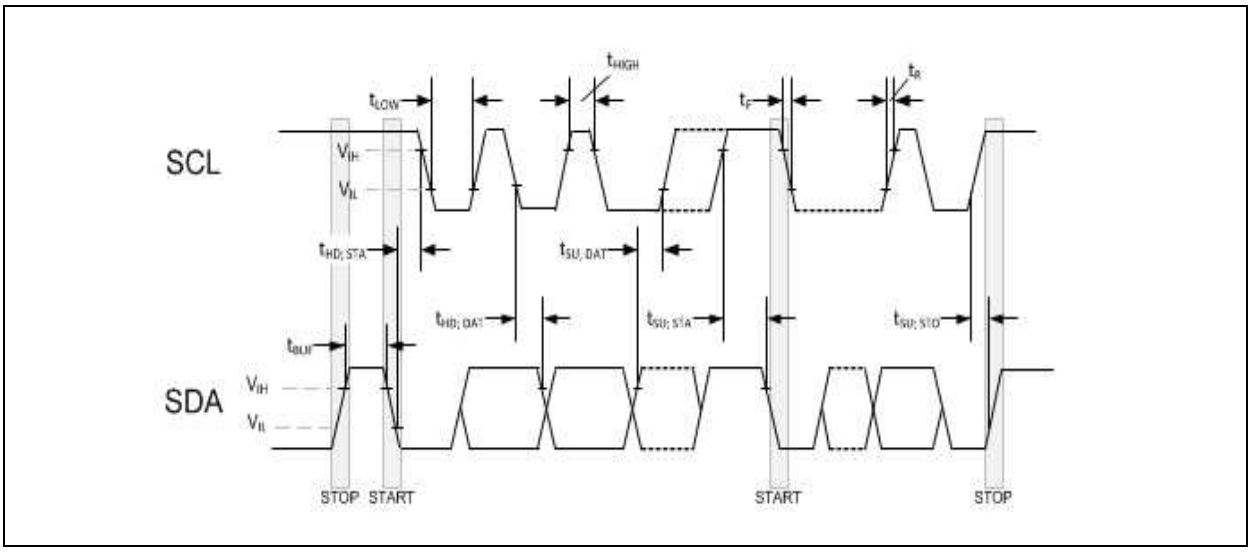
Alternately, if the previous I²C transaction was a Read, the internal register address buffer is still valid, allowing the transaction to proceed without "re"-specifying the register address. In this case the transaction consists of a START, CHIP-ADDRESS$_{READ}$, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9th clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at:

www.i2c-bus.org/references/

Timing Diagrams

Figure 13:
I²C Timing



Principles of Operation

System State Machine

An internal state machine provides system control of the ALS, proximity detection, and power management features of the device. At power up, an internal power-on-reset initializes the device and puts it in a low power Sleep state. When a write on I^2C bus to the Enable register (0x80) PON bit is set, the device transitions to the Idle state. If PON is disabled, the device will return to the Sleep state to save power. Otherwise, the device will remain in the Idle state until the ALS function is enabled. Once enabled, the device will execute the ALS and Wait states in sequence. Upon completion, the device will automatically begin a new ALS-Wait cycle as long as PON and AEN remain enabled. If the ALS function generates an interrupt and the Sleep-After-Interrupt (SAI) feature is enabled, the device will transition to the Sleep state and remain in a low-power mode until an I^2C command is received clearing the interrupts in the STATUS register. See Interrupts for additional information.

Register Description

Figure 14:
Register Overview

Address	Register Name	R/W	Register Function	Reset Value
0x80	ENABLE	R/W	Enables states and functions	0x00
0x81	ATIME	R/W	ALS integration time	0x00
0x82	PRATE	R/W	Proximity sampling time	0x1F
0x83	WTIME	R/W	Wait time	0x00
0x84	AILTL	R/W	ALS interrupt low threshold low byte	0x00
0x85	AILTH	R/W	ALS interrupt low threshold high byte	0x00
0x86	AIHTL	R/W	ALS interrupt high threshold low byte	0x00
0x87	AIHTH	R/W	ALS interrupt high threshold high byte	0x00
0x88	PILT	R/W	Proximity interrupt low threshold	0x00
0x8A	PIHT	R/W	Proximity interrupt high threshold	0x00
0x8C	PERS	R/W	Interrupt persistence filters	0x00
0x8D	CFG0	R/W	Configuration register zero	0x80
0x8E	PCFG0	R/W	Proximity configuration register zero	0x4F
0x8F	PCFG1	R/W	Proximity configuration register one	0x80
0x90	CFG1	R/W	Configuration register one	0x00
0x91	REVID	R	Revision ID	0x21
0x92	ID	R	Device ID	0xE4
0x93	STATUS	R	Device status register	0x00
0x94	VISDATAL	R	Visible channel data low byte	0x00
0x95	VISDATAH	R	Visible channel data high byte	0x00
0x96	IRDATAL	R	IR channel data low byte	0x00
0x97	IRDATAH	R	IR channel data high byte	0x00
0x9C	PDATA	R	Proximity channel data	0x00
0x9E	REVID2	R	Auxiliary ID	0x01
0x9F	CFG2	R/W	Configuration register two	0x04
0xAB	CFG3	R/W	Configuration register three	0x0C
0xC0	POFFSETL	R/W	Proximity offset magnitude	0x00

Address	Register Name	R/W	Register Function	Reset Value
0xC1	POFFSETH	R/W	Proximity offset sign	0x00
0xD6	AZ_CONFIG	R/W	Autozero configuration	0x7F
0xD7	CALIB	R/W	Calibration start	0x00
0xD9	CALIBCFG	R/W	Calibration configuration	0x50
0xDC	CALIBSTAT	R/W	Calibration status	0x00
0xDD	INTENAB	R/W	Interrupt enables	0x00

Register Access:

- R = Read Only
- W = Write Only
- R/W = Read or Write
- SC = Self Clearing after access

Detailed Register Description

Enable Register (Address 0x80)

Figure 15:
Enable Register

Addr: 0x80		Enable		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	RESERVED	0000	RW	Reserved.
3	WEN	0	RW	This bit activates the wait feature. Active high.
2	PEN	0	RW	This bit activates the proximity detection. Active high.
1	AEN	0	RW	This bit actives the ALS function. Active high. *Set AEN=1 and PON=1 in the same command to ensure auto-zero function is run prior to the first measurement.
0	PON	0	RW	This field activates the internal oscillator and ADC channels. Active high.

Before activating AEN or PEN, preset each applicable operating mode registers and bits.

ATIME Register (Address 0x81)

Figure 16:
ATIME Register

Addr: 0x81		ATIME					
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**			
7:0	ATIME	0x00	RW	ALS/Color value that specifies the integration time in 2.81ms intervals. 0x00 indicates 2.8ms. The maximum ALS value depends on the integration time. For every 2.81ms, the maximum value increases by 1024. This means that to be able to reach ALS full scale, the integration time has to be at least 64*2.8ms.			
				Value	**Integration Cycles**	**Integration Time**	**Maximum ALS Value**
				0x00	1	2.8ms	1023
				0x01	2	5.6ms	2047
				…	…	…	…
				0x3F	64	180ms	65535
				…	…	…	…
				0xFF	256	721ms	65535

The ATIME register controls the integration time of the ALS ADCs. The timer is implemented with a down counter with 0x00 as the terminal count. The timer is clocked at a 2.8ms nominal rate. Loading 0x00 will generate a 2.8ms integration time, loading 0x01 will generate a 5.6ms integration time, and so forth. The RC oscillator runs at 8MHz nominal rate. This gets divided by 11 to generate the integration clock of 727kHz. One count in ATIME (nominal 2.8ms) are 2.81ms. This is 2048 integration clock cycles: 125ns*11*8*256=2.81ms.

PRATE Register (Address 0x82)

Figure 17:
PRATE Register

Addr: 0x82		PRATE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PRATE	0x1F	RW	This register defines the duration of 1 Prox Sample, which is (PRATE + 1)*88µs.

WTIME Register (Address 0x83)

Figure 18:
WTIME Register

Addr: 0x83		WTIME				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**		
7:0	WTIME	0x00	RW	Value that specifies the wait time between ALS cycles in 2.81ms increments.		
				Value	**Increments**	**Wait Time**
				0x00	1	2.8ms (33.8ms)
				0x01	2	5.6ms (67.6ms)
				…	…	…
				0x3F	64	180ms (2.16s)
				…	…	…
				0xFF	256	721ms (8.65s)

The wait timer is implemented using a down counter.
Wait time = (value +1) x 2.8ms. If WLONG is enabled then
Wait time = (value +1) x 2.8ms x 12.

AILTL Register (Address 0x84)

Figure 19:
AILTL Register

Addr: 0x84		AILTL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AILTL	0x00	RW	This register sets the low byte of the LOW ALS threshold.

The Clear (C) channel is compared against low-going 16-bit threshold value set by AILTL and AILTH.

AILTH Register (Address 0x85)

Figure 20:
AILTH Register

Addr: 0x85		AILTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AILTH	0x00	RW	This register sets the high byte of the LOW ALS threshold.

The Clear (C) channel is compared against low-going 16-bit threshold value set by AILTL and AILTH.
The contents of the AILTH and AILTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the C channel is below the AILTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert.
When setting the 16-bit ALS threshold AILTL must be written first, immediately followed by AILTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

AIHTL Register (Address 0x86)

Figure 21:
AIHTL Register

Addr: 0x86		AIHTL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AIHTL	0x00	RW	This register sets the low byte of the HIGH ALS threshold.

The Clear (C) channel is compared against high-going 16-bit threshold value set by AIHTL and AIHTH.
The contents of the AIHTH and AIHTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the C channel is above the AIHTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert. When setting the 16-bit ALS threshold AIHTL must be written first, immediately followed by AIHTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

AIHTH Register (Address 0x87)

Figure 22:
AIHTH Register

Addr: 0x87		AIHTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AIHTH	0x00	RW	This register sets the high byte of the HIGH ALS threshold.

The Clear (C) channel is compared against high-going 16-bit threshold value set by AIHTL and AIHTH.
The contents of the AIHTH and AIHTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the C channel is above the AIHTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert.
When setting the 16-bit ALS threshold AIHTL must be written first, immediately follow by AIHTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

PILT Register (Address 0x88)

Figure 23:
PILT Register

Addr: 0x88		PILT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PILT	0x00	RW	This register sets the Proximity ADC channel low threshold.

The proximity channel is compared against low-going 8-bit threshold value set by PILT.
If the value generated by the proximity channel is below the PILT threshold and the PPERS value is reached, the PINT bit is asserted. If PIEN is set, then the INT pin will also assert.

PIHT Register (Address 0x8A)

Figure 24:
PIHT Register

Addr: 0x8A		PIHT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PIHT	0x00	RW	This register sets the proximity ADC channel high threshold.

The proximity channel is compared against high-going 8-bit threshold value set by PIHT.
If the value generated by the proximity channel is above the PIHT threshold and the PPERS value is reached, the PINT bit is asserted. If PIEN is set, then the INT pin will also assert.

PERS Register (Address 0x8C)

Figure 25:
PERS Register

Addr: 0x8C		PERS			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:4	PPERS	0000	RW	This register sets the proximity persistence filter.	
				Value	**Interrupt**
				0	Every proximity cycle
				1	Any value outside PILT/PIHT thresholds
				2	2 consecutive proximity values out of range
				3	3 consecutive proximity values out of range
				…	….
				15	15 consecutive proximity values out of range

Addr: 0x8C		PERS			
Bit	Bit Name	Default	Access	Bit Description	
3:0	APERS	0000	RW	This register sets the ALS persistence filter.	
				0	Every ALS cycle
				1	Any value outside ALS thresholds
				2	2 consecutive ALS values out of range
				3	3 consecutive ALS values out of range
				4	5 consecutive ALS values out of range
				5	10 consecutive ALS values out of range
				6	15 consecutive ALS values out of range
				7	20 consecutive ALS values out of range
				…	…
				13	50 consecutive ALS values out of range
				14	55 consecutive ALS values out of range
				15	60 consecutive ALS values out of range

The frequency of consecutive proximity channel results outside of threshold limits are counted; this count value is compared against the PPERS value. If the counter is equal to the PPERS value an interrupt is asserted. Any time a proximity channel result is inside the threshold values the counter is cleared.
The frequency of consecutive clear channel results outside of threshold limits are counted; this count value is compared against the APEARS value. If the counter is equal to the APERS setting an interrupt is asserted. Any time a clear channel result is inside the threshold values the counter is cleared.

CFG0 Register (Address 0x8D)

Figure 26:
CFG0 Register

Addr: 0x8D		CFG0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Reserved	10000	RW	This field must be set to the default value.
2	WLONG	0	RW	When Wait Long is asserted the wait period as set by WTIME is increased by a factor of 12.
1:0	Reserved	00	RW	This field must be set to the default value.

The wait timer is implemented using a down counter.
Wait time = (value +1) x 2.8ms. If WLONG is enabled then
Wait time = (value +1) x 2.8ms x 12.

PCFG0 Register (Address 0x8E)

Figure 27:
PCFG0 Register

Addr: 0x8E		PCFG0			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:6	PPULSE_LEN	01	RW	Proximity pulse length. Default is 8µs.	
				Value	**Pulse Length**
				0	4µs
				1	8µs
				2	16µs
				3	32µs
5:0	PPULSE	001111	RW	Maximum number of pulses in a single proximity cycle. Default is 16 pulses.	
				Value	**Maximum Number of Pulses**
				0	1
				1	2
				2	3
				…	…
				63	64

PCFG1 Register (Address 0x8F)

Figure 28:
PCFG1 Register

<table>
<tr><th colspan="2">Addr: 0x8F</th><th colspan="3">PCFG1</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th>Bit Description</th></tr>
<tr><td rowspan="6">7:6</td><td rowspan="6">PGAIN</td><td rowspan="6">10</td><td rowspan="6">RW</td><td colspan="2">This field sets the gain of the proximity IR sensor. Default is 4x gain.</td></tr>
<tr><td>Value</td><td>Prox Gain</td></tr>
<tr><td>0</td><td>1x</td></tr>
<tr><td>1</td><td>2x</td></tr>
<tr><td>2</td><td>4x</td></tr>
<tr><td>3</td><td>8x</td></tr>
<tr><td>5</td><td>Reserved</td><td>0</td><td>RW</td><td colspan="2">Reserved.</td></tr>
<tr><td rowspan="7">4:0</td><td rowspan="7">PLDRIVE</td><td rowspan="7">00000</td><td rowspan="7">RW</td><td colspan="2">This field sets the drive strength of the IR LED current. Default is 6mA.</td></tr>
<tr><td>Value</td><td>LED Current</td></tr>
<tr><td>0</td><td>6mA</td></tr>
<tr><td>1</td><td>12mA</td></tr>
<tr><td colspan="2">i_{LED} = 6(PLDRIVE +1) mA</td></tr>
<tr><td>30</td><td>186mA</td></tr>
<tr><td>31</td><td>192mA</td></tr>
</table>

CFG1 Register (Address 0x90)

Figure 29:
CFG1 Register

Addr: 0x90		CFG1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0000	RW	Reserved.
3	IR_TO_GREEN	0	RW	If set high, the IR (Proximity) photodiode is switched into the Green channel's data converter. GDATAL/H register will report IR content. Green photodiode is not connected.
2	Reserved	0	RW	Reserved.
1:0	AGAIN	00	RW	This field sets the gain of the ALS/Color sensor. Default is 1x gain.

Value	ALS/Color Gain
0	1x
1	4x
2	16x
3	64x

REVID Register (Address 0x91)

Figure 30:
REVID Register

Addr: 0x91		REVID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Reserved	00100	RO	Reserved.
2:0	REV_ID	001	RO	Device revision number.