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With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

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P-Channel Power MOSFET

-30V, -64A, 8.5mΩ

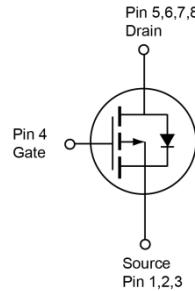
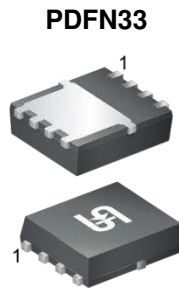
FEATURES

- Low $R_{DS(ON)}$ to minimize conductive losses
- Low gate charge for fast power switching
- 100% UIS and R_g tested
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

APPLICATIONS

- DC-DC Converters
- Battery Power Management
- Load Switch
- BLDC Motor Drives

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V_{DS}	-30	V
$R_{DS(on)}$ (max)	$V_{GS} = -10V$	8.5
	$V_{GS} = -4.5V$	14
Q_g	27	nC



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current (Note 1)	I_D	$T_C = 25^\circ\text{C}$	-64
		$T_A = 25^\circ\text{C}$	-14
Pulsed Drain Current	I_{DM}	-256	A
Single Pulse Avalanche Current (Note 2)	I_{AS}	-23	A
Single Pulse Avalanche Energy (Note 2)	E_{AS}	79	mJ
Total Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	50
		$T_C = 125^\circ\text{C}$	10
Total Power Dissipation	P_D	$T_A = 25^\circ\text{C}$	2.4
		$T_A = 125^\circ\text{C}$	0.5
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	53	$^\circ\text{C/W}$

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$	BV_{DSS}	-30	--	--	V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	$V_{GS(TH)}$	-1.2	-1.6	-2.5	V
Gate-Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	I_{GSS}	--	--	± 100	nA
Drain-Source Leakage Current	$V_{GS} = 0\text{V}, V_{DS} = -30\text{V}$	I_{DSS}	--	--	-1	μA
	$V_{GS} = 0\text{V}, V_{DS} = -30\text{V}$ $T_J = 125^\circ\text{C}$		--	--	-100	
Drain-Source On-State Resistance (Note 3)	$V_{GS} = -10\text{V}, I_D = -14\text{A}$	$R_{DS(on)}$	--	7.1	8.5	m Ω
	$V_{GS} = -4.5\text{V}, I_D = -14\text{A}$		--	11	14	
Forward Transconductance (Note 3)	$V_{DS} = -5\text{V}, I_D = -14\text{A}$	g_{fs}	--	38	--	S
Dynamic (Note 4)						
Total Gate Charge	$V_{GS} = -10\text{V},$ $V_{DS} = -15\text{V}, I_D = -14\text{A}$	Q_g	--	55	--	nC
Total Gate Charge	$V_{GS} = -4.5\text{V},$ $V_{DS} = -15\text{V}, I_D = -14\text{A}$	Q_g	--	27	--	
Gate-Source Charge		Q_{gs}	--	9.2	--	
Gate-Drain Charge		Q_{gd}	--	9.9	--	
Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = -15\text{V}$ $f = 1.0\text{MHz}$	C_{iss}	--	3234	--	pF
Output Capacitance		C_{oss}	--	396	--	
Reverse Transfer Capacitance		C_{rss}	--	251	--	
Gate Resistance	$f = 1.0\text{MHz},$ open drain	R_g	1.6	6	12	Ω
Switching (Note 4)						
Turn-On Delay Time	$V_{GS} = -10\text{V}, V_{DS} = -15\text{V},$ $I_D = -14\text{A}, R_G = 2\Omega,$	$t_{d(on)}$	--	7.2	--	ns
Turn-On Rise Time		t_r	--	2.6	--	
Turn-Off Delay Time		$t_{d(off)}$	--	56	--	
Turn-Off Fall Time		t_f	--	27	--	
Source-Drain Diode						
Forward Voltage (Note 3)	$V_{GS} = 0\text{V}, I_S = -14\text{A}$	V_{SD}	--	--	-1	V
Reverse Recovery Time	$I_S = -14\text{A},$ $di/dt = 100\text{A}/\mu\text{s}$	t_{rr}	--	23	--	ns
Reverse Recovery Charge		Q_{rr}	--	11	--	nC

Notes:

- Silicon limited current only.
- $L = 0.3\text{mH}, V_{GS} = -10\text{V}, V_{DD} = -25\text{V}, R_G = 25\Omega, I_{AS} = -23\text{A},$ Starting $T_J = 25^\circ\text{C}$
- Pulse test: Pulse Width $\leq 300\mu\text{s},$ duty cycle $\leq 2\%$.
- Switching time is essentially independent of operating temperature.

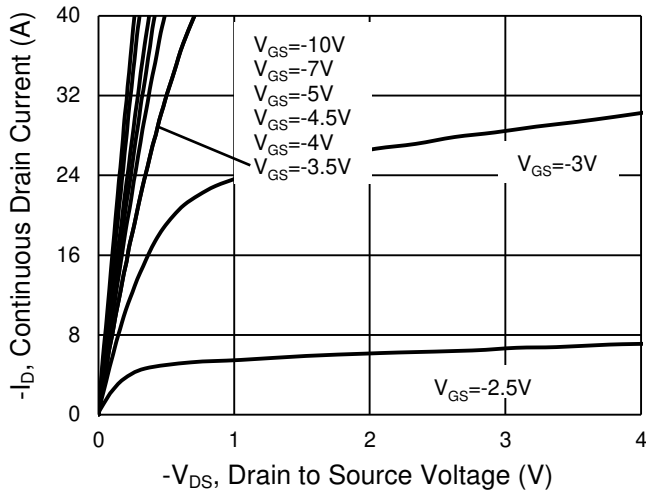
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM085P03CV RGG	PDFN33	5,000pcs / 13" Reel

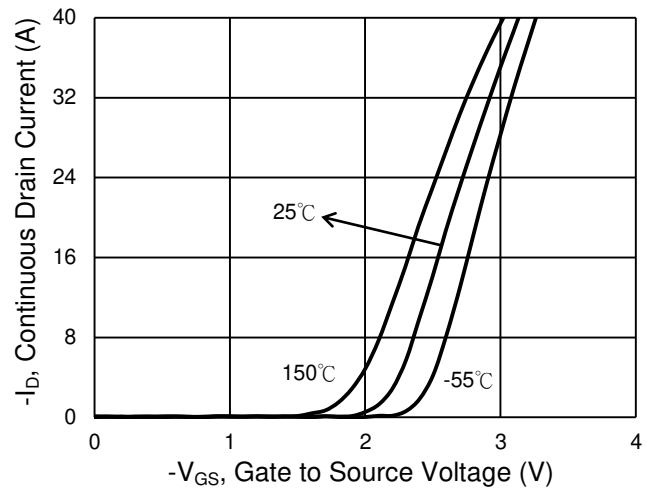
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

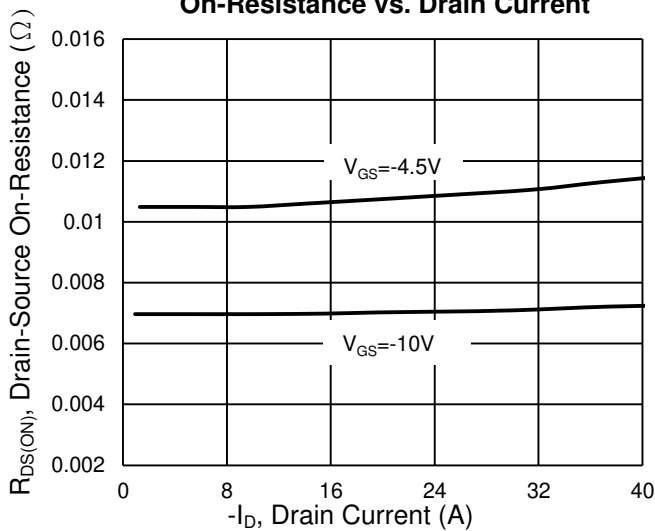
Output Characteristics



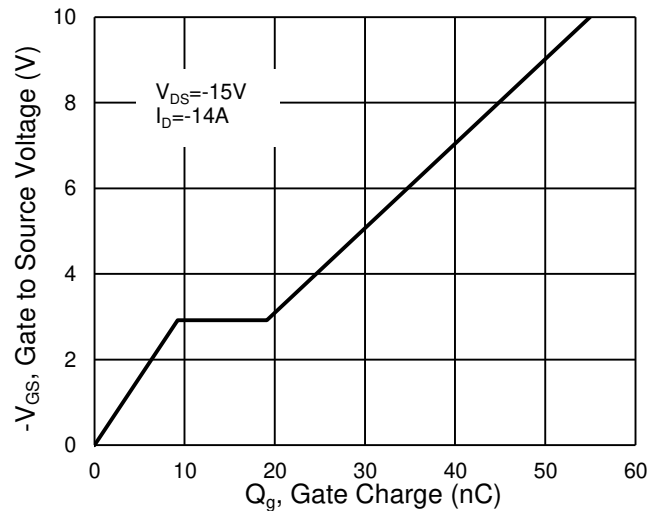
Transfer Characteristics



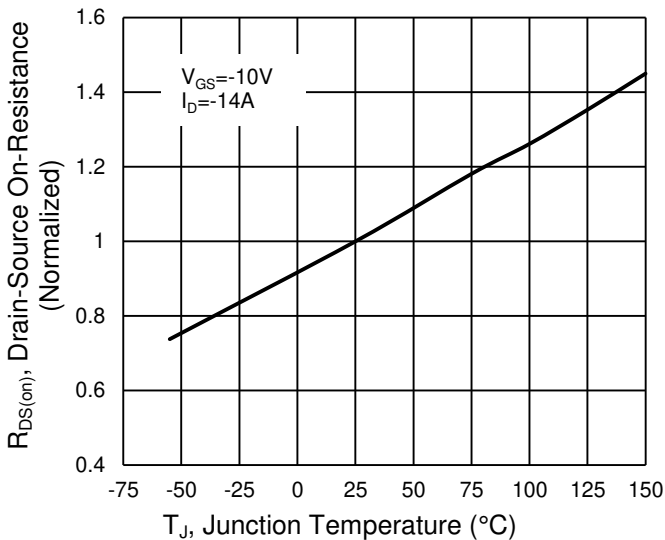
On-Resistance vs. Drain Current



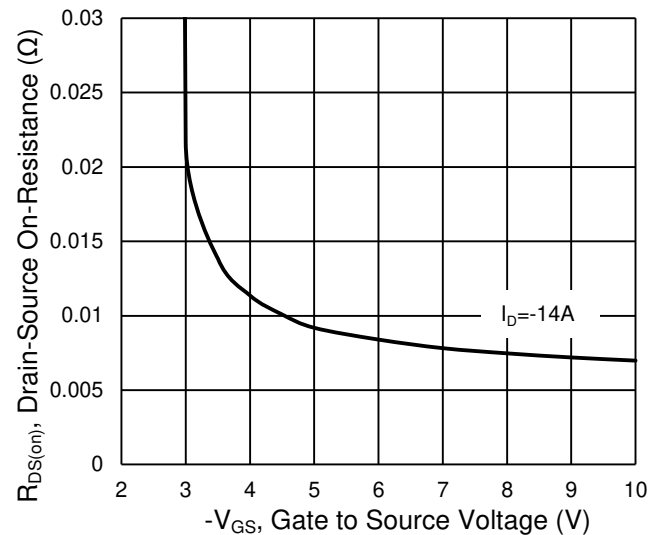
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



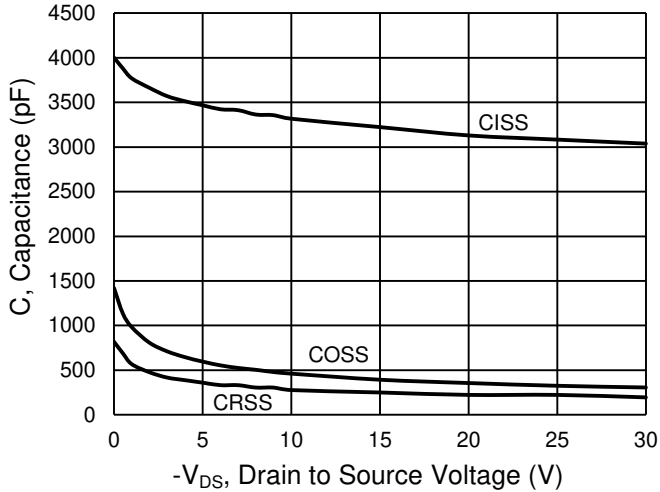
On-Resistance vs. Gate-Source Voltage



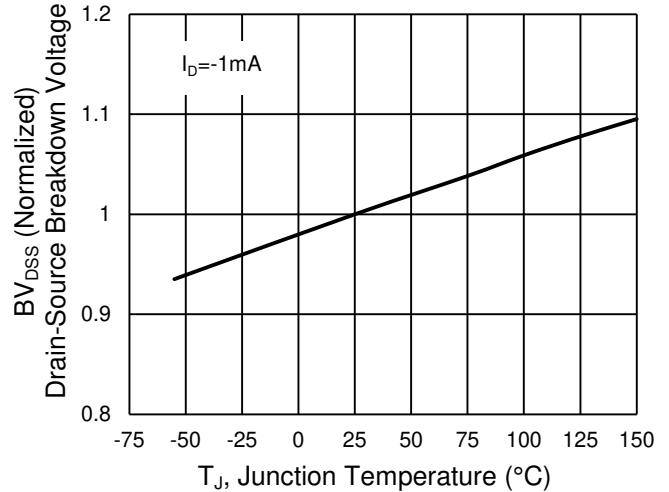
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

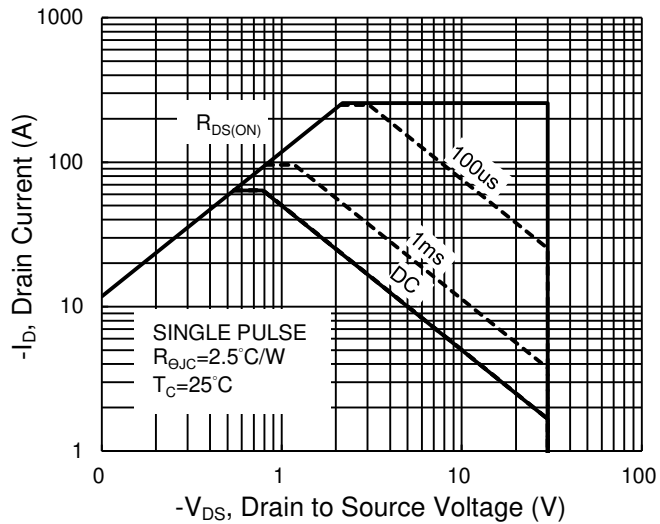
Capacitance vs. Drain-Source Voltage



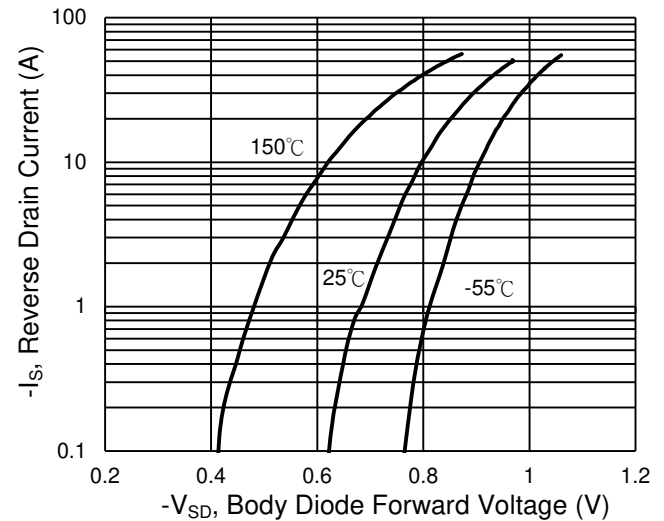
BV_{DSS} vs. Junction Temperature



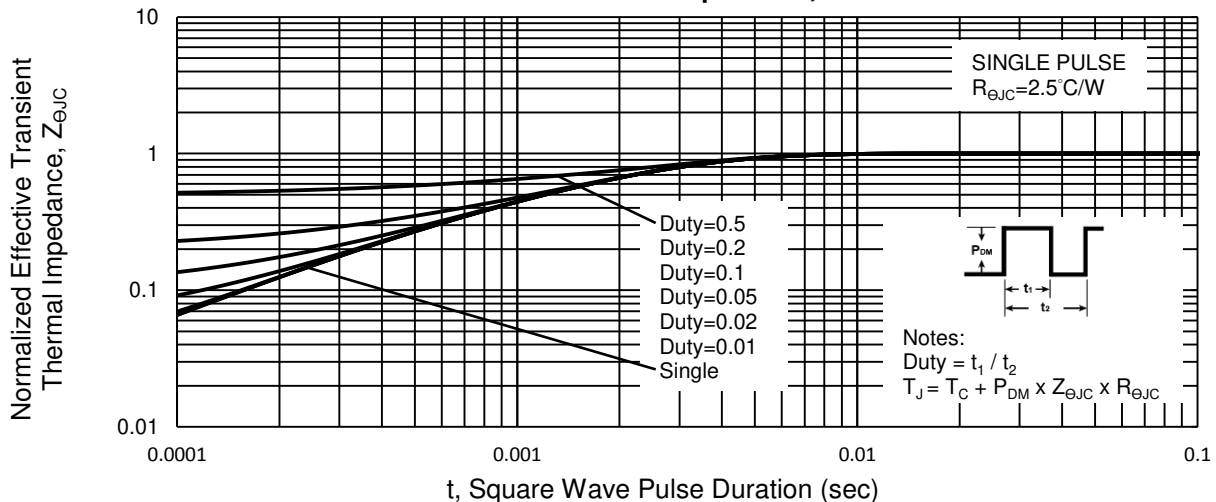
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

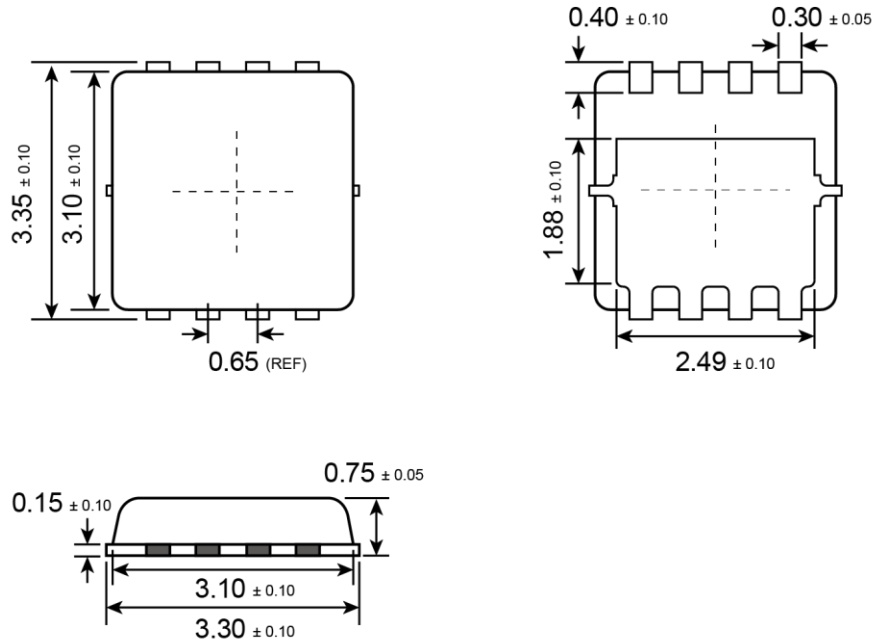


Normalized Thermal Transient Impedance, Junction-to-Case

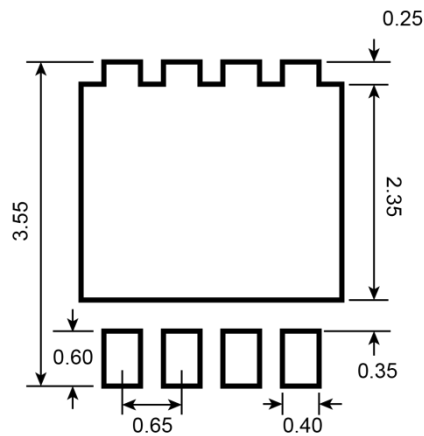


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

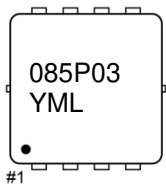
PDFN33



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- Y** = Year Code
- M** = Month Code for Halogen Free Product
 - O** =Jan
 - P** =Feb
 - Q** =Mar
 - R** =Apr
 - S** =May
 - T** =Jun
 - U** =Jul
 - V** =Aug
 - W** =Sep
 - X** =Oct
 - Y** =Nov
 - Z** =Dec
- L** = Lot Code (1~9, A~Z)

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