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N-Channel Power MOSFET

 $600V, 1A, 10\Omega$

FEATURES

- Advanced planar process
- 100% avalanche tested
- Low $R_{DS(ON)}$ 8 Ω (Typ.)
- Low gate charge typical @ 6.1 nC (Typ.)
- Low Crss typical @4.2pF (Typ.)

KEY PERFORMANCE PARAMETERS				
PARAMETER VALUE UN				
$V_{ t DS}$	600	V		
R _{DS(on)} (max)	10	Ω		
Q_g	6.1	nC		



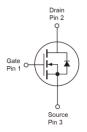




APPLICATION

- Power Supply
- Lighting
- Charger





Notes: MSL 3 (Moisture Sensitivity Level) for TO-252 (D-PAK), SOT-223 per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C unless otherwise noted)					
PARAMETER	SYMBOL	IPAK/DPAK	SOT-223	UNIT	
Drain-Source Voltage	V_{DS}	600		V	
Gate-Source Voltage	V_{GS}	±3	80	V	
Continuous Drain Current (Note 1) $ T_C = 25^{\circ}C $ $T_C = 100^{\circ}C $	I _D	0.	7	А	
Pulsed Drain Current (Note 2)	I _{DM}	4		Α	
Total Power Dissipation @ T _C = 25°C	P _{DTOT}	39	2.1	W	
Single Pulsed Avalanche Energy (Note 3)	E _{AS}	5	5	mJ	
Single Pulsed Avalanche Current (Note 3)	I _{AS}	1		Α	
Peak Diode Recovery dv/dt(Note 4)	dv/dt	4.5		V/ns	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150		°C	

THERMAL PERFORMANCE				
PARAMETER	SYMBOL	IPAK/DPAK	SOT-223	UNIT
Junction to Case Thermal Resistance	R _{eJC}	2.87		°C/W
Junction to Ambient Thermal Resistance	R _{OJA}	110	60	°C/W

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air.



ELECTRICAL SPECIFICATIONS (T _A = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 5)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV _{DSS}	600			V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 0.5A$	R _{DS(ON)}		8	10	Ω
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	$V_{GS(TH)}$	2.5	3.5	4.5	٧
Zero Gate Voltage Drain Current	$V_{DS} = 600V, V_{GS} = 0V$	I _{DSS}			10	μΑ
Gate Body Leakage	$V_{GS} = \pm 30V, V_{DS} = 0V$	I _{GSS}			±100	nA
Forward Transfer Conductance	$V_{DS} = 10V, I_D = 0.5A$	g _{fs}		0.8		S
Dynamic (Note 6)						
Total Gate Charge	.,	Q_g		6.1		
Gate-Source Charge	$V_{DS} = 480V, I_{D} = 1A,$ $V_{GS} = 10V$	Q_{gs}		1.4		nC
Gate-Drain Charge	V _{GS} = 10V	Q_{gd}		3.3		
Input Capacitance		C _{iss}		138		
Output Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ f = 1.0MHz	C _{oss}		17.1		pF
Reverse Transfer Capacitance		C_{rss}		4.2		
Gate Resistance	F = 1MHz, open drain	R_g		12.5		Ω
Switching (Note 7)						
Turn-On Delay Time		t _{d(on)}		7.7		
Turn-On Rise Time	$V_{DD} = 300V, R_G = 25\Omega$ $I_D = 1A, V_{GS} = 10V$	t _r		6.8		
Turn-Off Delay Time		$t_{d(off)}$		15.3		ns
Turn-Off Fall Time		t _f		14.9		
Source-Drain Diode (Note 5)						
Diode Forward Voltage	I _S = 1A, V _{GS} = 0V	V _{SD}		0.9	1.4	V
Source Current	Integral reverse diode	Is			1	
Source Current (Pulse)	In the MOSFET	I _{SM}			4	A

Notes:

- 1. Current limited by package.
- 2. Pulse width limited by the maximum junction temperature.
- 3. L = 10mH, $I_{AS} = 1A$, $V_{DD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}C$.
- 4. $I_{SD} \le 1A$, $V_{DD} \le BV_{DSS}$, $di/dt \le 200A/us$, Starting $T_J = 25^{\circ}C$.
- 5. Pulse test: PW \leq 300 μ s, duty cycle \leq 2%.
- 6. For DESIGN AID ONLY, not subject to production testing.
- 7. Switching time is essentially independent of operating temperature.





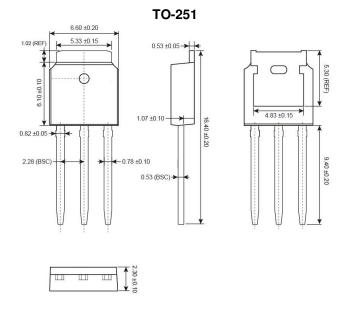
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM1NB60CH C5G	TO-251	75 pcs / Tube
TSM1NB60CP ROG	TO-252	2,500 pcs / 13" Reel
TSM1NB60CW RPG	SOT-223	2,500 pcs / 13" Reel

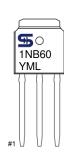
Note:

- 1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- 2. Halogen-free according to IEC 61249-2-21 definition





MARKING DIAGRAM



Y = Year Code

M = Month Code for Halogen Free Product

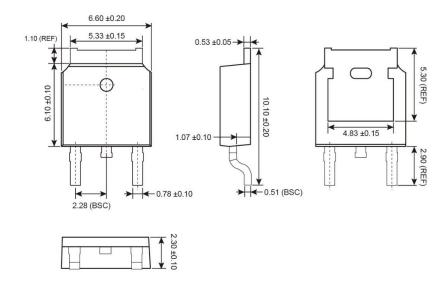
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W = Sep X = Oct Y = Nov Z = Dec

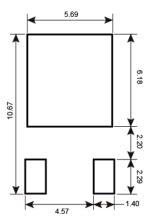
L = Lot Code (1~9, A~Z)



TO-252



SUGGESTED PAD LAYOUT



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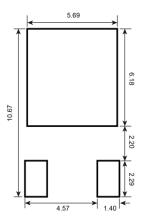
Z =Dec

 $\mathbf{L} = \text{Lot Code } (1 \sim 9, A \sim Z)$



TO-252 6.57 ±0.16 1.08 ±0.19 0.515 ±0.065 5.34 ±0.13 5.3 (MIN) 6.11 ±0.11 -0.825 ± 0.185 9.9 ± 0.5 0.127 (MAX) 2.743 0.525 ±0.075 0.955 ±0.185 -1.585 ±0.185 0.76 ±0.12 0.508 (BSC) 2.286 (BSC)

SUGGESTED PAD LAYOUT (Unit: Millimeters)



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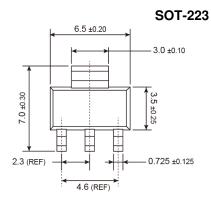
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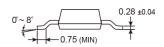
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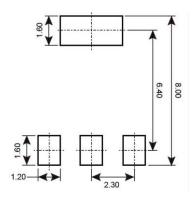








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