



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

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N-Channel Power MOSFET

60V, 35A, 22mΩ

FEATURES

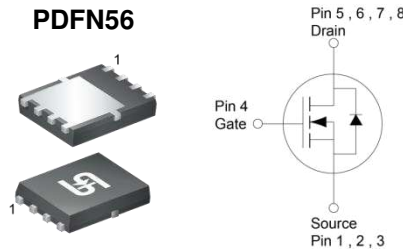
- Low $R_{DS(ON)}$ to minimize conductive losses
- Low gate charge for fast power switching
- 100% UIS and R_g tested.
- 175°C Operating Junction Temperature
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

KEY PERFORMANCE PARAMETERS

PARAMETER	VALUE	UNIT	
V_{DS}	60	V	
$R_{DS(on)}$ (max)	$V_{GS} = 10V$	22	mΩ
Q_g	23	nC	

APPLICATIONS

- BLDC Motor Control
- Battery Power Management
- DC-DC converter
- Secondary Synchronous Rectification



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current (Note 1)	I_D	$T_C = 25^\circ\text{C}$	35
		$T_A = 25^\circ\text{C}$	8
Pulsed Drain Current	I_{DM}	140	A
Single Pulse Avalanche Current (Note 2)	I_{AS}	15	A
Single Pulse Avalanche Energy (Note 2)	E_{AS}	33.8	mJ
Total Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	68
		$T_C = 125^\circ\text{C}$	23
Total Power Dissipation	P_D	$T_A = 25^\circ\text{C}$	3.1
		$T_A = 125^\circ\text{C}$	1
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +175	$^\circ\text{C}$

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	2.2	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	48	$^\circ\text{C/W}$

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. The $R_{\theta JA}$ limit presented here is based on mounting on a 1 in² pad of 2 oz copper.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	BV_{DSS}	60	--	--	V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	2	3.3	4	V
Gate-Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	I_{GSS}	--	--	± 100	nA
Drain-Source Leakage Current	$V_{GS} = 0\text{V}, V_{DS} = 60\text{V}$	I_{DSS}	--	--	1	μA
	$V_{GS} = 0\text{V}, V_{DS} = 60\text{V}$ $T_J = 125^\circ\text{C}$		--	--	100	
Drain-Source On-State Resistance (Note 3)	$V_{GS} = 10\text{V}, I_D = 8\text{A}$	$R_{DS(on)}$	--	19	22	m Ω
Forward Transconductance (Note 3)	$V_{DS} = 10\text{V}, I_D = 8\text{A}$	g_{fs}	--	35	--	S
Dynamic (Note 4)						
Total Gate Charge	$V_{GS} = 10\text{V}, V_{DS} = 30\text{V},$ $I_D = 8\text{A}$	Q_g	--	23	-	nC
Gate-Source Charge		Q_{gs}	--	6.5	--	
Gate-Drain Charge		Q_{gd}	--	5.4	--	
Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 30\text{V}$ $f = 1.0\text{MHz}$	C_{iss}	--	1454	--	pF
Output Capacitance		C_{oss}	--	90	--	
Reverse Transfer Capacitance		C_{rss}	--	24	--	
Gate Resistance	$f = 1.0\text{MHz}$	R_g	0.6	2	4	Ω
Switching (Note 4)						
Turn-On Delay Time	$V_{GS} = 10\text{V}, V_{DS} = 30\text{V},$ $I_D = 8\text{A}, R_G = 2\Omega$	$t_{d(on)}$	--	3	--	ns
Turn-On Rise Time		t_r	--	19	--	
Turn-Off Delay Time		$t_{d(off)}$	--	10	--	
Turn-Off Fall Time		t_f	--	18	--	
Source-Drain Diode						
Forward Voltage (Note 3)	$V_{GS} = 0\text{V}, I_S = 8\text{A}$	V_{SD}	--	--	1.2	V
Reverse Recovery Time	$I_S = 8\text{A},$ $di/dt = 100\text{A}/\mu\text{s}$	t_{rr}	--	16	--	ns
Reverse Recovery Charge		Q_{rr}	--	11	--	nC

Notes:

- Silicon limited current only.
- $L = 0.3\text{mH}, V_{GS} = 10\text{V}, V_{DD} = 30\text{V}, R_G = 25\Omega, I_{AS} = 15\text{A},$ Starting $T_J = 25^\circ\text{C}$
- Pulse test: Pulse Width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- Switching time is essentially independent of operating temperature.

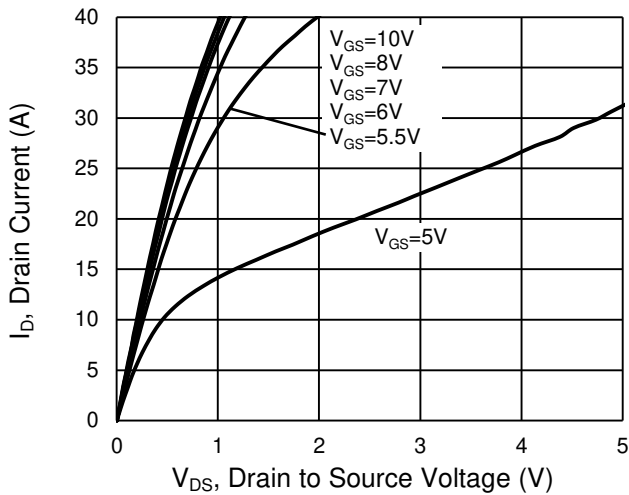
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM220NB06CR RLG	PDFN56	2,500pcs / 13" Reel

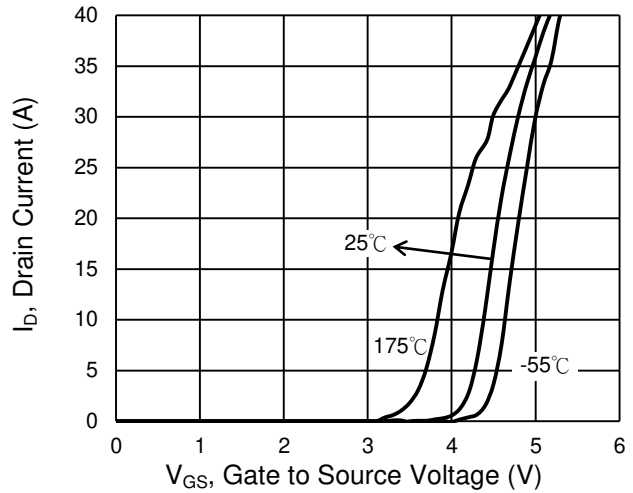
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

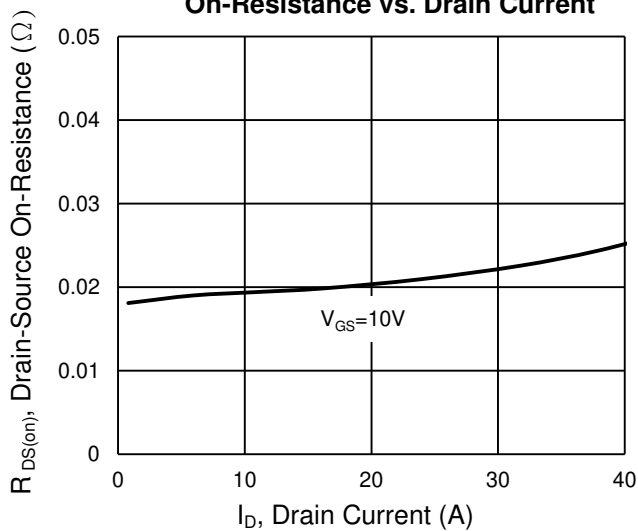
Output Characteristics



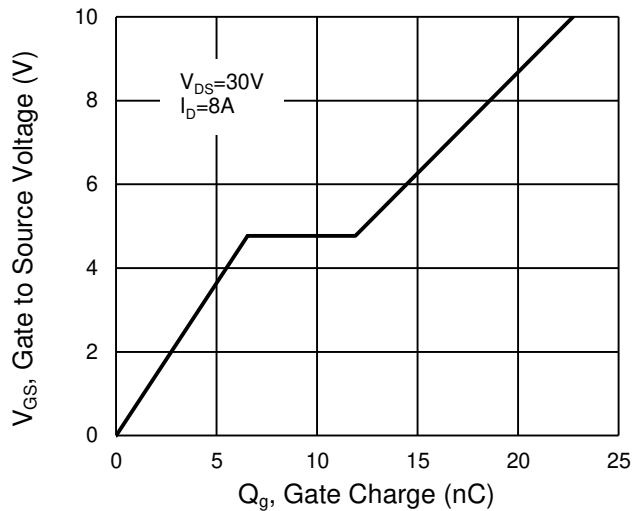
Transfer Characteristics



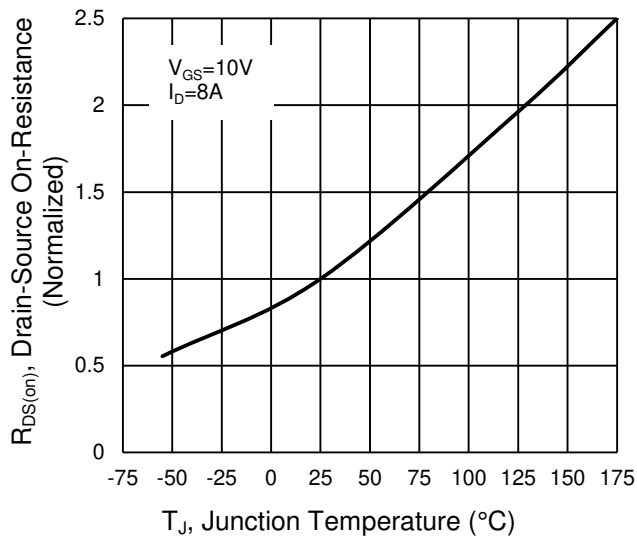
On-Resistance vs. Drain Current



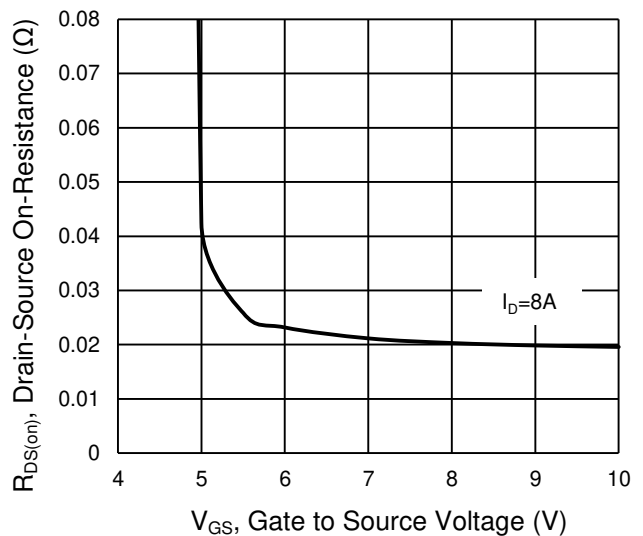
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



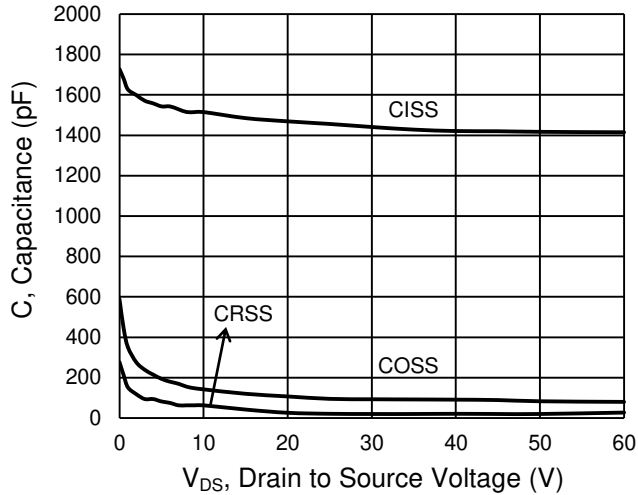
On-Resistance vs. Gate-Source Voltage



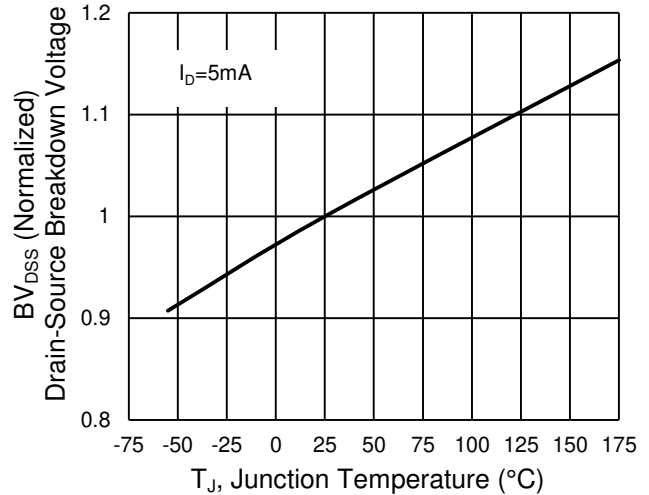
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

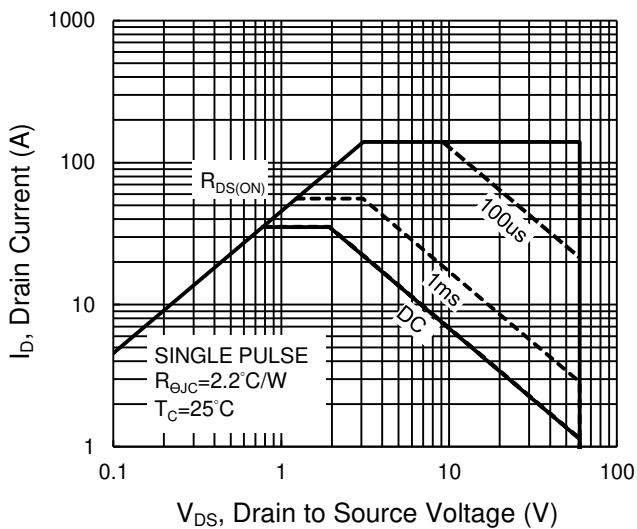
Capacitance vs. Drain-Source Voltage



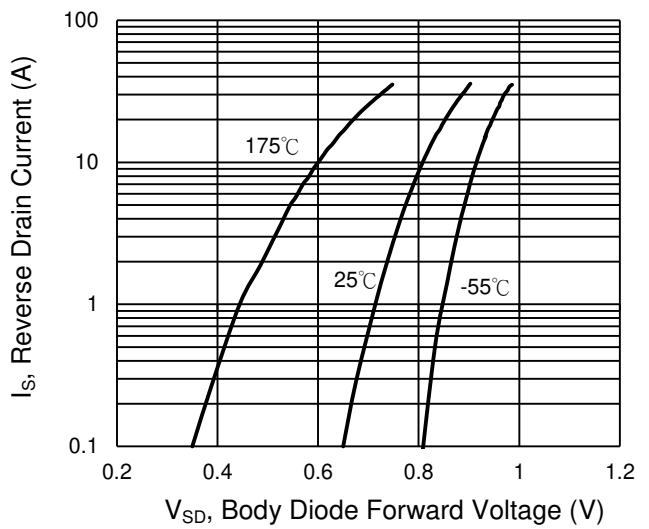
BV_{DSS} vs. Junction Temperature



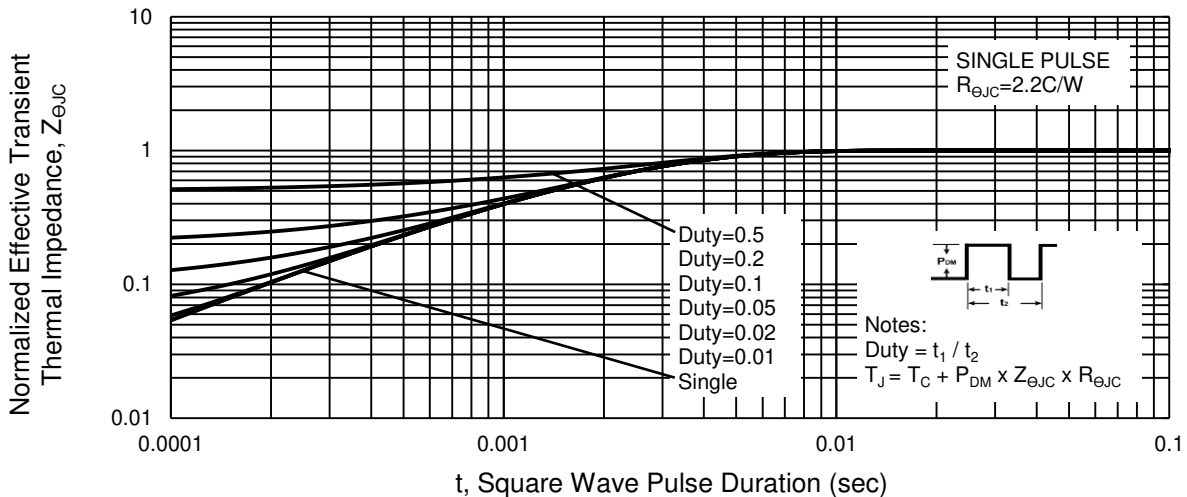
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

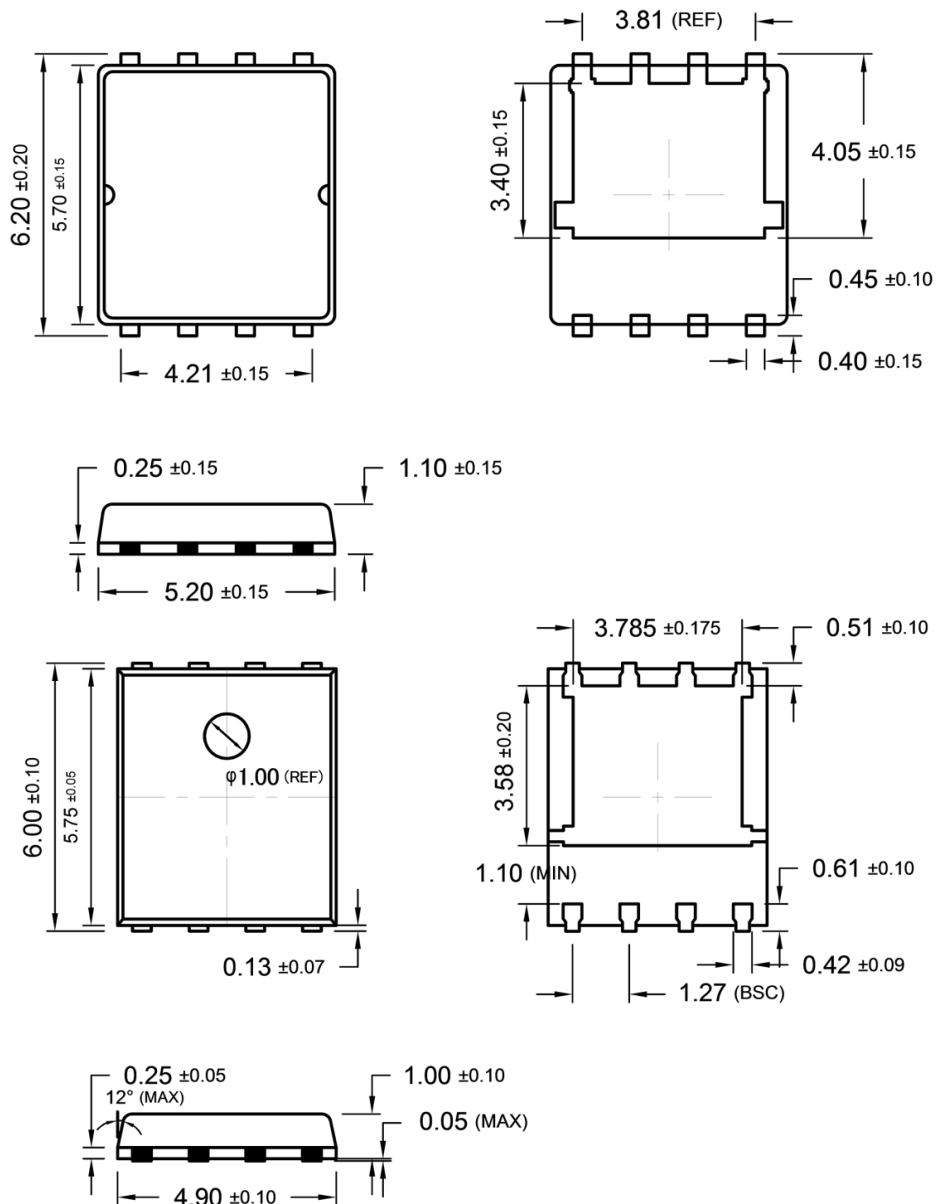


Normalized Thermal Transient Impedance, Junction-to-Case

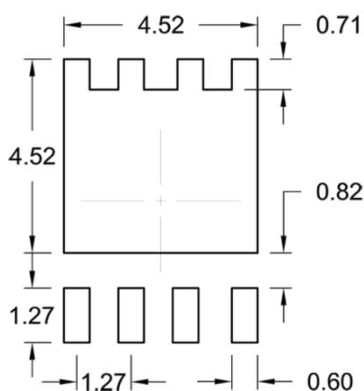


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

PDFN56



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

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