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With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



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N-Channel Power MOSFET

1000V, 1.85A, 8.5Ω

FEATURES

- 100% avalanche tested
- Advanced planar process
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

ΔD	DI	ICA	TI	n	NS

- AC/DC LED Lighting
- Power Supply
- Power Meter

KEY PERFORMANCE PARAMETERS				
PARAMETER	VALUE	UNIT		
V_{DS}	1000	V		
R _{DS(on)} (max)	8.5	Ω		
Q_g	17	nC		

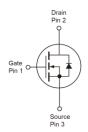






TO-252 (DPAK)





Notes: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C unless otherwise noted)				
PARAMETER		SYMBOL	Limit	UNIT
Drain-Source Voltage		V _{DS}	1000	٧
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current (Note 1)	$T_C = 25^{\circ}C$		1.85	
	$T_C = 100$ °C	I _D	1.16	A
Pulsed Drain Current (Note 2)		I _{DM}	7.4	А
Total Power Dissipation @ T _C = 25°C		P _{DTOT}	77	W
Single Pulse Avalanche Energy (Note 3)		E _{AS}	20	mJ
Single Pulse Avalanche Current (Note 3)		I _{AS}	1.4	А
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE				
PARAMETER	SYMBOL	Limit	UNIT	
Junction to Case Thermal Resistance	R _{eJC}	1.62	°C/W	
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	62	°C/W	

Thermal Performance Note: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air.

1



ELECTRICAL SPECIFICATIONS (T _A = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static	Static					
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV _{DSS}	1000			V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	$V_{GS(TH)}$	3.5	4.5	5.5	V
Gate Body Leakage	$V_{GS} = \pm 30 V$, $V_{DS} = 0 V$	I _{GSS}			±100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 1000V, V_{GS} = 0V$	I _{DSS}			1	μΑ
Drain-Source On-State Resistance (Note 4)	$V_{GS} = 10V, I_D = 0.9A$	R _{DS(on)}		6	8.5	Ω
Dynamic (Note 5)	l				l	l
Total Gate Charge		Q_g		17		
Gate-Source Charge	$V_{DS} = 800V, I_D = 1.85A,$ $V_{GS} = 10V$	Q _{gs}		5		nC
Gate-Drain Charge		Q_{gd}		9		
Input Capacitance		C _{iss}		625		
Output Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$	C _{oss}		38		pF
Reverse Transfer Capacitance	f = 1.0MHz	C _{rss}		15		
Gate Resistance	f = 1.0MHz, open drain	R_g		2.2		Ω
Switching (Note 6)						
Turn-On Delay Time		t _{d(on)}		31		
Turn-On Rise Time	$V_{DD} = 500V, R_G = 25\Omega,$ $I_D = 0.9A, V_{GS} = 10V$	t _r		14		
Turn-Off Delay Time		t _{d(off)}		78		ns
Turn-Off Fall Time		t _f		44		
Source-Drain Diode						
Forward Voltage (Note 4)	I _S = 1.85A, V _{GS} = 0V	V_{SD}			1.4	V
Reverse Recovery Time	V _B = 100V, I _S = 1.85A	t _{rr}		359		ns
Reverse Recovery Charge	$dI_F/dt = 100A/\mu s$	Q_{rr}		1.34		μC

Notes:

- 1. Current limited by package
- 2. Pulse width limited by the maximum junction temperature
- 3. L = 20mH, $I_{AS} = 1.4A$, $V_{DD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}C$
- 4. Pulse test: PW ≤ 300μs, duty cycle ≤ 2%
- 5. For DESIGN AID ONLY, not subject to production testing.
- 6. Switching time is essentially independent of operating temperature.

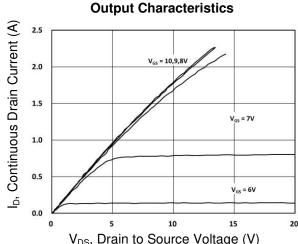
ORDERING INFORMATION

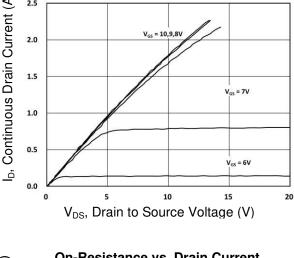
PART NO.	PACKAGE	PACKING
TSM2N100CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel

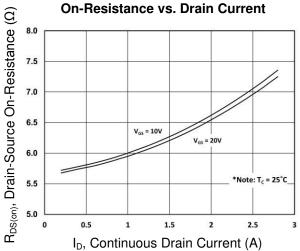


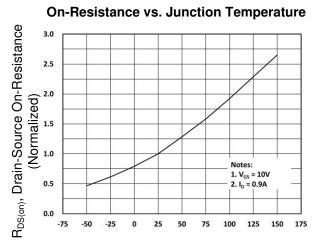
CHARACTERISTICS CURVES

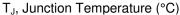
(T_C = 25°C unless otherwise noted)

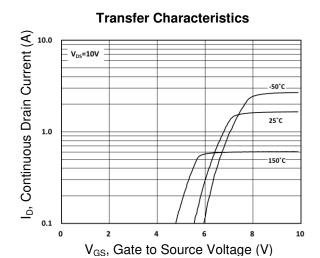




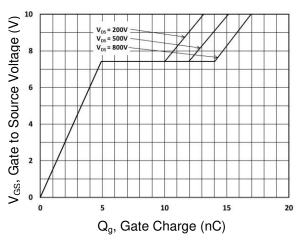




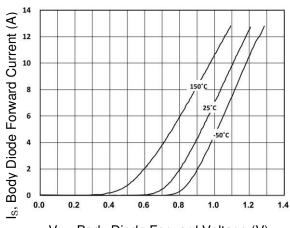




Gate-Source Voltage vs. Gate Charge



Source-Drain Diode Forward Current vs. Voltage



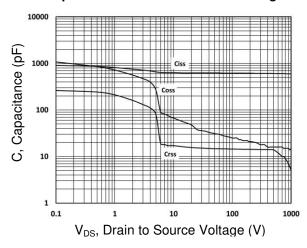
V_{SD}, Body Diode Forward Voltage (V)



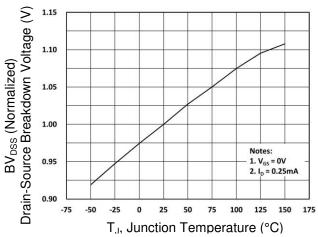
CHARACTERISTICS CURVES

 $(T_C = 25^{\circ}C \text{ unless otherwise noted})$

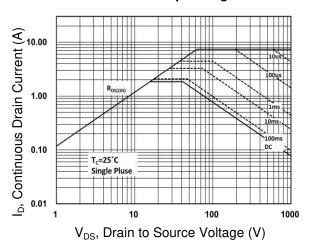
Capacitance vs. Drain-Source Voltage



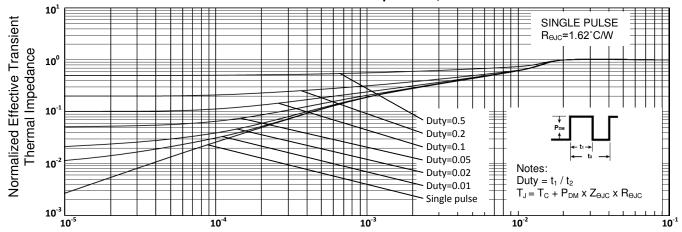
$\ensuremath{\mathsf{BV}_{\mathsf{DSS}}}$ vs. Junction Temperature



Maximum Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Square Wave Pulse Duration (s)

4



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-252

1.10 (REF)

5.30 ±0.15

0.53 ±0.05

1.07 ±0.10

1.07 ±0.10

1.07 ±0.10

1.07 ±0.10

1.07 ±0.10

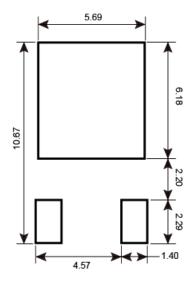
1.07 ±0.10

1.07 ±0.10

1.07 ±0.10

1.07 ±0.10

SUGGESTED PAD LAYOUT



MARKING DIAGRAM



Y = Year Code

M = Month Code

 \mathbf{O} =Jan \mathbf{P} =Feb \mathbf{Q} =Mar \mathbf{R} =Apr

 $S = May \quad T = Jun \quad U = Jul \quad V = Aug$

Y =Nov

Z =Dec

5

L = Lot Code $(1 \sim 9, A \sim Z)$

W =Sep X =Oct



Taiwan Semiconductor

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