



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

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N-Channel Power MOSFET

500V, 5A, 1.38Ω

FEATURES

- 100% UIS and R_g tested
- Advanced planar process
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

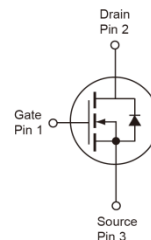
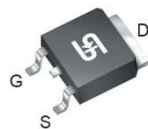
KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V_{DS}	500	V
$R_{DS(on)}$ (max)	1.38	Ω
Q_g	15	nC

APPLICATIONS

- AC/DC LED Lighting
- Power Supply
- Charger



TO-252 (DPAK)



Notes: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	Limit	UNIT
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	±30	V
Continuous Drain Current (Note 1)	I_D	$T_C = 25^\circ\text{C}$	5
		$T_C = 100^\circ\text{C}$	2.2
Pulsed Drain Current (Note 2)	I_{DM}	20	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_{DTOT}	83	W
Single Pulse Avalanche Energy (Note 3)	E_{AS}	122.5	mJ
Single Pulse Avalanche Current (Note 3)	I_{AS}	3.5	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	Limit	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	1.5	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62	°C/W

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	BV_{DSS}	500	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	2.5	3.3	4.5	V
Gate Body Leakage	$V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 500\text{V}, V_{GS} = 0\text{V}$	I_{DSS}	--	--	1	μA
Drain-Source On-State Resistance (Note 4)	$V_{GS} = 10\text{V}, I_D = 2.4\text{A}$	$R_{DS(on)}$	--	1.2	1.38	Ω
Dynamic (Note 5)						
Total Gate Charge	$V_{DS} = 400\text{V}, I_D = 4.8\text{A},$ $V_{GS} = 10\text{V}$	Q_g	--	15	--	nC
Gate-Source Charge		Q_{gs}	--	4	--	
Gate-Drain Charge		Q_{gd}	--	7	--	
Input Capacitance	$V_{DS} = 50\text{V}, V_{GS} = 0\text{V},$ $f = 1.0\text{MHz}$	C_{iss}	--	586	--	pF
Output Capacitance		C_{oss}	--	45	--	
Reverse Transfer Capacitance		C_{rss}	--	1	--	
Gate Resistance	$f = 1.0\text{MHz}$	R_g	--	2.9	5.8	Ω
Switching (Note 6)						
Turn-On Delay Time	$V_{DD} = 250\text{V}, R_G = 5\Omega,$ $I_D = 4.8\text{A}, V_{GS} = 10\text{V}$	$t_{d(on)}$	--	8.2	--	ns
Turn-On Rise Time		t_r	--	20.4	--	
Turn-Off Delay Time		$t_{d(off)}$	--	15.4	--	
Turn-Off Fall Time		t_f	--	20	--	
Source-Drain Diode						
Forward Voltage (Note 4)	$I_S = 4.8\text{A}, V_{GS} = 0\text{V}$	V_{SD}	--	--	1.3	V
Reverse Recovery Time	$I_S = 4.8\text{A}$	t_{rr}	--	205	--	ns
Reverse Recovery Charge	$di_f/dt = 100\text{A}/\mu\text{s}$	Q_{rr}	--	1.5	--	μC

Notes:

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3. $L = 20\text{mH}, I_{AS} = 3.5\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
4. Pulse test: $PW \leq 300\mu\text{s}$, duty cycle $\leq 2\%$
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

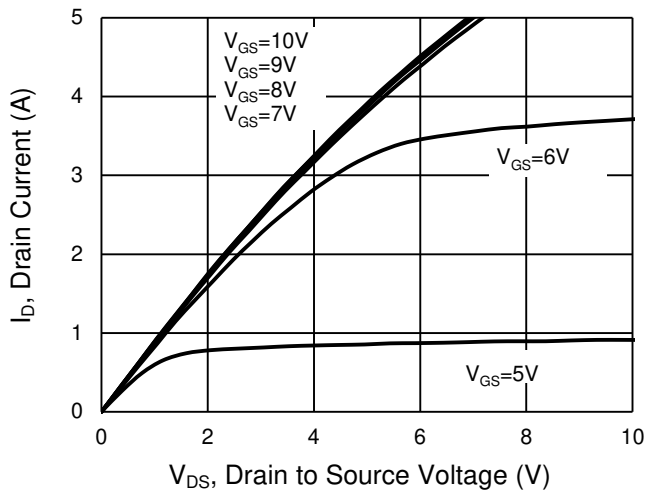
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM5NC50CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel

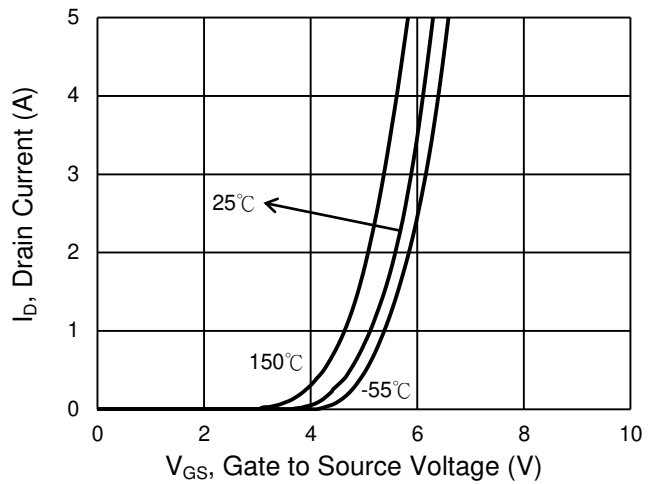
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

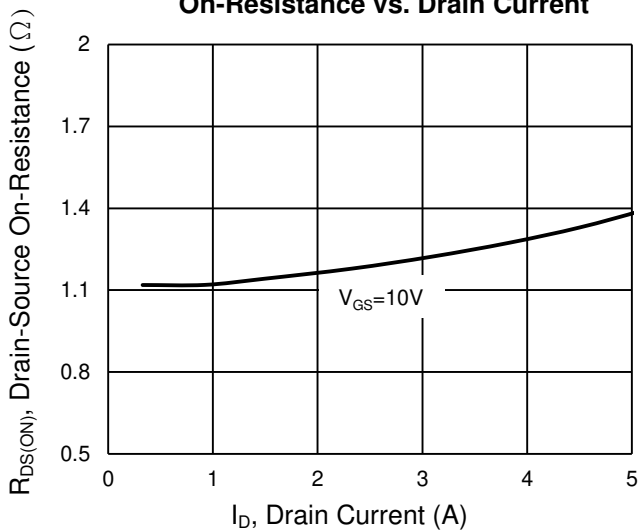
Output Characteristics



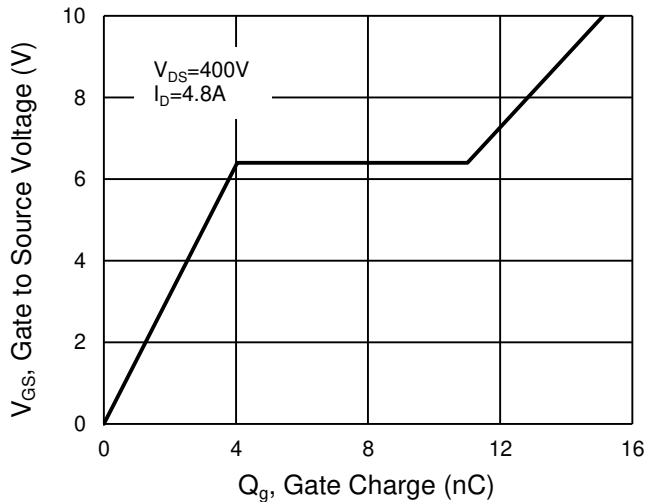
Transfer Characteristics



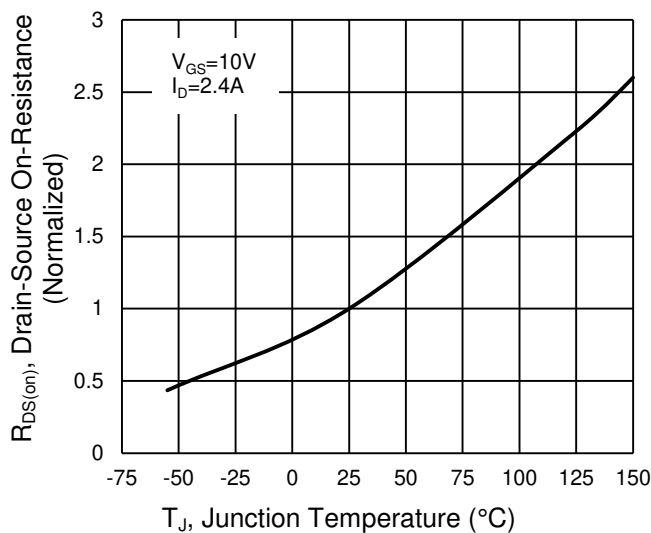
On-Resistance vs. Drain Current



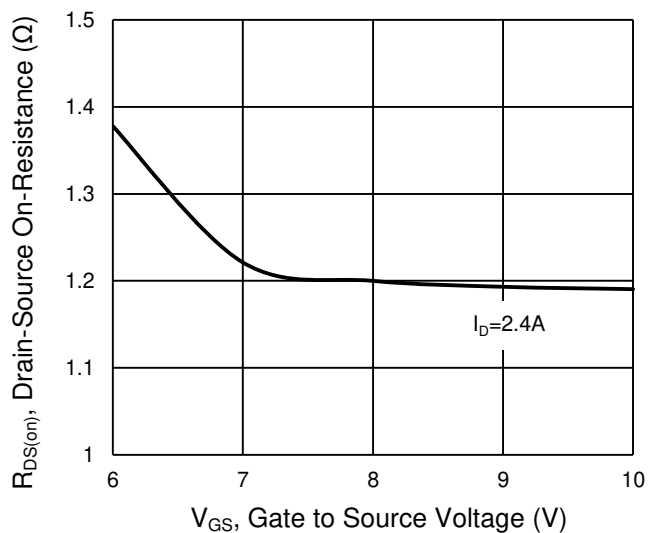
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



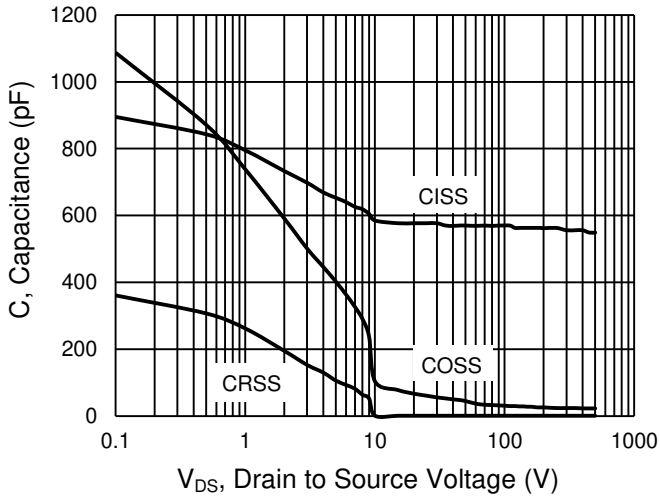
On-Resistance vs. Gate-Source Voltage



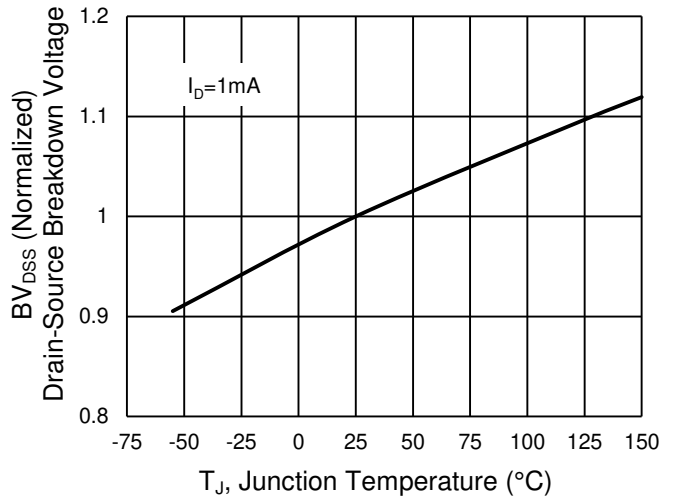
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

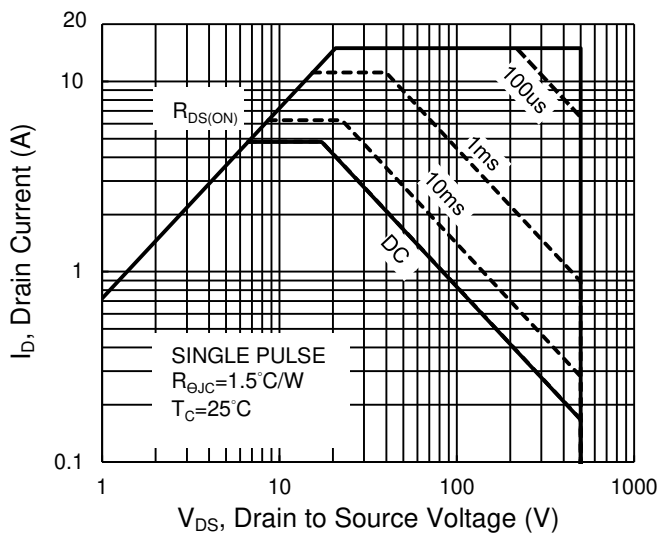
Capacitance vs. Drain-Source Voltage



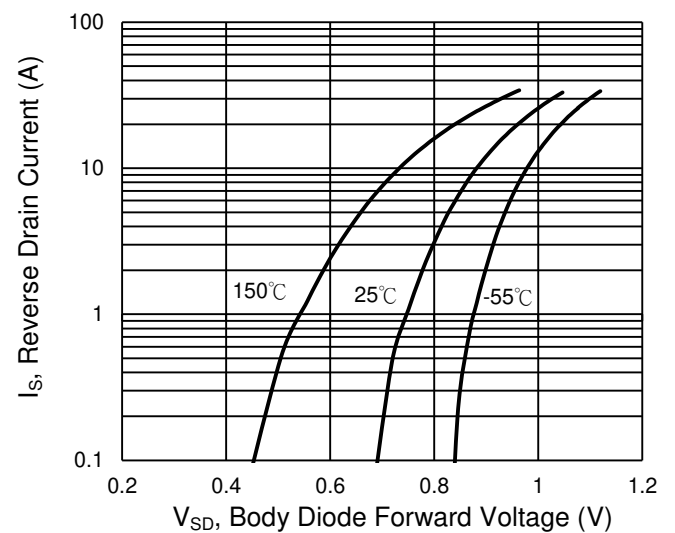
BV_{DSS} vs. Junction Temperature



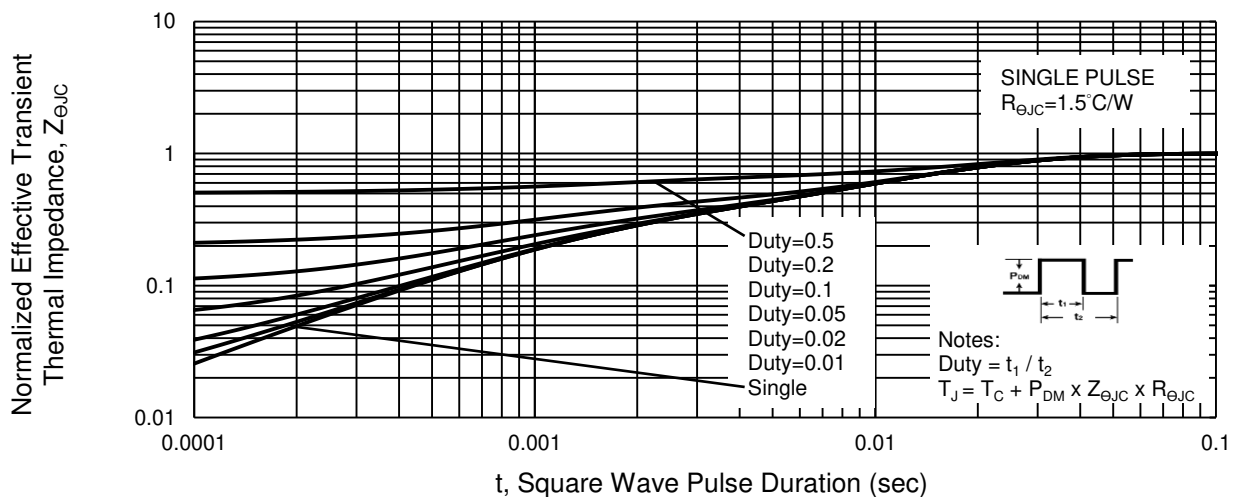
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

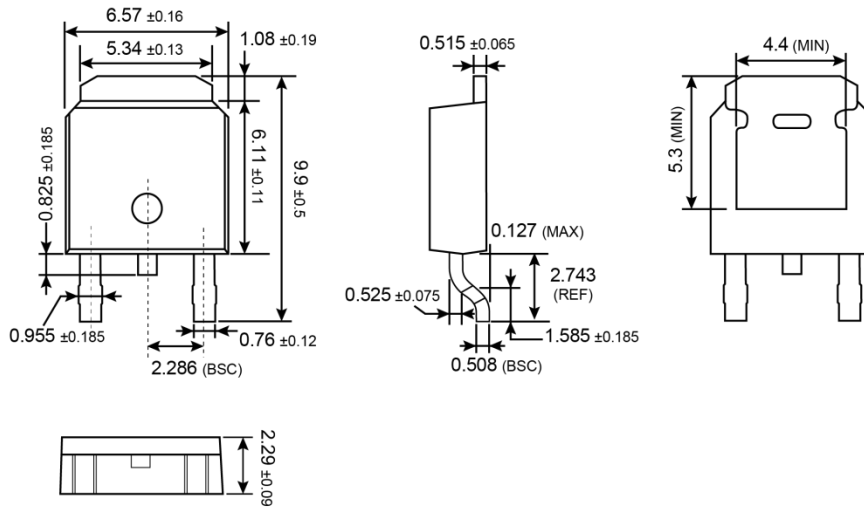


Normalized Thermal Transient Impedance, Junction-to-Case

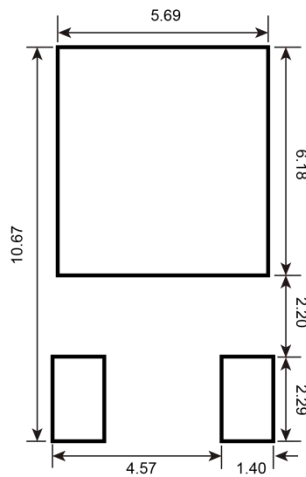


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

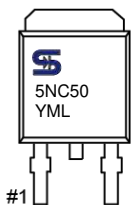
TO-252



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- Y** = Year Code
- M** = Month Code
- O** =Jan **P** =Feb **Q** =Mar **R** =Apr
- S** =May **T** =Jun **U** =Jul **V** =Aug
- W** =Sep **X** =Oct **Y** =Nov **Z** =Dec
- L** = Lot Code (1~9, A~Z)

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