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# **N-Channel Power MOSFET**

600V, 8A, 0.6Ω

#### **FEATURES**

- Super-Junction technology
- High performance due to small figure-of-merit
- High ruggedness performance
- High commutation performance

ΔD	DI	IC	ION

- Power Supply
- Lighting

KEY PERFORMANCE PARAMETERS				
PARAMETER VALUE UNIT				
$V_{DS}$	600	V		
R <sub>DS(on)</sub> (max)	0.6	Ω		
Q <sub>g</sub>	13	nC		



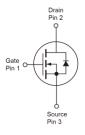












Notes: MSL 3 (Moisture Sensitivity Level) for TO-252 (D-PAK) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C unless otherwise noted)						
PARAMETER		SYMBOL	ITO-220	IPAK/DPAK	UNIT	
Drain-Source Voltage		$V_{DS}$	600		V	
Gate-Source Voltage		$V_{GS}$	±30		V	
Continuous Drain Current (Note 1)	$T_C = 25^{\circ}C$		8 4.8		A	
	$T_C = 100$ °C	- I <sub>D</sub>				
Pulsed Drain Current (Note 2)		I <sub>DM</sub>	24		Α	
Total Power Dissipation @ T <sub>C</sub> = 25°C		P <sub>DTOT</sub>	32	83	W	
Single Pulsed Avalanche Energy (Note 3)		E <sub>AS</sub>	100		mJ	
Single Pulsed Avalanche Current (Note 3)		I <sub>AS</sub>	2		Α	
Operating Junction and Storage Temperature Range		$T_J, T_{STG}$	- 55 to +150		°C	

THERMAL PERFORMANCE					
PARAMETER	SYMBOL	ITO-220	IPAK/DPAK	TINU	
Junction to Case Thermal Resistance	R <sub>eJC</sub>	3.9 1.5		°C/W	
Junction to Ambient Thermal Resistance	R <sub>eJA</sub>	62		°C/W	

**Notes:**  $R_{\Theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins.  $R_{\Theta JA}$  is guaranteed by design while  $R_{\Theta CA}$  is determined by the user's board design.  $R_{\Theta JA}$  shown below for single device operation on FR-4 PCB in still air.





<b>ELECTRICAL SPECIFICATIONS</b> (T <sub>A</sub> = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV <sub>DSS</sub>	600			V
Gate Threshold Voltage	$V_{DS} = V_{GS}, \ I_D = 250 \mu A$	$V_{GS(TH)}$	2.0	3.0	4.0	V
Gate Body Leakage	$V_{GS} = \pm 30V$ , $V_{DS} = 0V$	I <sub>GSS</sub>			±100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 600V, V_{GS} = 0V$	I <sub>DSS</sub>			1	μΑ
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 4A$	R <sub>DS(on)</sub>		0.49	0.6	Ω
Dynamic (Note 5)						
Total Gate Charge	.,	$Q_g$		13		
Gate-Source Charge	$V_{DS} = 380V, I_D = 8A,$	$Q_{gs}$		3		nC
Gate-Drain Charge	$V_{GS} = 10V$	$Q_{gd}$		4		
Input Capacitance	$V_{DS} = 100V, V_{GS} = 0V,$	C <sub>iss</sub>		743		. =
Output Capacitance	f = 1.0MHz	C <sub>oss</sub>		66		pF
Gate Resistance	F = 1MHz, open drain	$R_g$		3.2		Ω
Switching (Note 6)						
Turn-On Delay Time		t <sub>d(on)</sub>		21		
Turn-On Rise Time	$V_{DD} = 380V,$ $R_{GEN} = 25\Omega,$ $I_{D} = 8A, V_{GS} = 10V,$	t <sub>r</sub>		15		
Turn-Off Delay Time		t <sub>d(off)</sub>		40		ns
Turn-Off Fall Time	$I_D = OA$ , $V_{GS} = TOV$ ,	t <sub>f</sub>		9		
Source-Drain Diode (Note 4)						
Forward On Voltage	I <sub>S</sub> = 8A, V <sub>GS</sub> = 0V	$V_{SD}$			1.4	V
Reverse Recovery Time	V <sub>B</sub> =200V, I <sub>S</sub> = 4A	t <sub>rr</sub>		185		ns
Reverse Recovery Charge	$dI_F/dt = 100A/\mu s$	Q <sub>rr</sub>		1.4		μC

#### Notes:

- 1. Current limited by package
- 2. Pulse width limited by the maximum junction temperature
- 3. L = 50mH,  $I_{AS} = 2A$ ,  $V_{DD} = 50V$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^{\circ}C$
- 4. Pulse test: PW  $\leq$  300 $\mu$ s, duty cycle  $\leq$  2%
- 5. For DESIGN AID ONLY, not subject to production testing.
- 6. Switching time is essentially independent of operating temperature.





# **ORDERING INFORMATION**

PART NO.	PACKAGE	PACKING	
TSM60N600CI C0G	ITO-220	50pcs / Tube	
TSM60N600CH C5G	TO-251 (IPAK)	75pcs / Tube	
TSM60N600CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel	

#### Note:

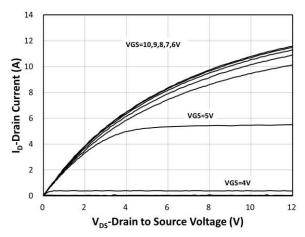
- 1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- 2. Halogen-free according to IEC 61249-2-21 definition



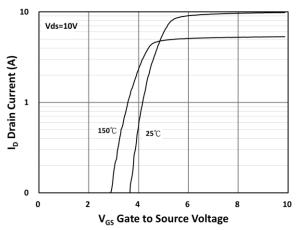
# **ELECTRICAL CHARACTERISTICS CURVES**

(T<sub>C</sub> = 25°C unless otherwise noted)

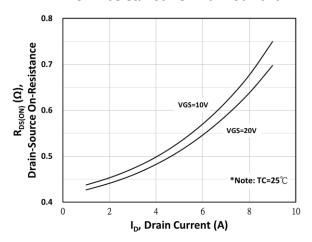
### **Output Characteristics**



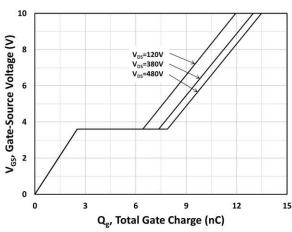
# **Transfer Characteristics**



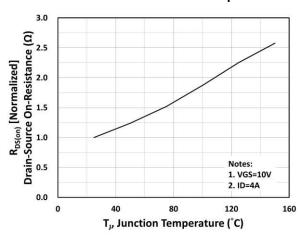
#### **On-Resistance vs. Drain Current**



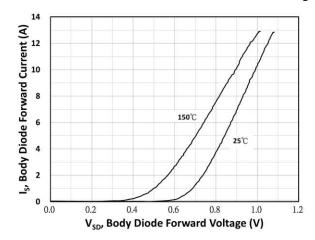
Gate-Source Voltage vs. Gate Charge



#### On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Current vs. Voltage



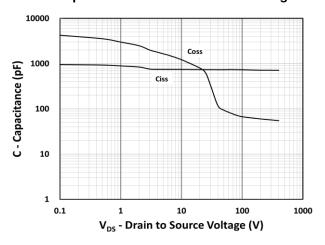
Version: C1706



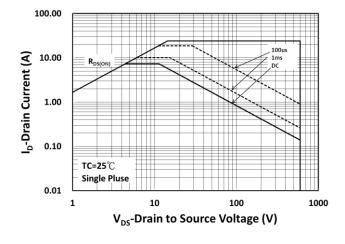
# **ELECTRICAL CHARACTERISTICS CURVES**

(T<sub>C</sub> = 25°C unless otherwise noted)

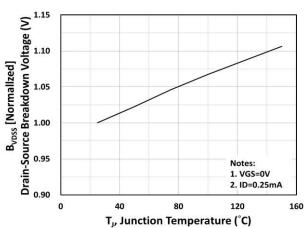
### Capacitance vs. Drain-Source Voltage



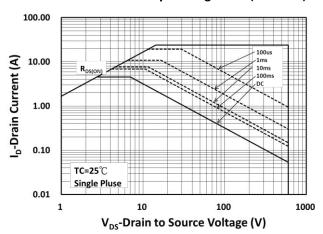
# Maximum Safe Operating Area (DPAK/IPAK)



BV<sub>DSS</sub> vs. Junction Temperature



#### **Maximum Safe Operating Area (ITO-220)**

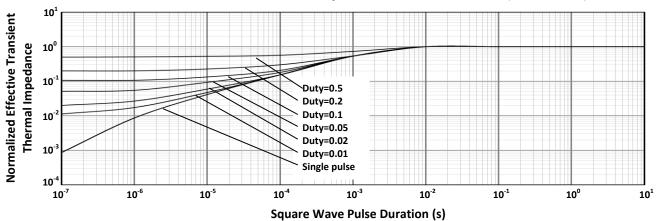




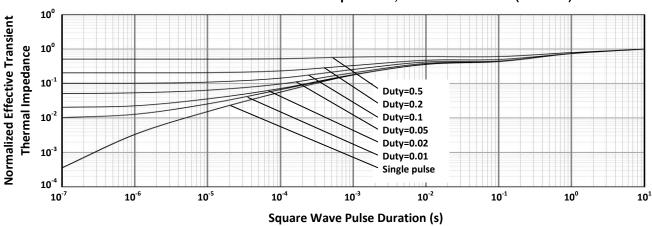
# **ELECTRICAL CHARACTERISTICS CURVES**

 $(T_C = 25^{\circ}C \text{ unless otherwise noted})$ 

#### Normalized Thermal Transient Impedance, Junction-to-Case (DPAK/IPAK)

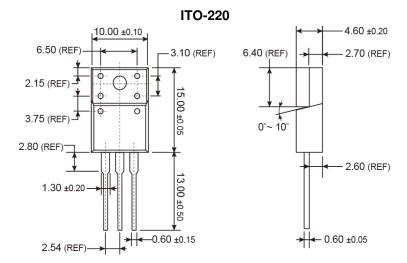


# Normalized Thermal Transient Impedance, Junction-to-Case (ITO-220)





# PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



# **MARKING DIAGRAM**



G = Halogen Free

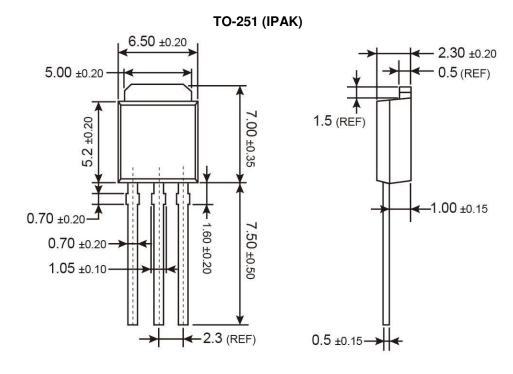
Y = Year Code

**WW** = Week Code  $(01 \sim 52)$ 

= Factory Code



# PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



# **MARKING DIAGRAM**



Y = Year Code

M = Month Code for Halogen Free Product

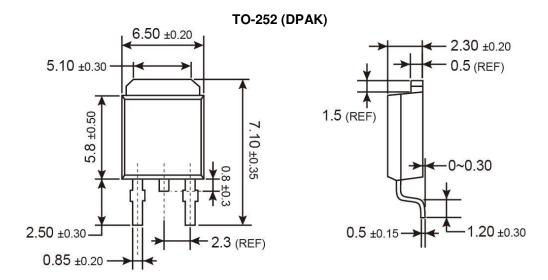
O =Jan P =Feb Q =Mar R =Apr S =May T =Jun U =Jul V =Aug

W =Sep X =Oct Y =Nov Z =Dec

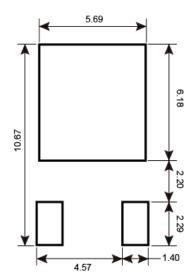
**L** = Lot Code (1~9, A~Z)



# PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



# **SUGGESTED PAD LAYOUT**



# **MARKING DIAGRAM**



Y = Year Code

M = Month Code for Halogen Free Product

O =Jan P =Feb Q =Mar R =Apr

S = May T = Jun U = Jul V = Aug

W = Sep X = Oct Y = Nov Z = Dec

 $\mathbf{L} = \text{Lot Code } (1 \sim 9, A \sim Z)$ 





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