Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

N-Channel Power MOSFET

150V, 9A, 65mΩ

FEATURES

- Low $R_{DS(ON)}$ to minimize conductive losses
- Low gate charge for fast power switching
- 100% UIS and R_g tested
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

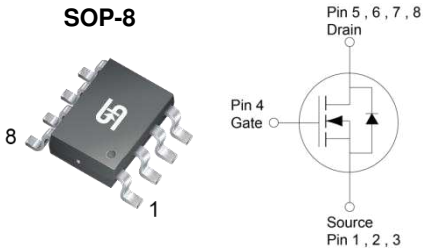
APPLICATIONS

- PoE
- LED Lighting
- Telecom Power

KEY PERFORMANCE PARAMETERS			
PARAMETER		**VALUE**	**UNIT**
V_{DS}		150	V
$R_{DS(on)}$ (max)	V_{GS} = 10V	65	mΩ
	V_{GS} = 6V	80	
Q_g		37	nC

Pb-Free RoHS COMPLIANT HALOGEN FREE

SOP-8



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	150	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	9	A
	T_A = 25°C		4	
Pulsed Drain Current		I_{DM}	36	A
Single Pulse Avalanche Current (Note 2)		I_{AS}	20	A
Single Pulse Avalanche Energy (Note 2)		E_{AS}	60	mJ
Total Power Dissipation	T_C = 25°C	P_D	12.5	W
	T_C = 125°C		2.5	
Total Power Dissipation	T_A = 25°C	P_D	2.2	W
	T_A = 125°C		0.4	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Junction to Case Thermal Resistance	$R_{\Theta JC}$	10	°C/W
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	57	°C/W

Thermal Performance Note: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design.

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	150	--	--	V
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	$V_{GS(TH)}$	2	2.7	4	V
Gate-Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Drain-Source Leakage Current	V_{GS} = 0V, V_{DS} = 150V	I_{DSS}	--	--	1	μA
	V_{GS} = 0V, V_{DS} = 150V T_J = 125°C		--	--	100	
Drain-Source On-State Resistance (Note 3)	V_{GS} = 10V, I_D = 4A	$R_{DS(on)}$	--	51	65	mΩ
	V_{GS} = 6V, I_D = 4A		--	59	80	
Forward Transconductance (Note 3)	V_{DS} = 5V, I_D = 4A	g_{fs}	--	11	--	S
Dynamic (Note 4)						
Total Gate Charge	V_{GS} = 10V, V_{DS} = 75V, I_D = 4A	Q_g	--	37	--	nC
Total Gate Charge	V_{GS} = 6V, V_{DS} = 75V, I_D = 4A	Q_g	--	24	--	
Gate-Source Charge		Q_{gs}	--	9	--	
Gate-Drain Charge		Q_{gd}	--	12	--	
Input Capacitance	V_{GS} = 0V, V_{DS} = 75V f = 1.0MHz	C_{iss}	--	1783	--	pF
Output Capacitance		C_{oss}	--	94	--	
Reverse Transfer Capacitance		C_{rss}	--	18	--	
Gate Resistance	f = 1.0MHz, open drain	R_g	0.4	1.3	2.6	Ω
Switching (Note 4)						
Turn-On Delay Time	V_{GS} = 10V, V_{DS} = 75V, I_D = 4A, R_G = 2Ω,	$t_{d(on)}$	--	7	--	ns
Turn-On Rise Time		t_r	--	5	--	
Turn-Off Delay Time		$t_{d(off)}$	--	17	--	
Turn-Off Fall Time		t_f	--	11	--	
Source-Drain Diode						
Forward Voltage (Note 3)	V_{GS} = 0V, I_S = 4A	V_{SD}	--	--	1	V
Reverse Recovery Time	I_S = 4A , dI/dt = 100A/μs	t_{rr}	--	50	--	ns
Reverse Recovery Charge		Q_{rr}	--	97	--	nC

Notes:

1. Silicon limited current only.
2. L = 0.3mH, V_{GS} = 10V, V_{DD} = 50V, R_G = 25Ω, I_{AS} = 18A, Starting T_J = 25°C
3. Pulse test: Pulse Width ≤ 300μs, duty cycle ≤ 2%.
4. Switching time is essentially independent of operating temperature.

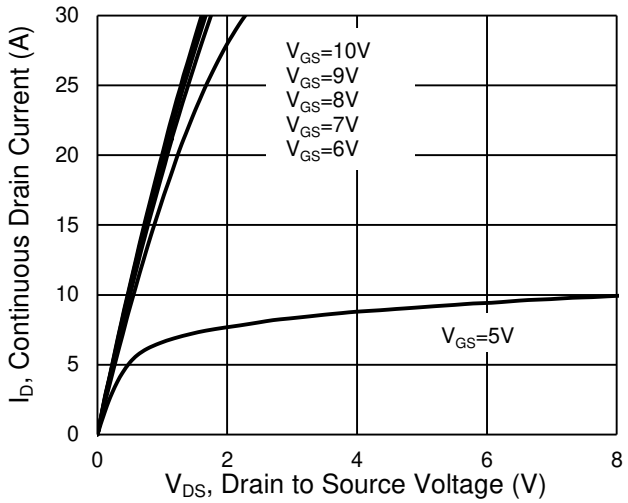
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM650N15CS RLG	SOP-8	2,500pcs / 13” Reel

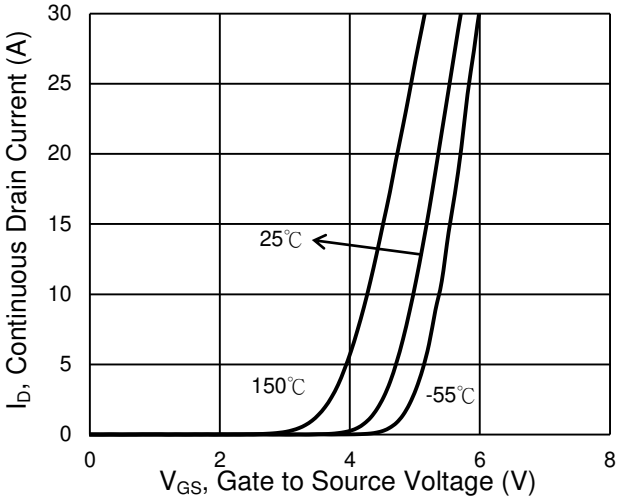
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

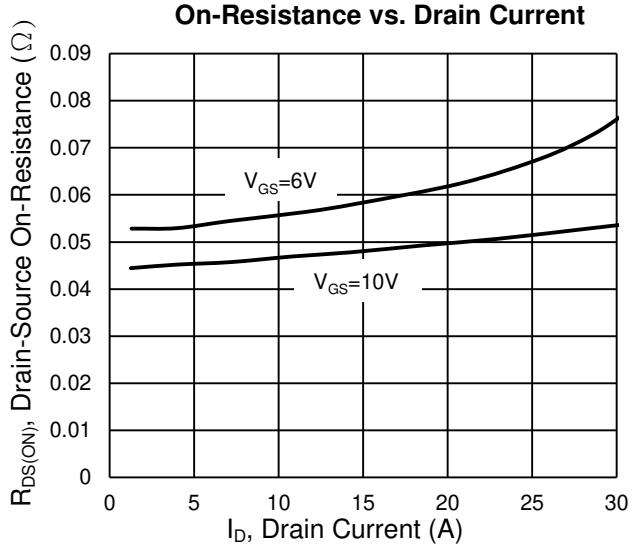
Output Characteristics



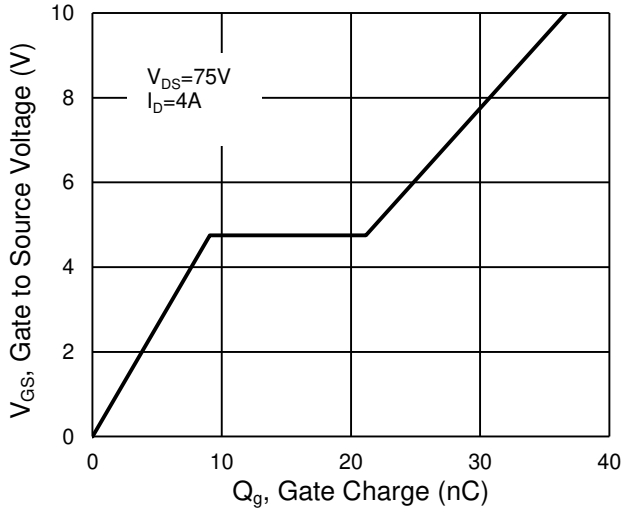
Transfer Characteristics



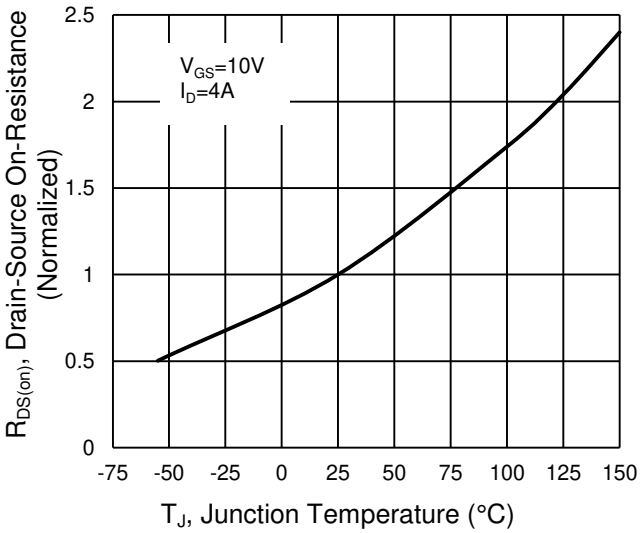
On-Resistance vs. Drain Current



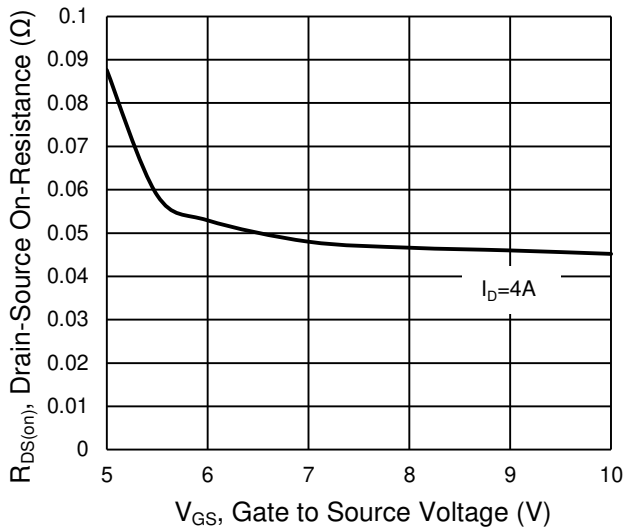
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



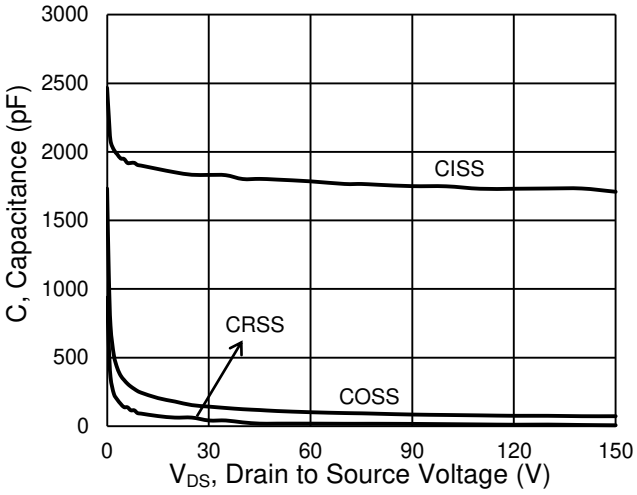
On-Resistance vs. Gate-Source Voltage



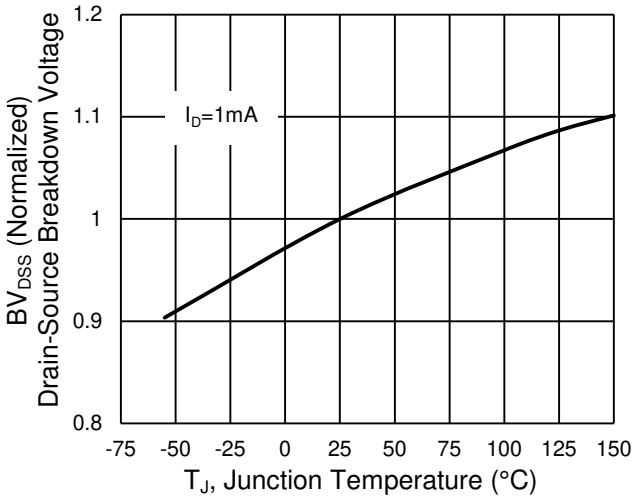
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

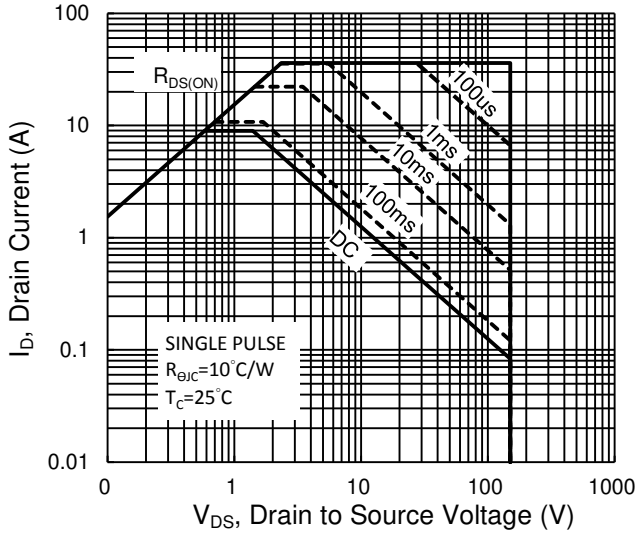
Capacitance vs. Drain-Source Voltage



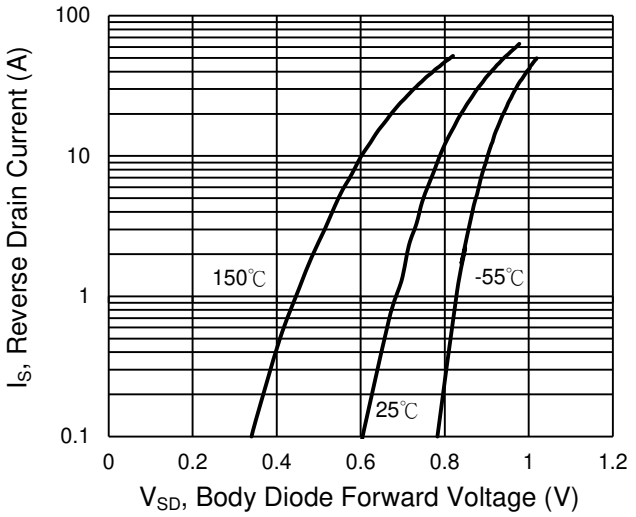
BV_{DSS} vs. Junction Temperature



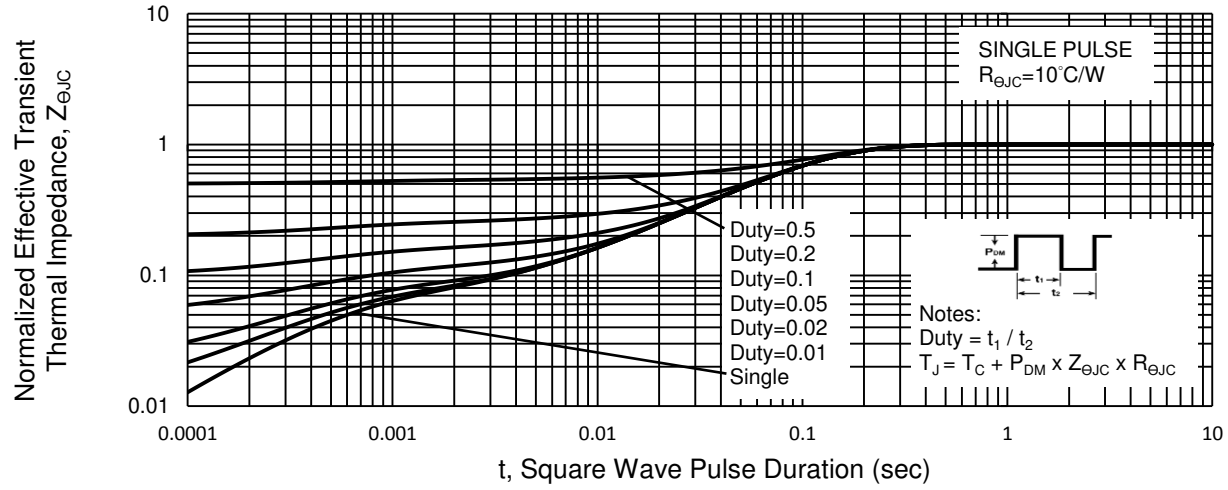
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

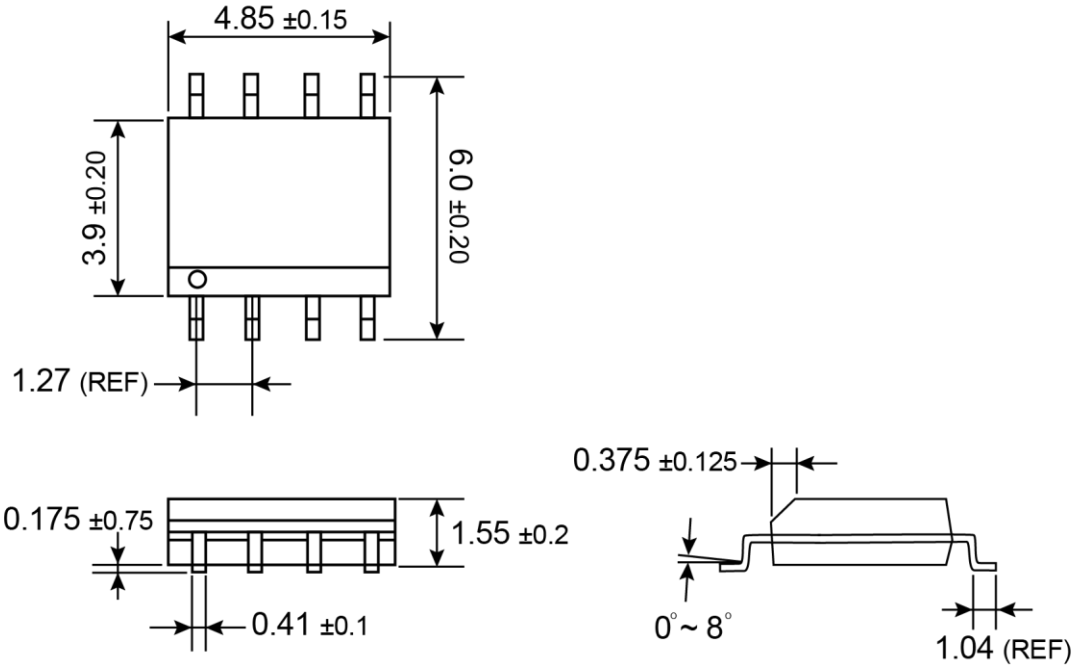


Normalized Thermal Transient Impedance, Junction-to-Case

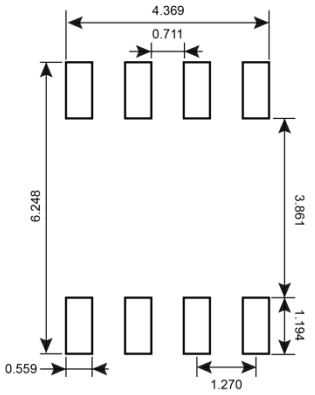


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

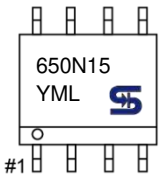
SOP-8



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



Y = Year Code

M = Month Code

O	=Jan	**P**	=Feb	**Q**	=Mar	**R**	=Apr
S	=May	**T**	=Jun	**U**	=Jul	**V**	=Aug
W	=Sep	**X**	=Oct	**Y**	=Nov	**Z**	=Dec

L = Lot Code (1~9, A~Z)

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