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N-Channel Power MOSFET

 $800V, 6A, 0.95\Omega$

FEATURES

- Super-Junction technology
- High performance due to small figure-of-merit
- High ruggedness performance
- High commutation performance
- Pb-free plating
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21 definition

| KEY PERFORMANCE PARAMETERS | | | | |
|----------------------------|------|----|--|--|
| PARAMETER VALUE UNIT | | | | |
| V_{DS} | 800 | V | | |
| R _{DS(on)} (max) | 0.95 | Ω | | |
| Q_g | 19.6 | nC | | |







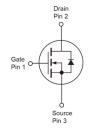
Version: B1706

APPLICATION

- Power Supply
- Lighting

TO-251 (IPAK)





Notes: MSL 3 (Moisture Sensitivity Level) for TO-252 (D-PAK) per J-STD-020

| ABSOLUTE MAXIMUM RATINGS (T _A = 25°C unless otherwise noted) | | | | |
|---|-----------------------|-----------------------------------|--------------|------|
| PARAMETER | | SYMBOL | LIMIT | UNIT |
| Drain-Source Voltage | | V _{DS} | 800 | V |
| Gate-Source Voltage | | V _{GS} | ±30 | V |
| Continuous Drain Current (Note 1) | T _C = 25°C | | 6 | А |
| | $T_C = 100$ °C | I _D | 3.8 | Α |
| Pulsed Drain Current (Note 2) | | I _{DM} | 18 | Α |
| Total Power Dissipation @ T _C = 25°C | | P _{DTOT} | 110 | W |
| Single Pulsed Avalanche Energy (Note | 93) | E _{AS} | 121 | mJ |
| Single Pulsed Avalanche Current (Not | e 3) | I _{AS} | 2.2 | Α |
| Operating Junction and Storage Tem | perature Range | T _J , T _{STG} | - 55 to +150 | °C |

TO-252 (DPAK)





| THERMAL PERFORMANCE | | | | |
|--|------------------|-------|------|--|
| PARAMETER | SYMBOL | LIMIT | UNIT | |
| Junction to Case Thermal Resistance | R _{eJC} | 1.14 | °C/W | |
| Junction to Ambient Thermal Resistance | R _{eJA} | 62 | °C/W | |

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB with minimum recommended footprint in still air.

| PARAMETER | CONDITIONS | SYMBOL | MIN | TYP | MAX | UNIT |
|----------------------------------|---|---------------------|-----|------|------|------|
| Static (Note 4) | | | | | | |
| Drain-Source Breakdown Voltage | $V_{GS} = 0V, I_D = 250\mu A$ | BV _{DSS} | 800 | | | V |
| Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = 250 \mu A$ | $V_{GS(TH)}$ | 2 | | 4 | V |
| Gate Body Leakage | $V_{GS} = \pm 30V, V_{DS} = 0V$ | I _{GSS} | | | ±100 | nA |
| Zero Gate Voltage Drain Current | $V_{DS} = 800V, V_{GS} = 0V$ | I _{DSS} | | | 1 | μΑ |
| Drain-Source On-State Resistance | $V_{GS} = 10V, I_D = 3A$ | R _{DS(on)} | | 0.8 | 0.95 | Ω |
| Dynamic (Note 5) | | | | | | |
| Total Gate Charge | $V_{DS} = 380V, I_D = 6A,$ $V_{GS} = 10V$ | Q_g | | 19.6 | | |
| Gate-Source Charge | | Q_gs | | 3.5 | | nC |
| Gate-Drain Charge | | Q_{gd} | | 9.7 | |] |
| Input Capacitance | $V_{DS} = 100V, V_{GS} = 0V,$ | C _{iss} | | 691 | | _ |
| Output Capacitance | f = 1.0MHz | C _{oss} | | 63 | | pF |
| Gate Resistance | F = 1MHz, open drain | R_g | | 3.4 | | Ω |
| Switching (Note 6) | | | | | | |
| Turn-On Delay Time | $V_{DD} = 380V,$ $R_{GEN} = 25\Omega,$ $I_{D} = 6A, V_{GS} = 10V,$ | t _{d(on)} | | 23 | | |
| Turn-On Rise Time | | t _r | | 12 | | |
| Turn-Off Delay Time | | t _{d(off)} | | 57 | | ns |
| Turn-Off Fall Time | $\int_{0}^{\infty} \int_{0}^{\infty} \int_{0$ | t _f | | 11 | | |
| Source-Drain Diode (Note 4) | | | | | | |
| Forward On Voltage | $I_S = 6A$, $V_{GS} = 0V$ | V_{SD} | | | 1.4 | ٧ |
| Reverse Recovery Time | V _B = 100V, I _S = 6A | t _{rr} | | 249 | | ns |
| Reverse Recovery Charge | $dI_F/dt = 100A/\mu s$ | Q _{rr} | | 2.6 | | μC |

Notes:

- 1. Current limited by package.
- 2. Pulse width limited by the maximum junction temperature.
- 3. L = 50mH, $I_{AS} = 2.2A$, $V_{DD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}C$
- 4. Pulse test: PW \leq 300 μ s, duty cycle \leq 2%.
- 5. For DESIGN AID ONLY, not subject to production testing.
- 6. Switching time is essentially independent of operating temperature.





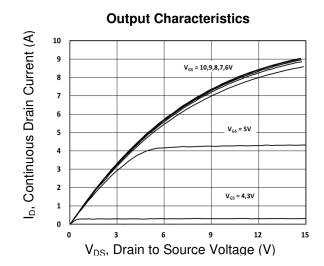
ORDERING INFORMATION

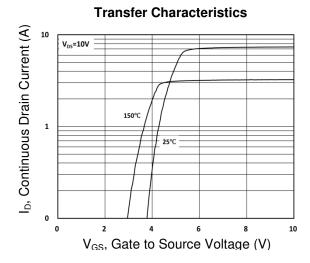
| PART NO. | PACKAGE | PACKING |
|-----------------|---------------|---------------------|
| TSM80N950CH C5G | TO-251 (IPAK) | 75pcs / Tube |
| TSM80N950CP ROG | TO-252 (DPAK) | 2,500pcs / 13" Reel |

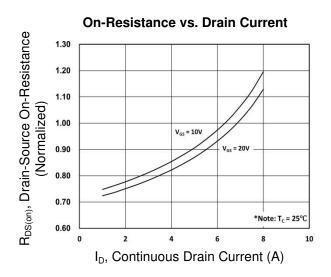


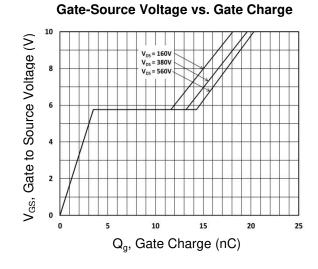
CHARACTERISTICS CURVES

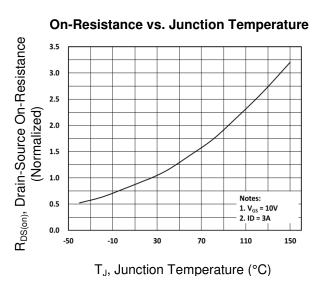
 $(T_C = 25^{\circ}C \text{ unless otherwise noted})$

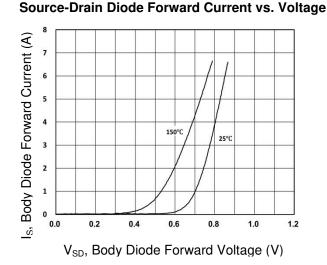










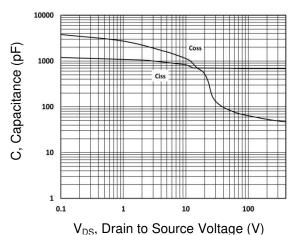




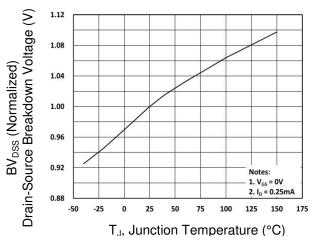
CHARACTERISTICS CURVES

 $(T_C = 25^{\circ}C \text{ unless otherwise noted})$

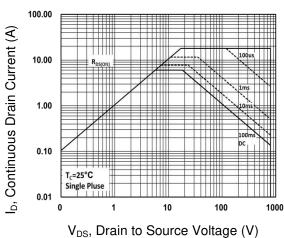
Capacitance vs. Drain-Source Voltage



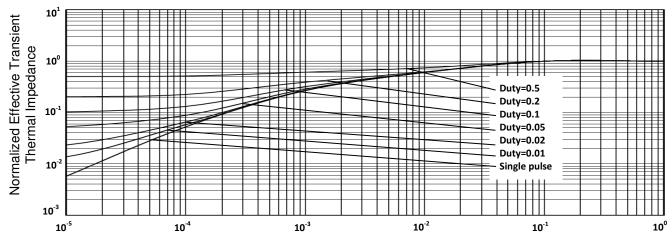
BV_{DSS} vs. Junction Temperature



Maximum Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



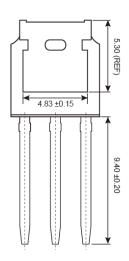
Square Wave Pulse Duration (s)



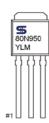


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-251 (IPAK) 6.60 ±0.20 5.33 ±0.15 1.02 (REF) 0.53 ±0.05 ->- 6.10 ± 0.10 1.07 ±0.10 0.82 ±0.05 → 2.28 (BSC) ← 0.78 ±0.10 0.53 (BSC) →



MARKING DIAGRAM



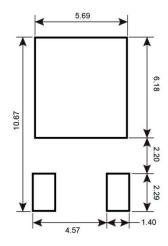
- Y = Year Code
- **M** = Month Code for Halogen Free Product
 - **P** =Feb O =Jan
 - $\mathbf{Q} = \mathbf{Mar} \quad \mathbf{R} = \mathbf{Apr}$
- - S =May **T** =Jun
- **W** =Sep **X** =Oct
- **U** =Jul **V** =Aug
- Y =Nov Z =Dec
- **L** = Lot Code $(1\sim9, A\sim Z)$



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-252 (DPAK) 6.60 ±0.20 1.10 (REF) 1.07 ±0.10 1.07 ±0.10 1.07 ±0.10 1.07 ±0.10 1.07 ±0.10 1.07 ±0.10

SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



Y = Year Code

M = Month Code for Halogen Free Product

O =Jan P =Feb Q =Mar R =Apr

 $S = May \quad T = Jun \quad U = Jul \quad V = Aug$

 $W = Sep \quad X = Oct \quad Y = Nov \quad Z = Dec$ L = Lot Code (1~9, A~Z)





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