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N-Channel Power MOSFET

100V, 15A, 90mΩ

FEATURES

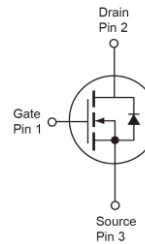
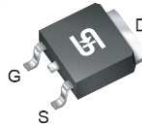
- 100% avalanche tested
- Low gate charge for fast switching
- Pb-free plating
- RoHS compliant
- Halogen-free mold compound

APPLICATION

- Networking
- Load Switching
- LED Lighting Control
- AC-DC Secondary Rectification

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V_{DS}	100	V
$R_{DS(on)}$ (max)	$V_{GS} = 10V$	90
	$V_{GS} = 4.5V$	100
Q_g	9.3	nC


**TO-251S
(IPAK SL)**

**TO-252
(DPAK)**

Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current (Note 1)	I_D	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Pulsed Drain Current (Note 2)	I_{DM}	60	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_{DTOT}	50	W
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	18	mJ
Single Pulsed Avalanche Current (Note 3)	I_{AS}	6	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62	$^\circ\text{C/W}$

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static ^(Note 4)						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	BV _{DSS}	100	--	--	V
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	V _{GS(TH)}	1.2	1.6	2.5	V
Gate Body Leakage	V _{GS} = ±20V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V _{DS} = 100V, V _{GS} = 0V	I _{DSS}	--	--	1	μA
Drain-Source On-State Resistance	V _{GS} = 10V, I _D = 5A	R _{DS(on)}	--	72	90	mΩ
	V _{GS} = 4.5V, I _D = 3A			75	100	
Dynamic ^(Note 5)						
Total Gate Charge	V _{DS} = 48V, I _D = 5A, V _{GS} = 10V	Q _g	--	9.3	--	nC
Gate-Source Charge		Q _{gs}	--	2.1	--	
Gate-Drain Charge		Q _{gd}	--	1.8	--	
Input Capacitance	V _{DS} = 50V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	1480	--	pF
Output Capacitance		C _{oss}	--	480	--	
Reverse Transfer Capacitance		C _{rss}	--	35	--	
Gate Resistance	F = 1MHz, open drain	R _g	--	1.3	--	Ω
Switching ^(Note 6)						
Turn-On Delay Time	V _{DD} = 30V, R _{GEN} = 3.3Ω, I _D = 1A, V _{GS} = 10V,	t _{d(on)}	--	2.9	--	ns
Turn-On Rise Time		t _r	--	9.5	--	
Turn-Off Delay Time		t _{d(off)}	--	18.4	--	
Turn-Off Fall Time		t _f	--	5.3	--	
Source-Drain Diode ^(Note 4)						
Forward On Voltage	I _S = 3.3A, V _{GS} = 0V	V _{SD}	--	--	1	V
Continuous Drain-Source Diode	V _G =V _D =0V, Force Current	I _S	--	--	15	A
Pulse Drain-Source Diode		I _{SM}	--	--	60	A

Notes:

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3. $L = 0.1\text{mH}, I_{AS} = 6A, V_{DD} = 50V, R_G = 25\Omega, \text{Starting } T_J = 25^\circ\text{C}$
4. Pulse test: $PW \leq 300\mu s, \text{duty cycle} \leq 2\%$
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

ORDERING INFORMATION (EXAMPLE)

PART NO.	PACKAGE	PACKING
TSM900N10CH X0G	TO-251S (IPAK SL)	75pcs / Tube
TSM900N10CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel

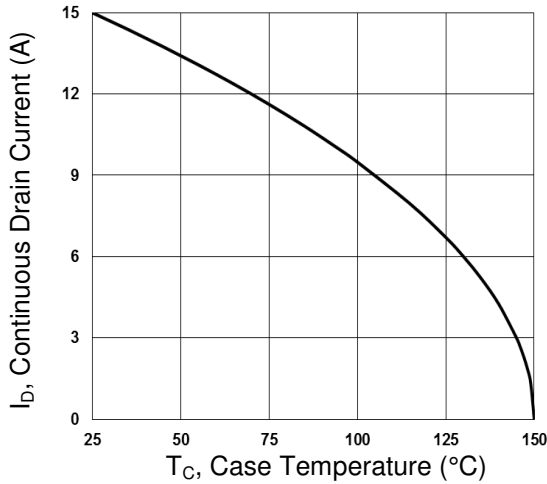
Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

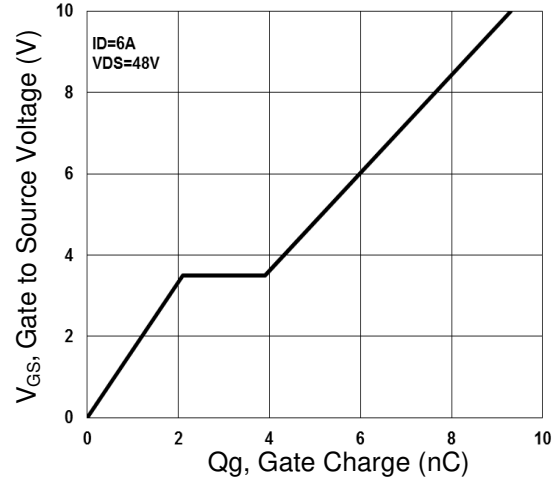
CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

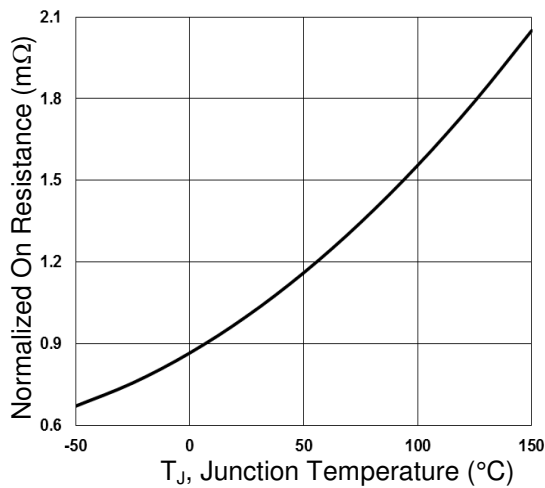
Continuous Drain Current vs. T_C



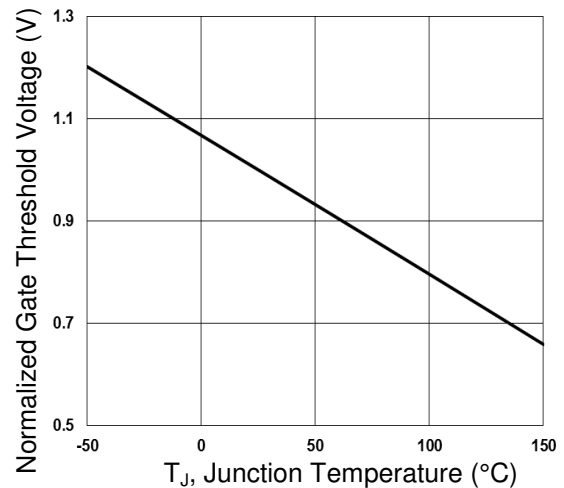
Gate Charge



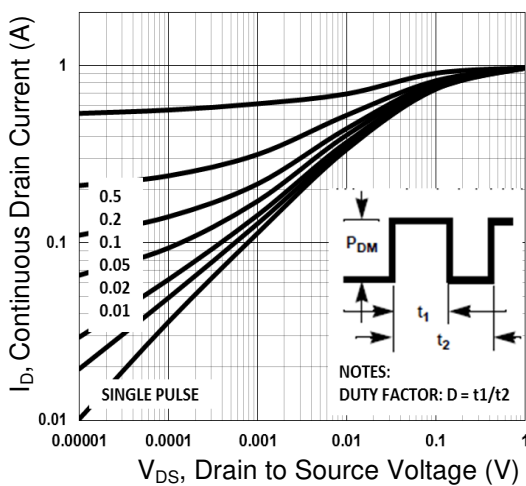
On-Resistance vs. Junction Temperature



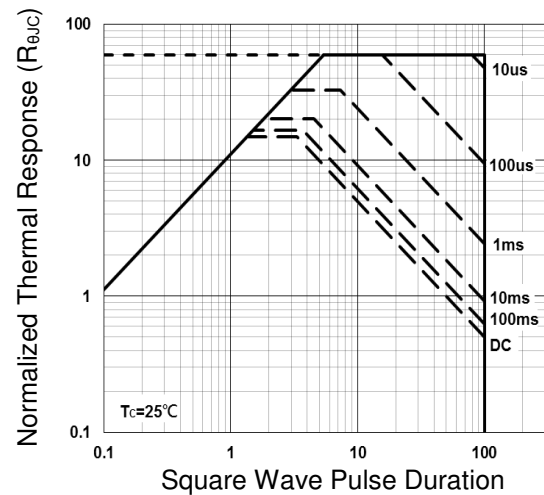
Threshold Voltage vs. Junction Temperature



Maximum Safe Operating Area

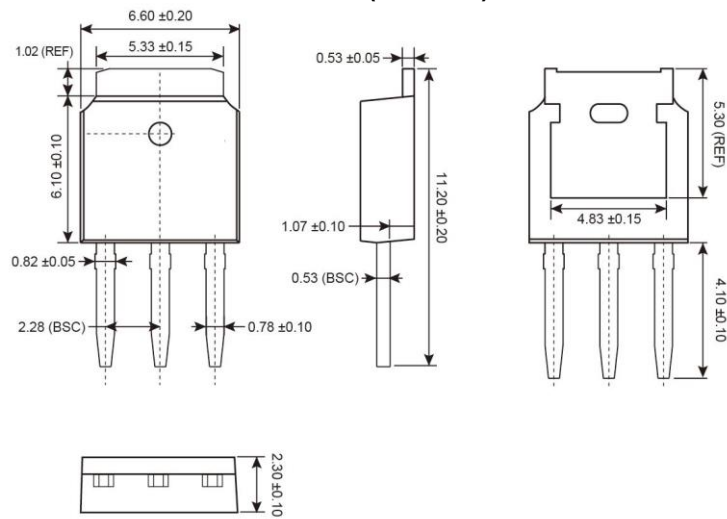


Normalized Thermal Transient Impedance Curve

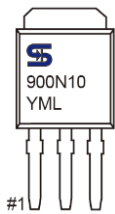


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-251S (IPAK SL)



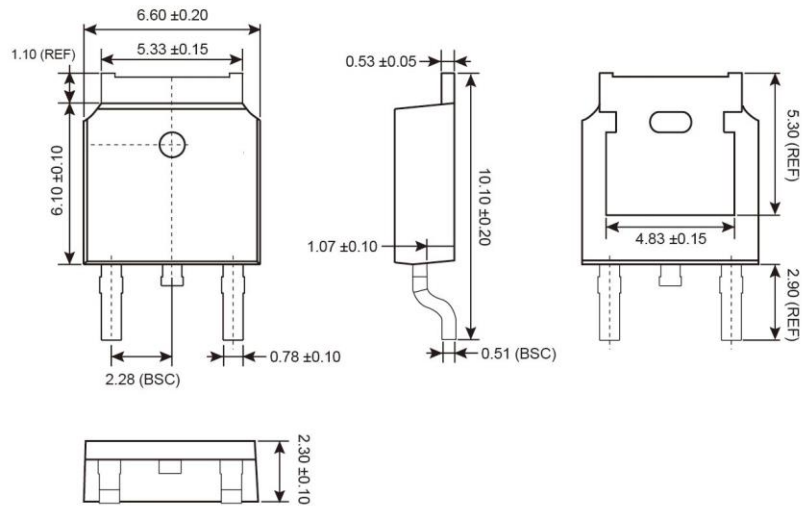
MARKING DIAGRAM



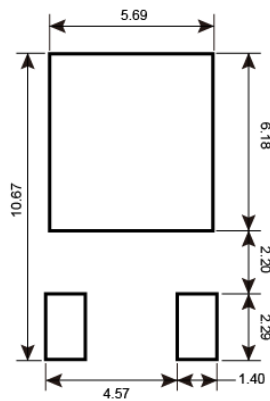
Y = Year Code
M = Month Code for Halogen Free Product
O =Jan **P** =Feb **Q** =Mar **R** =Apr
S =May **T** =Jun **U** =Jul **V** =Aug
W =Sep **X** =Oct **Y** =Nov **Z** =Dec
L = Lot Code (1~9, A~Z)

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

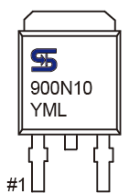
TO-252 (DPAK)



SUGGESTED PAD LAYOUT



MARKING DIAGRAM



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