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## Features

- Superscalar (3 Instructions per Clock Peak)
- Dual 16 KB Caches
- Selectable Bus Clock
- 32-bit Compatibility PowerPC Implementation
- On-chip Debug Support
- Nap, Doze and Sleep Power Saving Modes
- Device Offered in Cerquad, CBGA 255, HiTCE CBGA 255 and CI-CGA 255

### Features Specific to CBGA 255, HiTCE CBGA 255 and CI-CGA 255

- 7.4 SPECint95, 6.1 SPECfp95 at 300 MHz (Estimated)
- $P_D$ Typically = 3.5W (266 MHz), Full Operating Conditions
- Branch Folding
- 64-bit Data Bus (32-bit Data Bus Option)
- 4-Gbytes Direct Addressing Range
- Pipelined Single/Double Precision Float Unit
- IEEE 754 Compatible FPU
- IEEE P 1149-1 Test Mode (JTAG/C0P)
- $f_{INT}$ Max = 300 MHz
- $f_{BUS}$ Max = 75 MHz
- Compatible CMOS Input/TTL Output

### Features Specific to Cerquad

- 5.6 SPECint95, 4 SPECfp95 and 200 MHz (Estimated)
- $P_D$ Typically = 2.5W (200 MHz), Full Operating Conditions

# PowerPC® 603e RISC Microprocessor Family PID7t-603e

# TSPC603R

## 1. Description

The PID7t-603e implementation of the PowerPC 603e (renamed after the 603R) is a low-power implementation of the Reduced Instruction Set Computer (RISC) microprocessor PowerPC family. The 603R is pin-to-pin compatible with the PowerPC 603e and 603P in a Cerquad package. The 603R implements 32-bit effective addresses, integer data types of 8, 16 and 32 bits, and floating-point data types of 32 and 64 bits.

The 603R is a low-power 2.5/3.3V design and provides four software controllable power-saving modes. This device is a superscalar processor capable of issuing and retiring as many as three instructions per clock. Instructions can be executed in any order for increased performance, but, the 603R makes completion appear sequential. It integrates five execution units and is able to execute five instructions in parallel.

The 603R provides independent on-chip, 16-Kbyte, four-way set-associative, physically addressed caches for instructions and data, as well as on-chip instructions, and data Memory Management Units (MMUs). The MMUs contain 64-entry, two-way set-associative, data and instruction translation look aside buffers that provide support for demand-paged virtual memory address translation and variable-sized block translation. The 603R has a selectable 32- or 64-bit data bus and a 32-bit address bus. The interface protocol allows multiple masters to compete for system resources through a central external arbiter. The device supports single-beat and burst data transfers for memory accesses, and supports memory-mapped I/Os.

Rev. 5410B–HIREL–09/05

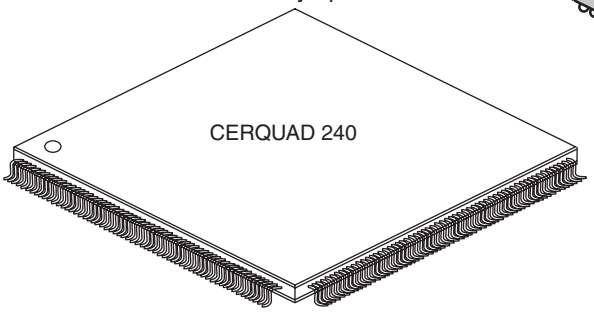
The 603R uses an advanced, 2.5/3.3V CMOS process technology and maintains full interface compatibility with TTL devices. It also integrates in-system testability and debugging features through JTAG boundary-scan capabilities.

## 2. Screening/Quality/Packaging

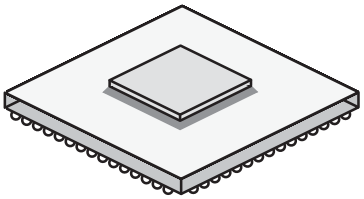
This product is manufactured in full compliance with:

- HiTCE CBGA according to Atmel Standards
- CI-CGA 255 and Cerquad: MIL-PRF-38535 class Q or according to Atmel standards
- CBGA 255: Upscreenings based upon Atmel standards
- CBGA, CI-CGA, HiTCE packages:
  - Full military temperature range ($T_C$ = -55°C, $T_j$ = +125°C)
  - Industrial temperature range ($T_C$ = -40°C, $T_j$ = +110°C)
- Cerquad:
  - Full military temperature range ($T_C$ = -55°C, $T_c$ = +125°C)
  - Industrial temperature range ($T_C$ = -40°C, $T_c$ = +110°C)
  - Commercial temperature ranges ($T_C$ = 0°C, $T_C$ = +70°C)
- Internal I/O Power Supply = 2.5 ±5% // 3.3V ±5%

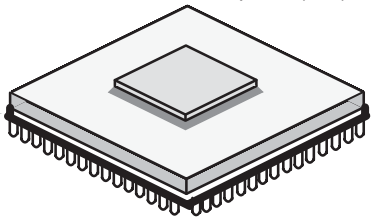
A suffix
**CERQUAD 240**
Ceramic Leaded Chip Carrier
Cavity up



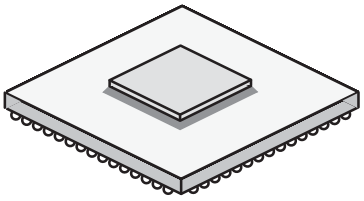

G suffix
**CBGA 255**
Ceramic Ball Grid Array



GS suffix
**CI-CGA 255**
Ceramic Ball Grid Array
with Solder Column Interposer (SCI)

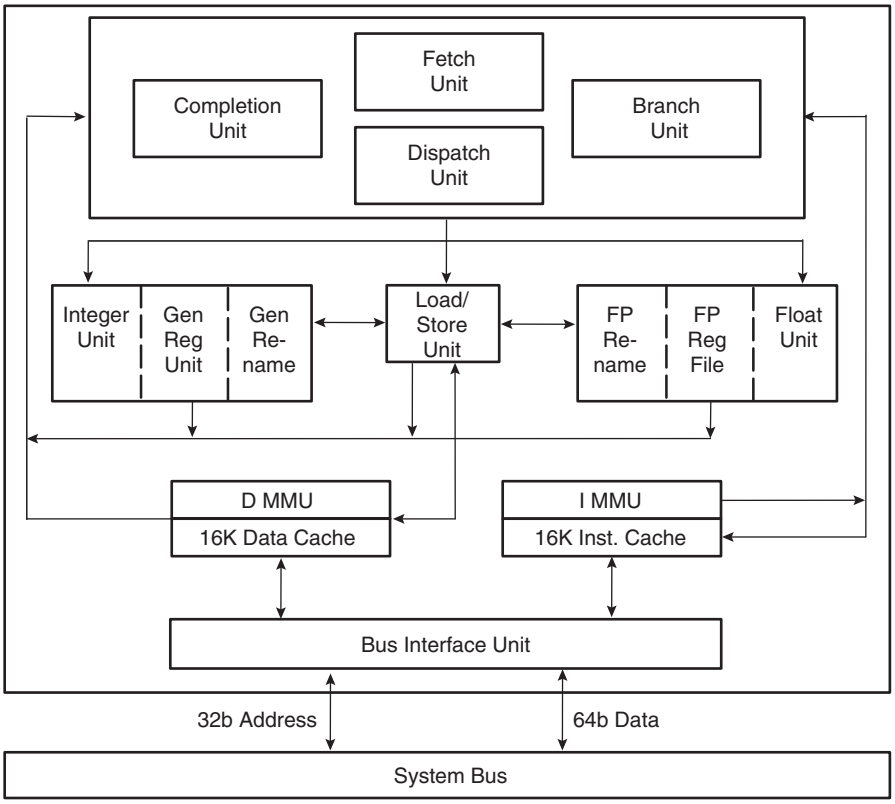


GH suffix
**HiTCE 255**
Ceramic Ball Grid Array



## 3. Block Diagram

**Figure 3-1.** Block Diagram




## 4. Overview

The 603R is a low-power implementation of the PowerPC microprocessor family of Reduced Instruction Set Computing (RISC) microprocessors. The 603R implements the 32-bit portion of the PowerPC architecture, which provides 32-bit effective addresses, integer data types of 8, 16 and 32 bits, and floating-point data types of 32 and 64 bits. For 64-bit PowerPC microprocessors, the PowerPC architecture provides 64-bit integer data types, 64-bit addressing, and other features required to complete the 64-bit architecture.

The 603R provides four software controllable power-saving modes. Three of the modes (nap, doze, and sleep) are static in nature, and progressively reduce the amount of power dissipated by the processor. The fourth is a dynamic power management mode that causes the functional units in the 603R to automatically enter a low-power mode when the functional units are idle without affecting operational performance, software execution, or any external hardware.

The 603R is a superscalar processor capable of issuing and retiring as many as three instructions per clock. Instructions can be executed in any order for increased performance, but, the 603R makes completion appear sequential.

The 603e integrates five execution units:

- an Integer Unit (IU)
- a Floating-point Unit (FPU)
- a Branch Processing Unit (BPU)

- a Load/Store Unit (LSU)
- a System Register Unit (SRU)

The ability to execute five instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput for 603R-based systems. Most integer instructions execute in one clock cycle. The FPU is pipelined so a single-precision multiply-add instruction can be issued every clock cycle.

The 603R provides independent on-chip, 16 Kbyte, four-way set-associative, physically addressed caches for instructions and data, as well as on-chip instruction and data Memory Management Units (MMUs). The MMUs contain 64-entry, two-way set-associative, Data and Instruction Translation Lookaside Buffers (DTLB and ITLB) that provide support for demand-paged virtual memory address translation and variable-sized block translation. The TLBs and caches use a Least Recently Used (LRU) replacement algorithm. The 603R also supports block address translation through the use of two independent Instruction and Data Block Address Translation (IBAT and DBAT) arrays of four entries each. Effective addresses are compared simultaneously with all four entries in the BAT array during block translation. In accordance with the PowerPC architecture, if an effective address hits in both the TLB and BAT array, the BAT translation has priority.

The 603R has a selectable 32- or 64-bit data bus and a 32-bit address bus. The 603R interface protocol allows multiple masters to compete for system resources through a central external arbiter. The 603R provides a three-state coherency protocol that supports the exclusive, modified, and invalid cache states. This protocol is a compatible subset of the MESI (Modified/Exclusive/Shared/Invalid) four-state protocol and operates coherently in systems that contain four-state caches. The 603R supports single-beat and burst data transfers for memory accesses, and supports memory-mapped I/Os.

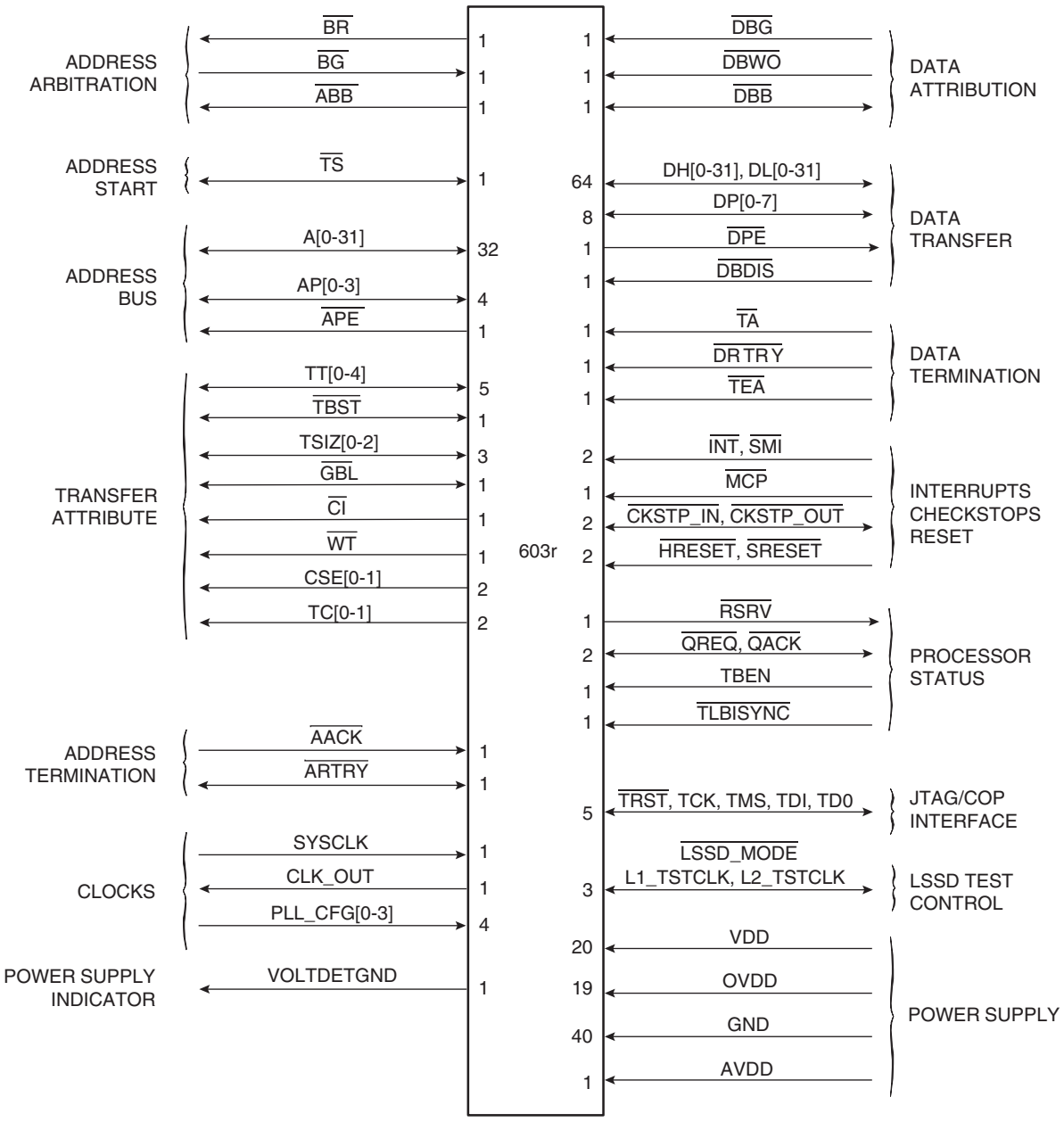
The 603R uses an advanced, 0.29 µm 5-metal-layer CMOS process technology and maintains full interface compatibility with TTL devices.

## 5. Signal Description

Figure 5-1 on page 5, Table 10-5 and Table 10-6 on page 20 describe the signals on the TSPC603R and indicate signal functions. The test signals, $\overline{\text{TRST}}$, TMS, TCK, TDI and TDO, comply with the subset P-1149.1 of the IEEE testability bus standard.

The three signals $\overline{\text{LSSD\_MODE}}$, LI_TSTCLK and L2_TSTCLK are test signals for factory use only and must be pulled up to $V_{DD}$ for normal machine operations.

**Figure 5-1.** Functional Signal Groups




## 6. Detailed Specifications

This specification describes the specific requirements for the microprocessor TSPC603R, in compliance with MIL-STD-883 class B or Atmel standard screening.

## 7. Applicable Documents

1. MIL-STD-883: Test methods and procedures for electronics
2. MIL-PRF-38535: General specifications for microcircuits

The microcircuits are in accordance with the applicable documents and as specified herein.

## 7.1 Design and Construction

### 7.1.1 Terminal Connections

Depending on the package, the terminal connections are as shown in Table 10-2 on page 15, Table 10-4 on page 18, "Recommended Operating Conditions" on page 6, Figure 15-2 on page 49, Figure 15-4 on page 52 and Figure 5-1 on page 5.

### 7.1.2 *Lead Material and Finish*

Lead material and finish shall be as specified in MIL-STD-1835. (See "Package Mechanical Data" on page 47.)

## 7.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only and functional operation at the maximum is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

### 7.2.1 Absolute Maximum Ratings for the 603R(1)(2)(3)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Core supply voltage | $V_{DD}$ | -0.3 | 2.75 | V |
| PLL supply voltage | $AV_{DD}$ | -0.3 | 2.75 | V |
| I/O supply voltage | $OV_{DD}$ | -0.3 | 3.6 | V |
| Input voltage | $V_{IN}$ | -0.3 | 5.5 | V |
| Storage temperature range | $T_{STG}$ | -55 | +150 | °C |

Notes:
1. **Caution**: The input voltage must not be greater than $OV_{DD}$ by more than 2.5V at any time, including during power-on reset.
2. **Caution**: The $OV_{DD}$ voltage must not be greater than $V_{DD}/AV_{DD}$ by more than 1.2V at any time, including during power-on reset.
3. **Caution**: The $V_{DD}/AV_{DD}$ voltage must not be greater than $OV_{DD}$ by more than 0.4V at any time, including during power-on reset.

Functional operating conditions are given in AC and DC electrical specifications. Stresses beyond the absolute maximums listed may affect device reliability or cause permanent damage to the device.

### 7.2.2 Recommended Operating Conditions

The following are the recommended and tested operating conditions. Proper device operation outside of these ranges is not guaranteed.

### 7.2.3 Recommended Operating Conditions

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Core supply voltage | $V_{DD}$ | 2.375 | 2.625 | V |
| PLL supply voltage | $AV_{DD}$ | 2.375 | 2.625 | V |
| I/O supply voltage | $OV_{DD}$ | 3.135 | 3.465 | V |
| Input voltage | $V_{IN}$ | GND | 5.5 | V |
| Operating temperature | $T_c$ | -55 | +125 | °C |
| Junction operating temperature specific to Cerquad | $T_j$ | – | +135 | °C |

# 8. Thermal Characteristics

## 8.1 CBGA 255 and CI-CGA 255 Packages

The data found in this section concerns 603R devices packaged in the 255-lead 21 mm multi-layer ceramic (MLC) and ceramic BGA package. Data is included for use with a Thermalloy #2328B heat sink.

The internal thermal resistance for this package is negligible due to the exposed die design. A thermal interface material is recommended at the package lid to heat sink interface to minimize the thermal contact resistance.

Additionally, the CBGA package offers an excellent thermal connection to the card and power planes. Heat generated at the chip is dissipated through the package, the heat sink (when used) and the card. The parallel heat flow paths result in the lowest overall thermal resistance as well as offer significantly better power dissipation capability if a heat sink is not used.

The thermal characteristics for the flip-chip CBGA and CI-CGA packages are as follows:

Thermal resistance (junction-to-case) = $R_{jc}$ or
$\theta_{jc}$ = 0.095°C/Watt for the 2 packages.

Thermal resistance (junction-to-ball) = $R_{jb}$ or
$\theta_{jb}$ = 3.5°C/Watt for the CBGA package.

Thermal resistance (junction-to-bottom SCI) = $R_{js}$ or
$\theta_{js}$ = 3.7°C/Watt for the CI-CGA package.

The junction temperature can be calculated from the junction to ambient thermal resistance, as follow:

Junction temperature:

$$T_j = T_a + (R_{jc} + R_{cs} + R_{sa}) \times P$$

where: $T_a$ is the ambient temperature in the vicinity of the device

$R_{jc}$ is the die junction to case thermal resistance of the device

$R_{cs}$ is the case to heat sink thermal resistance of the interface material

$R_{sa}$ is the heat sink to ambient thermal resistance

P is the power dissipated by the device

During operation, the die-junction temperatures ($T_j$) should be maintained at a lower value than the value specified in ”Recommended Operating Conditions” on page 6.

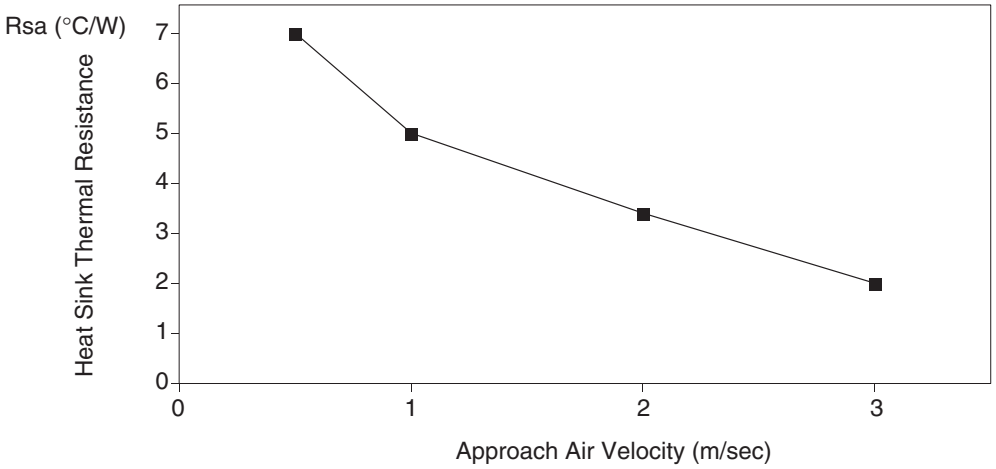
The thermal resistance of the thermal interface material ($R_{cs}$) is typically about 1°C/Watt.

Assuming a $T_a$ of 85°C and a consumption (P) of 3.6 Watts, the junction temperature of the device would be as follow:

$T_j$ = 85°C + (0.095°C/Watt + 1°C/Watt + $R_{sa}$) × 3.5 Watts.

For the Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance ($R_{sa}$) versus airflow velocity is shown in Figure 8-1.

**Figure 8-1.** CBGA Thermal Management Example




Assuming an air velocity of 1 m/sec, the associated overall thermal resistance and junction temperature, found in Table 8-1 will result.

**Table 8-1.** Thermal Resistance and Junction Temperature

| Configuration | $R_{ja}$ (°C/W) | $T_j$ (°C) |
|---|---|---|
| With 2328B heat sink | 5 | 106 |

Vendors such as Aavid, Thermalloy®, and Wakefield Engineering can supply heat sinks with a wide range of thermal performance.

## 8.2 HiTCE CBGA Package

**Table 8-2.** HiTCE CBGA Package

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Junction-to-bottom of balls(1) | $R\theta_J$ | 7.5 | °C/W |
| Junction-to-ambient thermal resistance natural convection, four-layer (2s2p) board | $R\theta_{JMA}$ | 22.4(2) | °C/W |
| Junction to board thermal resistance | $R\theta_{JB}$ | 11.7(3) | °C/W |

Notes: 1. Simulation, no convection air flow.
2. Per JEDEC JESD51-2 with the board horizontal.
3. Per JEDEC JESD51-8 with the board horizontal.

## 8.3 CERQUAD 240 Package

This section provides thermal management data for the 603R. This information is based on a typical desktop configuration using a 240 lead, 32 mm x 32 mm, wire-bond CERQUAD package with the cavity up (the silicon die is attached to the bottom of the package). This configuration enables dissipation through the PCB.

The thermal characteristics for a wire-bond CERQUAD package are as follows:

- Thermal resistance (junction to bottom of the case) (typical) = $R_{\theta jc}$ or $\theta_{jc}$ = 2.5°C/Watt
- Thermal resistance (junction to top of the case) is typically 16°C/W

### 8.3.1 Thermal Management Example

The junction temperature can be calculated from the junction to ambient thermal resistance, as follows:

Junction temperature:

$$T_j = T_C + R_{\theta jc} \times P$$

$$T_j = T_a + (R_{cs} + R_{sa}) \times P + R_{\theta jc} \times P$$

so

$$T_j = T_a + (R_{\theta jc} + R_{cs} + R_{sa}) \times P$$

Where:

$T_a$ is the ambient temperature in the vicinity of the device

$R_{\theta ja}$ is the junction to ambient resistance

$R_{\theta jc}$ is the junction to case thermal resistance of the device

$R_{cs}$ is the case to heat sink thermal resistance of the interface material

$R_{sa}$ is the heat sink to ambient thermal resistance

P is the power dissipated by the device

Because dissipation is made through the PCB, $R_{cs}$ and $R_{sa}$ are user values, and can vary considerably depending on the customer's application.

In a typical customer application, if $R_{cs}$ is 0.5°C/W, $R_{sa}$ is 3°C/W and Ta is 110°C, $T_j$ can be estimated.

$$T_j = 110°C + (2.5 + 0.5 + 3) \times 2.5 = 125°C$$

Note that verification of external thermal resistance and case temperature should be performed for each application. Thermal resistance depends on many factors including the amount of air turbulence and can therefore vary considerably.

## 9. Power Consideration

The PowerPC 603R is a microprocessor specifically designed for low-power operation. Like the 603e microprocessor version, the 603R provides both automatic and program-controllable power reduction modes for progressive reduction of power consumption. This section describes the hardware support provided by the 603R for power management.

### 9.1 Dynamic Power Management

Dynamic power management automatically powers up and down the individual execution units of the 603R, based upon the contents of the instruction stream. For example, if no floating-point instructions are being executed, the floating-point unit is automatically powered down. Power is not actually removed from the execution unit; instead, each execution unit has an independent clock input, which is automatically controlled on a clock-by-clock basis. Since CMOS circuits consume negligible power when they are not switching, stopping the clock to an execution unit effectively eliminates its power consumption. The operation of DPM is completely transparent to software or any external hardware. Dynamic power management is enabled by setting bit 11 in HID0 on power-up, following $\overline{\text{HRESET}}$.

## 9.2 Programmable Power Modes

The 603R provides four programmable power states, full power, doze, nap and sleep. The software selects these modes by setting one (and only one) of the three power saving mode bits. The hardware can enable a power management state through external asynchronous interrupts. The hardware interrupt causes the transfer of program flow to interrupt the handler code. The appropriate mode is then set by the software. The 603R provides a separate interrupt and interrupt vector for power management, the System Management Interrupt (SMI). The 603R also contains a decrement timer which allows it to enter the nap or doze mode for a predetermined amount of time and then return to full power operation through the Decrementer Interrupt (DI). Note that the 603R cannot switch from power-on management mode to another without first returning to full on mode. The nap and sleep modes disable bus snooping; therefore, a hardware handshake is provided to ensure coherency before the 603R enters these power management modes.

Table 9-1 summarizes the four power states.

**Table 9-1.** Power PC 603R Microprocessor Programmable Power Modes

| PM Mode | Functioning Units | Activation Method | Full-power Wake-up Method |
|---|---|---|---|
| Full Power | All units active | – | – |
| Full Power (with DPM) | Requested logic by demand | By instruction dispatch | – |
| Doze | - Bus snooping<br>- Data cache as needed<br>- Decrementer timer | Controlled by SW | External asynchronous exceptions(1)<br>Decrementer interrupt<br>Reset |
| Nap | Decrementer timer | Controlled by hardware and software | External asynchronous exceptions<br>Decrementer interrupt<br>Reset |
| Sleep | None | Controlled by hardware and software | External asynchronous exceptions<br>Reset |

Note: 1. Exceptions are referred to as interrupts in the architecture specification.

## 9.3 Power Management Modes

The following describes the characteristics of the 603R's power management modes, the requirements for entering and exiting the various modes, and the system capabilities provided by the 603R while the power management modes are active.

### Full Power Mode with DPM Disabled

Full power mode with DPM disabled; power mode is selected when the DPM enable bit (bit 11) in HID0 is cleared

- Default state following power-up and $\overline{\text{HRESET}}$
- All functional units are operating at full processor speed at all times

### Full Power Mode with DPM Enabled

Full power mode with DPM enabled (HID0[11] = 1); provides on-chip power management without affecting the functionality or performance of the 603R

- Required functional units are operating at full processor speed

- Functional units are clocked only when needed
- No software or hardware intervention required after mode is set
- Software/hardware and performance are transparent

**Doze Mode**

The doze mode disables most functional units but maintains cache coherency by enabling the bus interface unit and snooping. A snoop hit will cause the 603R to enable the data cache, copy the data back to the memory, disable the cache, and fully return to the doze state. In this mode:

- Most functional units are disabled
- Bus snooping and time base/decrementer are still enabled
- Dose mode sequence:
  - Set doze bit (HID0[8] = 1)
  - 603R enters doze mode after several processor clocks
- There are several methods for returning to full-power mode
  - Assert $\overline{\text{INT}}$, $\overline{\text{SMI}}$, $\overline{\text{MCP}}$ or decrementer interrupts
  - Assert hard reset or soft reset
- The Transition to full-power state takes no more than a few processor cycles
- Phase Locked Loop (PLL) running and locked to SYSCLK

**Nap Mode**

The nap mode disables the 603R but still maintains the phase locked loop (PLL) and the time base/decrementer. The time base can be used to restore the 603R to full-on state after a programmed amount of time. Because bus snooping is disabled for nap and sleep modes, a hardware handshake using the quiesce request ($\overline{\text{QREQ}}$) and quiesce acknowledge ($\overline{\text{QACK}}$) signals is required to maintain data coherency. The 603R will assert the $\overline{\text{QREQ}}$ signal to indicate that it is ready to disable bus snooping. When the system has ensured that snooping is no longer necessary, it will assert $\overline{\text{QACK}}$ and the 603R will enter the sleep or nap mode. In this mode:

- The time base/decrementer is still enabled
- Most functional units are disabled (including bus snooping)
- All non-essential input receivers are disabled
- Nap mode sequence:
  - Set nap bit (HID0[9] = 1)
  - 603R asserts quiesce request ($\overline{\text{QREQ}}$) signal
  - System asserts quiesce acknowledge ($\overline{\text{QACK}}$) signal
  - 603R enters sleep mode after several processor clocks
- There are several methods for returning to full-power mode:
  - Assert $\overline{\text{INT}}$, $\overline{\text{SPI}}$, $\overline{\text{MCP}}$ or decrementer interrupts
  - Assert hard reset or soft reset
- Transition to full-power takes no more than a few processor cycles
- The PLL is running and locked to SYSCLK

### Sleep Mode

Sleep mode consumes the least amount of power of the four modes since all functional units are disabled. To conserve the maximum amount of power, the PLL may be disabled and the SYSCLK may be removed. Due to the fully static design of the 603R, the internal processor state is preserved when no internal clock is present. Because the time base and decrementer are disabled while the 603R is in sleep mode, the 603R's time base contents will have to be updated from an external time base following sleep mode if accurate time-of-day maintenance is required. Before the 603R enters the sleep mode, the 603R will assert the $\overline{\text{QREQ}}$ signal to indicate that it is ready to disable bus snooping. When the system has ensured that snooping is no longer necessary, it will assert $\overline{\text{QACK}}$ and the 603R will enter the sleep mode.

In this mode:

- All functional units are disabled (including bus snooping and time base)
- All non-essential input receivers are disabled
  - Internal clock regenerators are disabled
  - The PLL is still running (see below)
- Sleep mode sequence
  - Set sleep bit (HID0[10] = 1)
  - 603R asserts quiesce request ($\overline{\text{QREQ}}$)
  - System asserts quiesce acknowledge ($\overline{\text{QACK}}$)
  - 603R enters sleep mode after several processor clocks
- There are several methods for returning to full-power mode
  - Assert $\overline{\text{INT}}$, $\overline{\text{SMI}}$, or $\overline{\text{MCP}}$ interrupts
  - Assert hard reset or soft reset
- The PLL may be disabled and SYSCLK may be removed while in sleep mode
- Return to full-power mode after PLL and SYSCLK disabled in sleep mode
  - Enable SYSCLK
  - Reconfigure PLL into the desired processor clock mode
  - System logic waits for PLL startup and relock time (100 µs)
  - System logic asserts one of the sleep recovery signals (for example, INT or SMI)

## 9.4 Power Management Software Considerations

Since the 603R is a dual issue processor with out-of-order execution capabilities, care must be taken with the way the power management mode is entered. Furthermore, nap and sleep modes require all outstanding bus operations to be completed before the power management mode is entered. Normally, during the system configuration time, one of the power management modes would be selected by setting the appropriate HID0 mode bit. Later on, the power management mode is invoked by setting the MSR[POW] bit. To provide a clean transition into and out of the power management mode, the **stmsr**[POW] should be preceded by a **sync** instruction and followed by an **isync** instruction.

## 9.5 Power Dissipation

**Table 9-2.** Power Dissipation[1][2][3][4] with $V_{DD}/AV_{DD}$ = 2.5 ±5%V, $OV_{DD}$ = 3.3 ±5%V, GND = 0V, 0°C ≤ $T_C$ ≤ 125°C

| | Cerquad 240 Package | | CBGA 255, HiTCE CBGA 255 and CI-CGA 255 | | | | | |
|---|---|---|---|---|---|---|---|---|
| **CPU Clock Frequency** | **166 MHz** | **200 MHz** | **166 MHz** | **200 MHz** | **233 MHz** | **266 MHz** | **300 MHz** | **Units** |
| **Full-on Mode (DPM Enabled)** | | | | | | | | |
| Typical | 2.1 | 2.5 | 2.1 | 2.5 | 3 | 3.5 | 4 | W |
| Max | 3.2 | 4 | 3.2 | 4 | 4.6 | 5.3 | 6 | W |
| **Doze Mode** | | | | | | | | |
| Typical | 1.5 | 1.7 | 1.5 | 1.7 | 1.8 | 2 | 2.1 | W |
| **Nap Mode** | | | | | | | | |
| Typical | 100 | 120 | 100 | 120 | 140 | 160 | 180 | mW |
| **Sleep Mode** | | | | | | | | |
| Typical | 96 | 110 | 96 | 110 | 123 | 135 | 150 | mW |
| **Sleep Mode-PLL Disabled** | | | | | | | | |
| Typical | 60 | 60 | 60 | 60 | 60 | 60 | 60 | mW |
| **Sleep Mode-PLL and SYSCLK Disabled** | | | | | | | | |
| Typical | 25 | 25 | 25 | 25 | 25 | 25 | 25 | mW |
| Maximum | 60 | 60 | 60 | 60 | 60 | 80 | 100 | mW |

Notes:
1. These values apply for all valid PLL_CFG[0-3] settings and do not include output driver power ($OV_{DD}$) or analog supply power ($AV_{DD}$). $OV_{DD}$ power is system dependent but is typically ≤ 10% of $V_{DD}$. Worst case $AV_{DD}$ = 15 mW.
2. Typical power is an average value measured at $V_{DD} = AV_{DD}$ = 2.5V, $OV_{DD}$ = 3.3V, in a system executing typical applications and benchmark sequences.
3. Maximum power is measured at $V_{DD}$ = 2.625V using a worst-case instruction mix.
4. To calculate the power consumption at low temperature (-55°C), **use a factor of 1.25.**

## 9.6 Marking

Each microcircuit is legible and permanently marked with at least the following information:

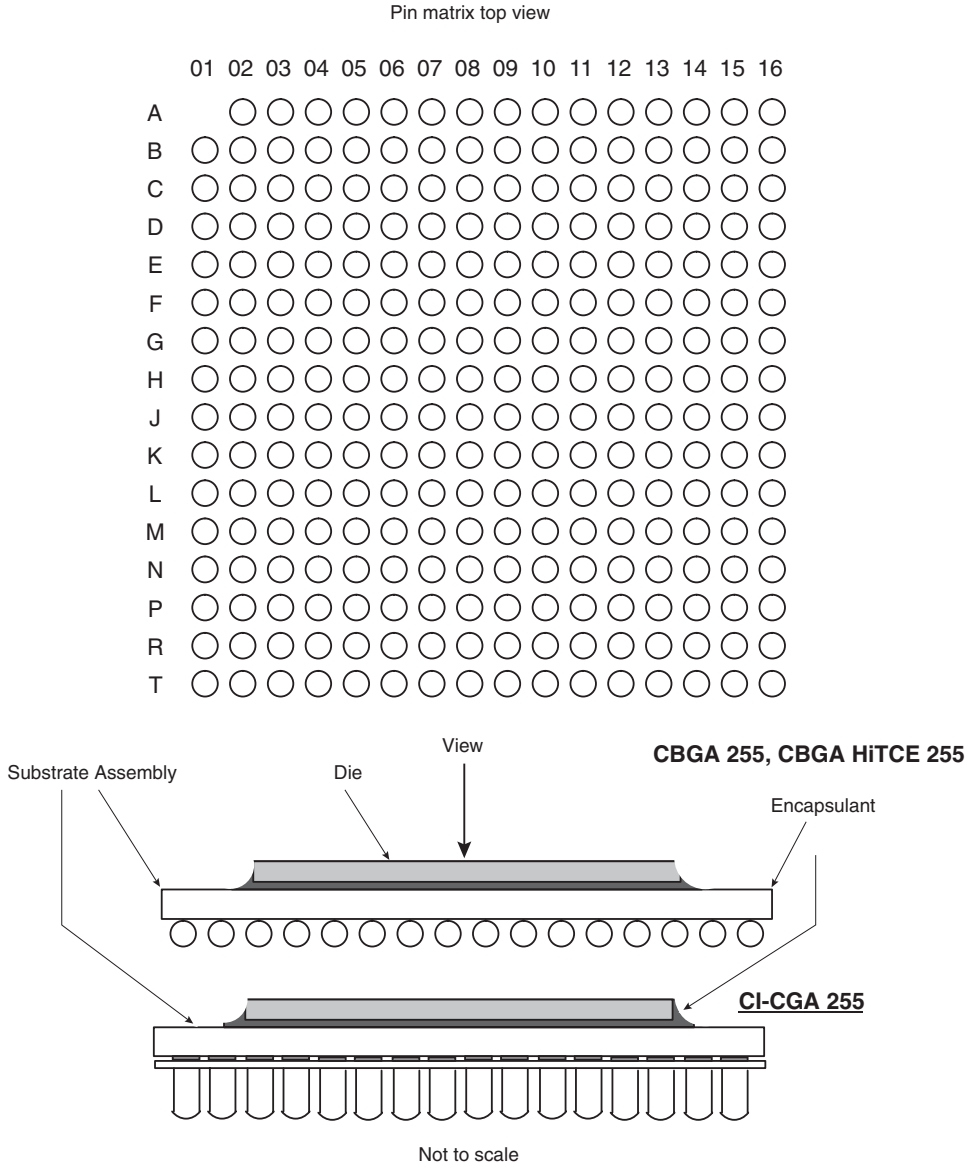
- Atmel logo
- Manufacturer's part number
- Class B identification if applicable
- Date code of inspection lot
- ESD identifier if available
- Country of manufacture

# 10. Pin Assignments

## 10.1 CBGA 255 and CI-CGA 255 Packages

Figure 10-1 (pin matrix) shows the pinout as viewed from the top of the CBGA and CI-CGA packages. The direction of the top surface view is shown by the side profile of the packages.

**Figure 10-1.** CBGA 255, HiTCE CBGA 255 and CI–CGA 255 Top View



### 10.1.1 Pinout Listing

**Table 10-1.** Power and Ground Pins

| | CBGA, HiTCE CBGA and CI-CGA Pin Number | |
|---|---|---|
| | **$V_{DD}$** | **GND** |
| PLL ($AV_{DD}$) | A10 | |
| Internal Logic[1] ($V_{DD}$) | F06, F08, F09, F11, G07, G10, H06, H08, H09, H11, J06, J08, J09, J11, K07, K10, L06, L08, L09, L11 | C05, C12, E03, E06, E08, E09, E11, E14, F05, F07, F10, F12, G06, G08, G09, G11, H05, H07, H10, H12, J05, J07, J10, J12, K06, K08, K09, K11, L05, L07, L10, L12, M03, M06, M08, M09, M11, M14, P05, P12 |
| I/O Drivers[1] ($OV_{DD}$) | C07, E05, E07, E10, E12, G03, G05, G12, G14, K03, K05, K12, K14, M05, M07, M10, M12, P07, P10 | |

Notes: 1. $OV_{DD}$ inputs apply power to the I/O drivers and $V_{DD}$ inputs supply power to the processor core.

**Table 10-2.** Signal Pinout Listing

| Signal Name | CBGA, HiTCE CBGA and CI-CGA Pin Number | Active | I/O |
|---|---|---|---|
| A[0-31] | C16, E04, D13, F02, D14, G01, D15, E02, D16, D04, E13, G02, E15, H01, E16, H02, F13, J01, F14, J02, F15, H03, F16, F04, G13, K01, G15, K02, H16, M01, J15, P01 | High | I/O |
| $\overline{\text{AACK}}$ | L02 | Low | Input |
| $\overline{\text{ABB}}$ | K04 | Low | I/O |
| AP[0-3] | C01, B04, B03, B02 | High | I/O |
| $\overline{\text{APE}}$ | A04 | Low | Output |
| $\overline{\text{ARTRY}}$ | J04 | Low | I/O |
| $\overline{\text{BG}}$ | L01 | Low | Input |
| $\overline{\text{BR}}$ | B06 | Low | Output |
| $\overline{\text{CI}}$ | E01 | Low | Output |
| $\overline{\text{CKSTP\_IN}}$ | D08 | Low | Input |
| $\overline{\text{CKSTP\_OUT}}$ | A06 | Low | Output |
| CLK_OUT | D07 | - | Output |
| CSE[0-1] | B01, B05 | High | Output |
| $\overline{\text{DBB}}$ | J14 | Low | I/O |
| $\overline{\text{DBG}}$ | N01 | Low | Input |
| $\overline{\text{DBDIS}}$ | H15 | Low | Input |
| $\overline{\text{DBWO}}$ | G04 | Low | Input |
| DH[0-31] | P14, T16, R15, T15, R13, R12, P11, N11, R11, T12, T11, R10, P09, N09, T10, R09, T09, P08, N08, R08, T08, N07, R07, T07, P06, N06, R06, T06, R05, N05, T05, T04 | High | I/O |
| DL[0-31] | K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P03, N03, N04, R03, T01, T02, P04, T03, R04 | High | I/O |
| DP[0-7] | M02, L03, N02, L04, R01, P02, M04, R02 | High | I/O |
| $\overline{\text{DPE}}$ | A05 | Low | Output |
| $\overline{\text{DRTRY}}$ | G16 | Low | Input |

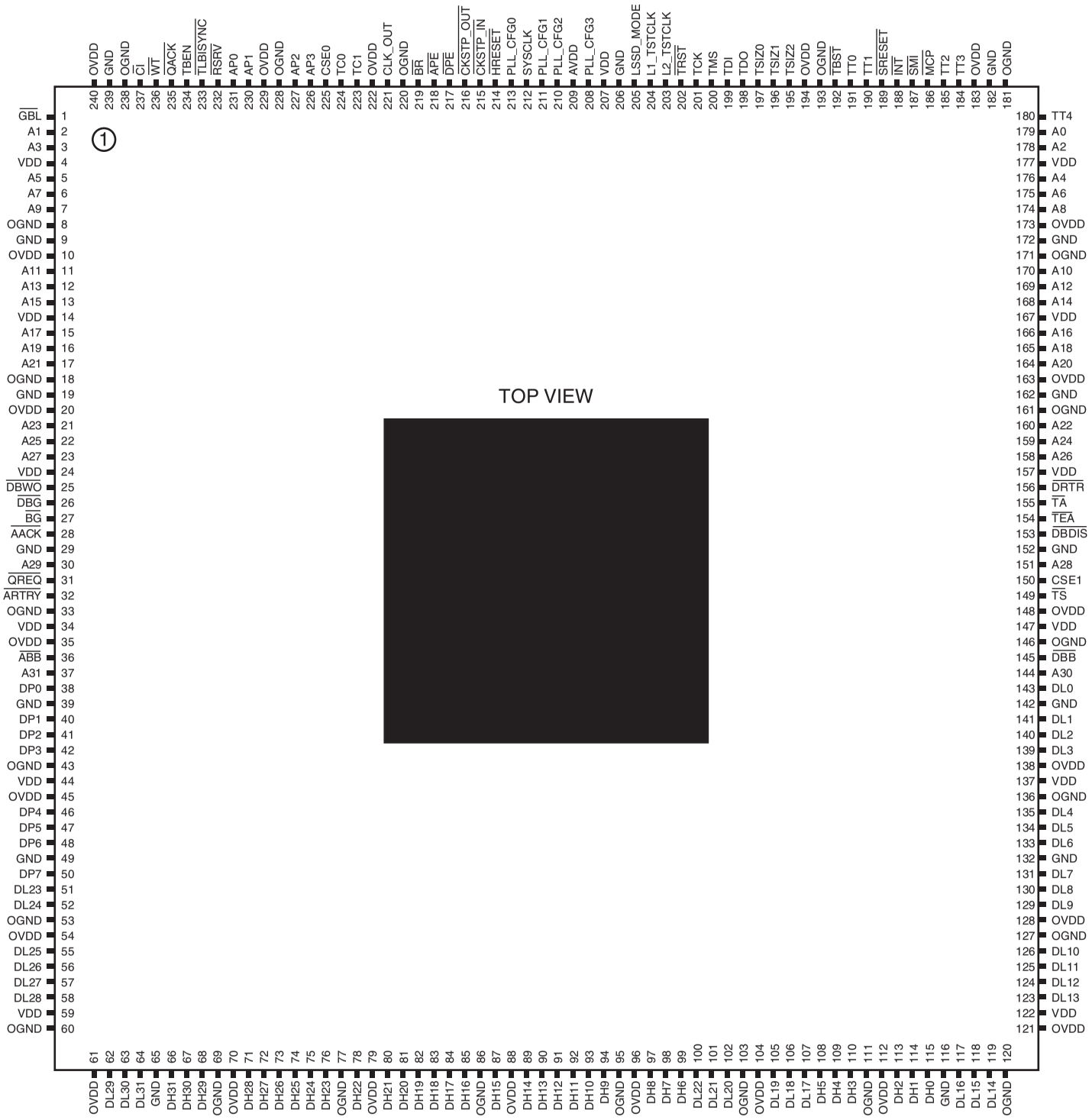
**Table 10-2.** Signal Pinout Listing (Continued)

| Signal Name | CBGA, HiTCE CBGA and CI-CGA Pin Number | Active | I/O |
|---|---|---|---|
| $\overline{\text{GBL}}$ | F01 | Low | I/O |
| $\overline{\text{HRESET}}$ | A07 | Low | Input |
| $\overline{\text{INT}}$ | B15 | Low | Input |
| L1_TSTCLK(1) | D11 | - | Input |
| L2_TSTCLK(1) | D12 | - | Input |
| $\overline{\text{LSSD\_MODE}}$(1) | B10 | Low | Input |
| $\overline{\text{MCP}}$ | C13 | Low | Input |
| PLL_CFG[0-3] | A08, B09, A09, D09 | High | Input |
| $\overline{\text{QACK}}$ | D03 | Low | Input |
| $\overline{\text{QREQ}}$ | J03 | Low | Output |
| $\overline{\text{RSRV}}$ | D01 | Low | Output |
| $\overline{\text{SMI}}$ | A16 | Low | Input |
| $\overline{\text{SRESET}}$ | B14 | Low | Input |
| SYSCLK | C09 | - | Input |
| $\overline{\text{TA}}$ | H14 | Low | Input |
| TBEN | C02 | High | Input |
| $\overline{\text{TBST}}$ | A14 | Low | I/O |
| TC[0-1] | A02, A03 | High | Output |
| TCK | C11 | - | Input |
| TDI | A11 | High | Input |
| TDO | A12 | High | Output |
| $\overline{\text{TEA}}$ | H13 | Low | Input |
| $\overline{\text{TLBISYNC}}$ | C04 | Low | Input |
| TMS | B11 | High | Input |
| $\overline{\text{TRST}}$ | C10 | Low | Input |
| $\overline{\text{TS}}$ | J13 | Low | I/O |
| TSIZ[0-2] | A13, D10, B12 | High | I/O |
| TT[0-4] | B13, A15, B16, C14, C15 | High | I/O |
| $\overline{\text{WT}}$ | D02 | Low | Output |
| NC | B07, B08, C03, C06, C08, D05, D06, F03, H04, J16 | Low | Input |
| VOLTDETGND(2) | F03 | Low | Output |

Notes: 1. These are test signals for factory use only and must be pulled up to $OV_{DD}$ for normal machine operation.
2. NC (not connected) in the 603e BGA package; internally tied to GND in the 603R BGA package to indicate to the power supply that a low-voltage processor is present.

## 10.2 CERQUAD 240 Package

**Figure 10-2.** CERQUAD 240: Top View



### 10.2.1 Pinout Listing

**Table 10-3.** Power and Ground Pins

| | CERQUAD Pin Number | |
|---|---|---|
| | **VCC** | **GND** |
| PLL ($AV_{DD}$) | 209 | |
| Internal Logic | 4, 14, 24, 34, 44, 59, 122, 137, 147, 157, 167, 177, 207 | 9, 19,29, 39, 49, 65, 116, 132, 142, 152, 162, 172, 182, 206, 239 |
| Output Drivers | 10, 20, 35, 45, 54, 61, 70, 79, 88, 96, 104, 112, 121, 128, 138, 148, 163, 173, 183, 194, 222, 229, 240 | 8, 18, 33, 43, 53, 60, 69, 77, 86, 95, 103, 111, 120, 127, 136, 146, 161, 171, 181, 193, 220, 228, 238 |

**Table 10-4.** Signal Pinout Listing

| Signal Name | CERQUAD Pin Number |
|---|---|
| A[0-31] | 179, 2, 178, 3, 176, 5, 175, 6, 174, 7, 170, 11, 169, 12, 168, 13, 166, 15, 165, 16, 164, 17, 160, 21, 159, 22, 158, 23, 151, 30, 144, 37 |
| $\overline{\text{AACK}}$ | 28 |
| $\overline{\text{ABB}}$ | 36 |
| AP[0-3] | 231,230,227,226 |
| $\overline{\text{APE}}$ | 218 |
| $\overline{\text{ARTRY}}$ | 32 |
| $\overline{\text{BG}}$ | 27 |
| $\overline{\text{BR}}$ | 219 |
| $\overline{\text{CI}}$ | 237 |
| $\overline{\text{CKSTP\_IN}}$ | 215 |
| $\overline{\text{CKSTP\_OUT}}$ | 216 |
| CLK_OUT | 221 |
| CSE[0-1] | 225,150 |
| $\overline{\text{DBB}}$ | 145 |
| $\overline{\text{DBG}}$ | 26 |
| $\overline{\text{DBDIS}}$ | 153 |
| $\overline{\text{DBWO}}$ | 25 |
| DH[0-31] | 115, 114, 113, 110, 109, 108, 99, 98, 97, 94, 93, 92, 91, 90, 89, 87, 85, 84, 83, 82, 81, 80, 78, 76, 75, 74, 73, 72, 71, 68, 67, 66 |
| DL[0-31] | 143, 141, 140, 139, 135, 134, 133, 131, 130, 129, 126, 125, 124, 123, 119, 118, 117, 107, 106, 105, 102, 101, 100, 51, 52, 55, 56, 57, 58, 62, 63, 64 |
| DP[0-7] | 38, 40, 41, 42, 46, 47, 48, 50 |
| $\overline{\text{DPE}}$ | 217 |
| $\overline{\text{DRTRY}}$ | 156 |
| $\overline{\text{GBL}}$ | 1 |
| $\overline{\text{HRESET}}$ | 214 |

**Table 10-4.** Signal Pinout Listing (Continued)

| Signal Name | CERQUAD Pin Number |
|---|---|
| $\overline{\text{INT}}$ | 188 |
| L1_TSTCLK[1] | 204 |
| L2_TSTCLK[1] | 203 |
| $\overline{\text{LSSD\_MODE}}$[1] | 205 |
| $\overline{\text{MCP}}$ | 186 |
| PLL_CFG[0-3] | 213, 211, 210, 208 |
| $\overline{\text{QACK}}$ | 235 |
| $\overline{\text{QREQ}}$ | 31 |
| $\overline{\text{RSRV}}$ | 232 |
| $\overline{\text{SMI}}$ | 187 |
| $\overline{\text{SRESET}}$ | 189 |
| SYSCLK | 212 |
| $\overline{\text{TA}}$ | 155 |
| TBEN | 234 |
| $\overline{\text{TBST}}$ | 192 |
| TC[0-1] | 224, 223 |
| TCK | 201 |
| TDI | 199 |
| TDO | 198 |
| $\overline{\text{TEA}}$ | 154 |
| $\overline{\text{TLBISYNC}}$ | 233 |
| TMS | 200 |
| $\overline{\text{TRST}}$ | 202 |
| $\overline{\text{TS}}$ | 149 |
| TSIZ[0-2] | 197, 196, 195 |
| TT[0-4] | 191, 190, 185, 184, 180 |
| $\overline{\text{WT}}$ | 236 |
| NC | |

Notes: 1. These are test signals for factory use only and must be pulled up to $V_{DD}$ for normal machine operation.
2. $OV_{DD}$ inputs supply power to the I/O drivers and $V_{DD}$ inputs supply power to the processor core. Future members of the 603 family may use different $OV_{DD}$ and $V_{DD}$ input levels.

**Table 10-5.** Address and Data Bus Signal Index for Cerquad, CBGA 255 and CI-CGA 255 Packages

| Signal Name | Abbreviation | Signal Function | Signal Type |
|---|---|---|---|
| Address Bus | A[0-31] | If output, physical address of data to be transferred<br>If input, represents the physical address of a snoop operation | I/O |
| Data Bus | DH[0-31] | Represents the state of data, during a data write operation if output, or during a data read operation if input | I/O |
| Data Bus | DL[0-31] | Represents the state of data, during a data write operation if output, or during a data read operation if input | I/O |

**Table 10-6.** Signal Index for Cerquad, CBGA 255, HiTCE CBGA 255 and CI-CGA 255 Packages

| Signal Name | Abbreviation | Signal Function | Signal Type |
|---|---|---|---|
| Address Acknowledge | $\overline{\text{AACK}}$ | The address phase of a transaction is complete | Input |
| Address Bus Busy | $\overline{\text{ABB}}$ | If output, the 603R is the address bus master<br>If input, the address bus is in use | I/O |
| Address Bus Parity | AP[0-3] | If output, represents odd parity for each of 4 bytes of the physical address for a transaction<br>If input, represents odd parity for each of 4 bytes of the physical address for snooping operations | I/O |
| Address Parity Error | $\overline{\text{APE}}$ | Incorrect address bus parity detected on a snoop | Output |
| Address Retry | $\overline{\text{ARTRY}}$ | If output, detects a condition in which a snooped address tenure must be retried<br>If input, must retry the preceding address tenure | I/O |
| Bus Grant | $\overline{\text{BG}}$ | May, with the proper qualification, assume mastership of the address bus | Input |
| Bus Request | $\overline{\text{BR}}$ | Request mastership of the address bus | Output |
| Cache Inhibit | $\overline{\text{CI}}$ | A single-beat transfer will not be cached | Output |
| Checkstop Input | $\overline{\text{CKSTP\_IN}}$ | Must terminate operation by internally gating off all clocks, and release all outputs | Input |
| Checkstop Output | $\overline{\text{CKSTP\_OUT}}$ | Has detected a checkstop condition and has ceased operation | Output |
| Cache Set Entry | CSE[0-1] | Cache replacement set element for the current transaction reloading into or writing out of the cache | Output |
| Data Bus Busy | $\overline{\text{DBB}}$ | If output, the 603R is the data bus master<br>If input, another device is bus master | I/O |
| Data Bus Disable | $\overline{\text{DBDIS}}$ | (For a write transaction) must release data bus and the data bus parity to high impedance during the following cycle | Input |
| Data Bus Grant | $\overline{\text{DBG}}$ | May, with the proper qualification, assume mastership of the data bus | Input |
| Data Bus Write Only | $\overline{\text{DBW0}}$ | May run the data bus tenure | Input |
| Data Bus Parity | DP[0-7] | If output, odd parity for each of 8 bytes of data write transactions<br>If input, odd parity for each byte of read data | I/O |
| Data Parity Error | $\overline{\text{DPE}}$ | Incorrect data bus parity | Output |
| Data Retry | $\overline{\text{DRTRY}}$ | Must invalidate the data from the previous read operation | Input |

**Table 10-6.** Signal Index for Cerquad, CBGA 255, HiTCE CBGA 255 and CI-CGA 255 Packages (Continued)

| Signal Name | Abbreviation | Signal Function | Signal Type |
|---|---|---|---|
| Global | $\overline{\text{GBL}}$ | If output, a transaction is global<br>If input, a transaction must be snooped by the 603R | I/O |
| Hard Reset | $\overline{\text{HRESET}}$ | Initiates a complete hard reset operation | Input |
| Interrupt | $\overline{\text{INT}}$ | Initiates an interrupt if bit EE of MSR register is set | Input |
| Factory Test | $\overline{\text{LSSD\_MODE}}$ | LSSD test control signal for factory use only | Input |
| | L1_TSTCLK | LSSD test control signal for factory use only | Input |
| | L2_TSTCLK | LSSD test control signal for factory use only | Input |
| Machine Check Interrupt | $\overline{\text{MCP}}$ | Initiates a machine check interrupt operation if the bit ME of MSR register and bit EMCP of HID0 register are set | Input |
| PLL Configuration | PLL_CFG[0-3] | Configures the operation of the PLL and the internal processor clock frequency | Input |
| Power supply indicator | VOLTDETGND | Available only on BGA package<br>Indicates to the power supply that a low-voltage processor is present. | Output |
| Quiescent Acknowledge | $\overline{\text{QACK}}$ | All bus activity has terminated and the 603R may enter a quiescent (or low power) state | Input |
| Quiescent Request | $\overline{\text{QREQ}}$ | Is requesting all bus activity normally to enter a quiescent (low power) state | Output |
| Reservation | $\overline{\text{RSRV}}$ | Represents the state of the reservation coherency bit in the reservation address register | Output |
| System Management Interrupt | $\overline{\text{SMI}}$ | Initiates a system management interrupt operation if the bit EE of MSR register is set | Input |
| Soft Reset | $\overline{\text{SRESET}}$ | Initiates processing for a reset exception | Input |
| System Clock | SYSCLK | Represents the primary clock input for the 603R, and the bus clock frequency for 603R bus operation | Input |
| Test Clock | CLK_OUT | Provides PLL clock output for PLL testing and monitoring | Output |
| Transfer Acknowledge | $\overline{\text{TA}}$ | A single-beat data transfer completed successfully or a data beat in a burst transfer completed successfully | Input |
| Timebase Enable | TBEN | The timebase should continue clocking | Input |
| Transfer Burst | $\overline{\text{TBST}}$ | If output, a burst transfer is in progress<br>If input, when snooping for single-beat reads | I/O |
| Transfer Code | TC[0-1] | Special encoding for the transfer in progress | Output |
| Test Clock | TCK | Clock signal for the IEEE P1149.1 test access port (TAP) | Input |
| Test Data Input | TDI | Serial data input for the TAP | Input |
| Test Data Output | TDO | Serial data output for the TAP | Output |
| Transfer Error Acknowledge | $\overline{\text{TEA}}$ | A bus error occurred | Input |
| TLBI Sync | $\overline{\text{TLBISYNC}}$ | Instruction execution should stop after execution of a **tlbsync** instruction | Input |
| Test Mode Select | TMS | Selects the principal operations of the test-support circuitry | Input |
| Test Reset | $\overline{\text{TRST}}$ | Provides an asynchronous reset of the TAP controller | Input |
| Transfer Size | TSIZ[0-2] | For memory accesses, these signals along with $\overline{\text{TBST}}$ indicate the data transfer size for the current bus operation | I/O |

**Table 10-6.** Signal Index for Cerquad, CBGA 255, HiTCE CBGA 255 and CI-CGA 255 Packages (Continued)

| Signal Name | Abbreviation | Signal Function | Signal Type |
|---|---|---|---|
| Transfer Start | $\overline{TS}$ | If output, begun a memory bus transaction and the address bus and transfer attribute signals are valid<br>If input, another master has begun a bus transaction and the address bus and transfer attribute signals are valid for snooping (see $\overline{GBL}$) | I/O |
| Transfer Type | TT[0-4] | Type of transfer in progress | I/O |
| Write-through | $\overline{WT}$ | A single-beat transaction is write-through | Output |

# 11. Electrical Characteristics

## 11.1 General Requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below:

- Table 11-1: Static electrical characteristics for the electrical variants
- Table 11-2: Dynamic electrical characteristics for the 603R

The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG0 to PLL_CFG3 signals. All timings are respectively specified to the rising edge of SYSCLK.

These specifications are for 166 MHz to 300 MHz processor core frequencies for CBGA 255, HiTCE CBGA 255 and CI-CGA 255 packages and 166 MHz to 200 MHz processor core frequencies for the Cerquad 240 package.

## 11.2 Static Characteristics

**Table 11-1.** Electrical Characteristics with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $-55°C \le T_C \le 125°C$

| Characteristics | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input High Voltage (all inputs except SYSCLK) | | $V_{IH}$ | 2 | 5.5 | V |
| Input Low Voltage (all inputs except SYSCLK) | | $V_{IL}$ | GND | 0.8 | V |
| SYSCLK Input High Voltage | | $CV_{IH}$ | 2.4 | 5.5 | V |
| SYSCLK Input Low Voltage | | $CV_{IL}$ | GND | 0.4 | V |
| Input Leakage Current | $V_{IN}$ = 3.465V(1)(3) | $I_{IN}$ | - | 30 | µA |
| | $V_{IN}$ = 5.5V(1)(3) | $I_{IN}$ | - | 300 | µA |
| Hi-Z (off-state) Leakage Current | $V_{IN}$ = 3.465V(1)(3) | $I_{TSI}$ | - | 30 | µA |
| | $V_{IN}$ = 5.5V(1)(3) | $I_{TSI}$ | - | 300 | µA |
| Output High Voltage | $I_{OH}$ = -7 mA | $V_{OH}$ | 2.4 | - | V |
| Output Low Voltage | $I_{OL}$ = +7 mA | $V_{OL}$ | - | 0.4 | V |
| Capacitance, $V_{IN}$ = 0V, f = 1 MHz(2) (excludes $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$) | | $C_{IN}$ | - | 10 | pF |
| Capacitance, $V_{IN}$ = 0V, f = 1 MHz(2) (for $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$) | | $C_{IN}$ | - | 15 | pF |

Notes: 1. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK, and JTAG signals).
2. Capacitance is periodically sampled rather than 100% tested.

3. Leakage currents are measured for nominal $OV_{DD}$ and $V_{DD}$ or both $OV_{DD}$ and $V_{DD}$. Same variation (for example, both $V_{DD}$ and $OV_{DD}$ vary by either +5% or -5%)

## 11.3 Dynamic Characteristics

### 11.3.1 Clock AC Specifications

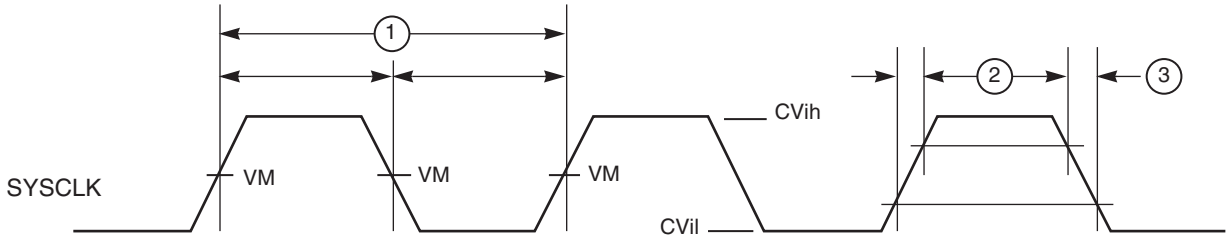
Table 11-2 provides the clock AC timing specifications as defined in Figure 11-1.

**Table 11-2.** Clock AC Timing Specifications[1][2][3][4] with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $-55°C \le T_C \le 125°C$

| Figure Number | Characteristics | CBGA 255, HiTCE CBGA 255, CI-CGA 255 and CERQUAD | | | | CBGA 255, HiTCE CBGA 255 and CI-CGA 255 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 166 MHz | | 200 MHz | | 233 MHz | | 266 MHz | | 300 MHz | | Unit | Note |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | |
| | Processor Frequency | 150 | 166 | 150 | 200 | 180 | 233 | 180 | 266 | 180 | 300 | MHz | [5] |
| | VCO Frequency | 300 | 332 | 300 | 400 | 360 | 466 | 360 | 532 | 360 | 600 | MHz | [5] |
| | SYSCLK (bus) Frequency | 25 | 66.7 | 33.3 | 66.7 | 33.3 | 75 | 33.3 | 75 | 33.3 | 75 | MHz | [5] |
| 1 | SYSCLK Cycle Time | 15 | 30 | 13.3 | 30 | 13.3 | 30 | 13.3 | 30 | 13.3 | 30 | ns | |
| 2,3 | SYSCLK Rise and Fall Time | – | 2 | – | 2 | – | 2 | – | 2 | – | 2 | ns | [1] |
| 4 | SYSCLK Duty Cycle (1.4V measured) | 40 | 60 | 40 | 60 | 40 | 60 | 40 | 60 | 40 | 60 | % | [3] |
| | SYSCLK Jitter | – | ±150 | – | ±150 | – | ±150 | – | ±150 | – | ±150 | ps | [2] |
| | 603R Internal PLL Relock Time | – | 100 | – | 100 | – | 100 | – | 100 | – | 100 | µs | [3][4] |

Notes:
1. Rise and fall times for the SYSCLK input are measured from 0.4V to 2.4V.
2. Cycle-to-cycle jitter is guaranteed by design.
3. Timing is guaranteed by design and characterization and is not tested.
4. The PLL relock time is the maximum amount of time required for PLL lock after a stable $V_{DD}$, $OV_{DD}$, $AV_{DD}$ and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 µs) during the power-on reset sequence.
5. **Caution**: The SYSCLK frequency and PLL_CFG[0-3] settings must be chosen so that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0-3] signal description for valid PLL_CFG[0-3] settings.

**Figure 11-1.** SYSCLK Input Timing Diagram




VM = Midpoint Voltage (1.4V)

### 11.3.2 Input AC Specifications

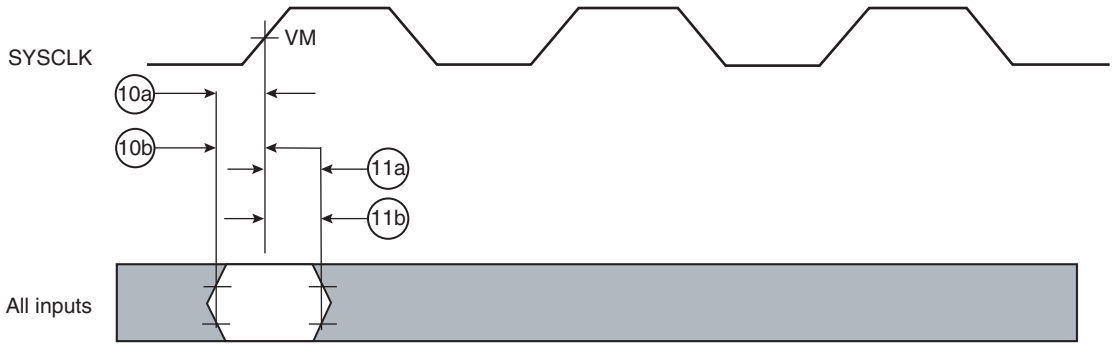
Table 11-3 provides the input AC timing specifications for the 603R as defined in Figure 11-2 and Figure 11-3.

**Table 11-3.** Input AC Timing Specifications[1] with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $-55°C \le T_C \le 125°C$

| Figure Number | Characteristics | CBGA 255, HiTCE CBGA 255, CI-CGA 255 and Cerquad 240 Packages | | CBGA 255, HiTCE CBGA 255 and CI-CGA 255 | | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | 166, 200 MHz | | 233, 266 MHz | | 300 MHz | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| 10a | Address/data/transfer attribute inputs valid to SYSCLK (input setup) | 2.5 | – | 2.5 | – | 2.5 | – | ns | (2) |
| 10b | All other inputs valid to SYSCLK (input setup) | 4 | – | 3.5 | – | 3.5 | – | ns | (3) |
| 10c | Mode select inputs valid to $\overline{HRESET}$ (input setup) (for $\overline{DRTRY}$, $\overline{QACK}$ and $\overline{TLBISYNC}$) | 8 | – | 8 | – | 8 | – | $t_{sysclk}$ | (4)(5)(6)(7) |
| 11a | SYSCLK to address/data/transfer attribute inputs invalid (input hold) | 1 | – | 1 | – | 1 | – | ns | (2) |
| 11b | SYSCLK to all other inputs invalid (input hold) | 1 | – | 1 | – | 1 | – | ns | (3) |
| 11c | $\overline{HRESET}$ to mode select inputs invalid (input hold) (for $\overline{DRTRY}$, $\overline{QACK}$, and $\overline{TLBISYNC}$) | 0 | – | 0 | – | 0 | – | ns | (4)(6)(7) |

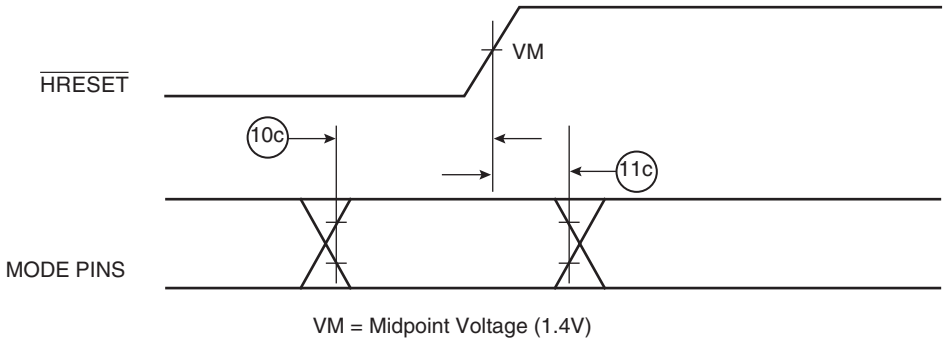
Notes:
1. All input specifications are measured from the TTL level (0.8 or 2V) of the signal in question to the 1.4V of the rising edge of the input SYSCLK. Both input and output timings are measured at the pin. See Figure 11-3.
2. Address/data/transfer attribute input signals are composed of the following: A[0-31], AP[0-3], TT[0-4], TC[0-1], $\overline{TBST}$, TSIZ[0-2], $\overline{GBL}$, DH[0-31], DL[0-31], DP[9-7].
3. All other input signals are composed of the following: $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, $\overline{ARTRY}$, $\overline{BG}$, $\overline{AACK}$, $\overline{DBG}$, $\overline{DBWO}$, $\overline{TA}$, $\overline{DRTRY}$, $\overline{TEA}$, $\overline{DBDIS}$, $\overline{HRESET}$, $\overline{SRESET}$, $\overline{INT}$, $\overline{SMI}$, $\overline{MCP}$, TBEN, $\overline{QACK}$, $\overline{TLBISYNC}$.
4. The setup and hold time is with respect to the rising edge of $\overline{HRESET}$. See Figure 11-3.
5. $t_{sysclk}$ is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
6. These values are guaranteed by design, and are not tested.
7. This specification is for configuration mode only. Also note that $\overline{HRESET}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 µs) during the power-on reset sequence.

**Figure 11-2.** Input Timing Diagram




VM = Midpoint Voltage (1.4V)

**Figure 11-3.** Mode Select Input Timing Diagram




### 11.3.3 Output AC Specifications

Table 11-4 provides the output AC timing specifications for the 603R (shown in Figure 11-4).

**Table 11-4.** Output AC Timing Specifications[1][2] with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $C_L = 50$ pF, $55°C \le T_C \le 125°C$

| Number | Characteristics | CBGA 255, HiTCE CBGA 255, CI-CGA 255 and Cerquad 240 Packages | | CBGA 255, HiTCE CBGA 255 and CI-CGA 255 | | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | 166, 200 MHz | | 233, 266 MHz | | 300 MHz | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| 12 | SYSCLK to output driven (output enable time) | 1 | – | 1 | – | 1 | – | ns | |
| 13a | SYSCLK to output valid (5.5V to 0.8V – $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$) | – | 9 | – | 9 | – | 9 | ns | (4) |
| 13b | SYSCLK to output valid ($\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$) | – | 8 | – | 8 | – | 8 | ns | (6) |
| 14a | SYSCLK to output valid (5.5V to 0.8V – all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$) | – | 11 | – | 11 | – | 11 | ns | (4) |
| 14b | SYSCLK to output valid (all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$) | – | 9 | – | 9 | – | 9 | ns | (6) |
| 15 | SYSCLK to output invalid (output hold) | 1 | – | 1 | – | 1 | – | ns | (3) |
| 16 | SYSCLK to output high impedance (all except $\overline{ARTRY}$, $\overline{ABB}$, $\overline{DBB}$) | – | 8.5 | – | 8 | – | 8 | ns | |
| 17 | SYSCLK to $\overline{ABB}$, $\overline{DBB}$, high impedance after precharge | – | 1 | – | 1 | – | 1 | $t_{SYSCLK}$ | (5)(7) |
| 18 | SYSCLK to $\overline{ARTRY}$ high impedance before precharge | – | 8 | – | 7.5 | – | 7.5 | ns | |
| 19 | SYSCLK to $\overline{ARTRY}$ precharge enable | 0.2 × $t_{SYSCLK}$ + 1 | – | 0.2 × $t_{SYSCLK}$ + 1 | – | 0.2 × $t_{SYSCLK}$ | – | ns | (3)(5) (8) |
| 20 | Maximum delay to $\overline{ARTRY}$ precharge | – | 1 | – | 1 | – | 1 | $t_{SYSCLK}$ | (5)(8) |
| 21 | SYSCLK to $\overline{ARTRY}$ high impedance after precharge | – | 2 | – | 2 | – | 2 | $t_{SYSCLK}$ | (6)(8) |