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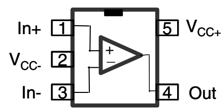
TSV611, TSV611A, TSV612, TSV612A

Rail-to-rail input/output 10 µA, 120 kHz CMOS operational amplifiers

Features

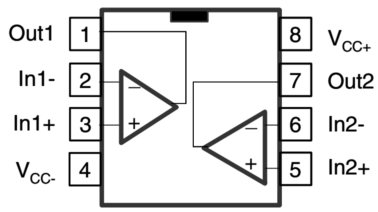
- Rail-to-rail input and output
- Low power consumption: 10 µA typ at 5 V
- Low supply voltage: 1.5 to 5.5 V
- Gain bandwidth product: 120 kHz typ
- Unity gain stable
- Low input offset voltage: 800 µV max (A version)
- Low input bias current: 1 pA typ
- Temperature range: -40 to +85° C

TSV611ILT - TSV611ICT



SOT23-5/SC70-5

TSV612IST - TSV612ID/DT



MiniSO-8/SO-8

Applications

- Battery-powered applications
- Smoke detectors
- Proximity sensors
- Portable devices
- Signal conditioning
- Active filtering
- Medical instrumentation

Description

The TSV61x family of single and dual operational amplifiers offers low voltage, low power operation and rail-to-rail input and output.

The devices also feature an ultra-low input bias current as well as a low input offset voltage.

The TSV61x have a gain bandwidth product of 120 kHz while consuming only 10 µA at 5 V.

These features make the TSV61x family ideal for sensor interfaces, battery supplied and portable applications, as well as active filtering.

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	6	V
V_{id}	Differential input voltage (2)	$\pm V_{CC}$	V
V_{in}	Input voltage (3)	V_{CC-} -0.2 to V_{CC+}+0.2	V
T_{stg}	Storage temperature	-65 to +150	°C
R_{thja}	Thermal resistance junction to ambient(4)(5)		°C/W
	SC70-5	205	
	SOT23-5	250	
	MiniSO-8	190	
	SO-8	125	
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model(6)	4	kV
	MM: machine model(7)	200	V
	CDM: charged device model(8)	1.5	kV
	Latch-up immunity	200	mA

1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. Vcc-Vin must not exceed 6 V.
4. Short-circuits can cause excessive heating and destructive dissipation.
5. Rth are typical values.
6. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
7. Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
8. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to ground.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.5 to 5.5	V
V_{icm}	Common mode input voltage range	V_{CC-} -0.1 to V_{CC+} +0.1	V
T_{oper}	Operating free air temperature range	-40 to +85	°C

2 Electrical characteristics

Table 3. Electrical characteristics at V_{CC+} = +1.8 V with V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, T_{amb} = 25° C, and R_L connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSV61x TSV61xA			4 0.8	mV
		$T_{min.} < T_{op} < T_{max.}$ TSV61x $T_{min.} < T_{op} < T_{max}$ TSV61xA			5 2	
DV_{io}	Input offset voltage drift			2		µV/°C
I_{io}	Input offset current ($V_{out} = V_{cc}/2$)			1	10(1)	pA
		$T_{min.} < T_{op} < T_{max.}$		1	100	pA
I_{ib}	Input bias current ($V_{out} = V_{cc}/2$)			1	10(1)	pA
		$T_{min.} < T_{op} < T_{max.}$		1	100	pA
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 1.8 V, V_{out} = 0.9 V	55	71		dB
		$T_{min.} < T_{op} < T_{max.}$	53			dB
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, Vout = 0.5 V to 1.3 V	78	83		dB
		$T_{min.} < T_{op} < T_{max.}$	74			dB
V_{OH}	High level output voltage	R_L = 10 kΩ $T_{min.} < T_{op} < T_{max.}$	35 50	4		mV
V_{OL}	Low level output voltage	R_L = 10 kΩ $T_{min.} < T_{op} < T_{max.}$		7	35 50	mV
I_{out}	Isink	V_o = 1.8 V $T_{min.} < T_{op} < T_{max.}$	9 9	13		mA
	Isource	V_o = 0 V $T_{min.} < T_{op} < T_{max.}$	8 8	10		
I_{CC}	Supply current (per operator)	No load, $V_{out} = V_{cc}/2$	6.5	9	12	µA
		$T_{min.} < T_{op} < T_{max.}$	6		12.5	µA
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 20 pF		100		kHz
ϕm	Phase margin	R_L = 10 kΩ, C_L = 20 pF		60		Degrees
G_m	Gain margin	R_L = 10 kΩ, C_L = 20 pF		9.5		dB
SR	Slew rate	R_L = 10 kΩ, C_L = 20 pF, V_{out} = 0.5V to 1.3V		0.03		V/µs

Table 3. Electrical characteristics at V_{CC+} = +1.8 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25° C, and R_L connected to V_{CC}/2 (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
e_n	Equivalent input noise voltage	f = 1 kHz		110		$\frac{nV}{\sqrt{Hz}}$
THD+N	Total harmonic distortion + noise	F_{in} = 1 kHz, Av = 1, V_{out} = 1 V_{pp}, R_L = 100 kΩ, BW = 22 kHz		0.07		%

1. Guaranteed by design.

Table 4. V_{CC+} = +3.3 V, V_{CC-} = 0 V, $V_{icm} = V_{CC}/2$, T_{amb} = 25° C, R_L connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSV61x TSV61xA			4 0.8	mV
		$T_{min}<T_{op}<T_{max}$ TSV61x $T_{min}<T_{op}<T_{max}$ TSV61xA			5 2	
DV_{io}	Input offset voltage drift			2		µV/°C
I_{io}	Input offset current			1	10(1)	pA
		$T_{min.} < T_{op} < T_{max.}$		1	100	pA
I_{ib}	Input bias current			1	10(1)	pA
		$T_{min.} < T_{op} < T_{max.}$		1	100	pA
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 3.3 V, V_{out} = 1.75 V	61	76		dB
		$T_{min.} < T_{op} < T_{max.}$	58			dB
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, Vout = 0.5 V to 2.8 V	85	92		dB
		$T_{min.} < T_{op} < T_{max.}$	83			dB
V_{OH}	High level output voltage	R_L = 10 kΩ $T_{min.} < T_{op} < T_{max.}$	35 50	5		mV
V_{OL}	Low level output voltage	R_L = 10 kΩ $T_{min.} < T_{op} < T_{max.}$		10	35 50	mV
I_{out}	Isink	$V_o = V_{CC}$ $T_{min.} < T_{op} < T_{max.}$	37 35	44		mA
	Isource	V_o = 0 V $T_{min.} < T_{op} < T_{max.}$	32 30	38		
I_{CC}	Supply current (per operator)	No load, $V_{out} = V_{CC}/2$	6.5	9.5	12.5	µA
		$T_{min.} < T_{op} < T_{max.}$	6		13	µA
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 20 pF		110		kHz
ϕm	Phase margin	R_L = 10 kΩ, C_L = 20 pF		60		Degrees
G_m	Gain margin	R_L = 10 kΩ, C_L = 20 pF,		9.5		dB
SR	Slew rate	R_L = 10 kΩ, C_L = 20 pF, V_{out} = 0.5V to 2.8V		0.035		V/µs
e_n	Equivalent input noise voltage	f = 1 kHz		110		$\frac{nV}{\sqrt{Hz}}$

1. Guaranteed by design.

Table 5. V_{CC+} = +5 V, V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, T_{amb} = 25° C, R_L connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSV61x TSV61xA			4 0.8	mV
		$T_{min}<T_{op}<T_{max}$ TSV61x $T_{min}<T_{op}<T_{max}$ TSV61xA			5 2	
DV_{io}	Input offset voltage drift			2		µV/°C
I_{io}	Input offset current			1	10(1)	pA
		$T_{min.} < T_{op} < T_{max.}$		1	100	pA
I_{ib}	Input bias current			1	10(1)	pA
		$T_{min.} < T_{op} < T_{max.}$		1	100	pA
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 5 V, V_{out} = 2.5 V	64	80		dB
		$T_{min.} < T_{op} < T_{max.}$	63			dB
SVR	Supply voltage rejection ratio 20 log ($\Delta V_{cc}/\Delta V_{io}$)	Vcc = 1.8 to 5 V	76	93		dB
		$T_{min.} < T_{op} < T_{max.}$	74			dB
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, Vout = 0.5 V to 4.5 V	88	93		dB
		$T_{min}<T_{op}<T_{max}$	85			dB
V_{OH}	High level output voltage	R_L = 10 kΩ $T_{min.} < T_{op} < T_{max.}$	35 50	7		mV
V_{OL}	Low level output voltage	R_L = 10 kΩ $T_{min.} < T_{op} < T_{max.}$		16	35 50	mV
I_{out}	Isink	$V_o = V_{CC}$ $T_{min.} < T_{op} < T_{max.}$	52 42	57		mA
	Isource	V_o = 0 V $T_{min.} < T_{op} < T_{max.}$	58 49	63		
I_{CC}	Supply current (per operator)	No load, $V_{out} = V_{CC}/2$	7.5	10.5	14	µA
		$T_{min.} < T_{op} < T_{max.}$	7		15	µA
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 20 pF		120		kHz
φm	Phase margin	R_L = 10 kΩ, C_L = 20 pF		62		Degrees
G_m	Gain margin	R_L = 10 kΩ, C_L = 20 pF		10		dB
SR	Slew rate	R_L = 10 kΩ, C_L = 20 pF, V_{out} = 0.5V to 4.5V		0.04		V/µs

Table 5. V_{CC+} = +5 V, V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, T_{amb} = 25° C, R_L connected to $V_{CC}/2$ (unless otherwise specified) (continued)

Symbol	Parameter		Min.	Typ.	Max.	Unit
e_n	Equivalent input noise voltage	f = 1 kHz		105		$\frac{nV}{\sqrt{Hz}}$
THD+N	Total harmonic distortion + noise	F_{in} = 1 kHz, Av = 1, V_{out} = 1 V_{pp}, R_L = 100 kΩ, BW = 22kHz		0.02		%

1. Guaranteed by design.

Figure 1. Supply current vs. supply voltage at V_{icm} = $V_{CC}/2$

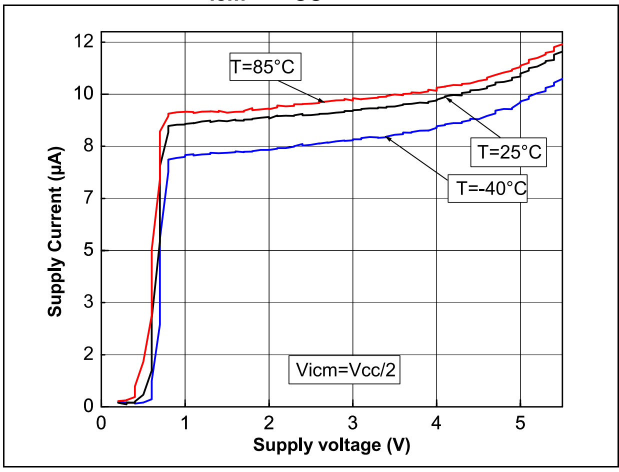


Figure 2. Output current vs. output voltage at V_{CC} = 1.5 V

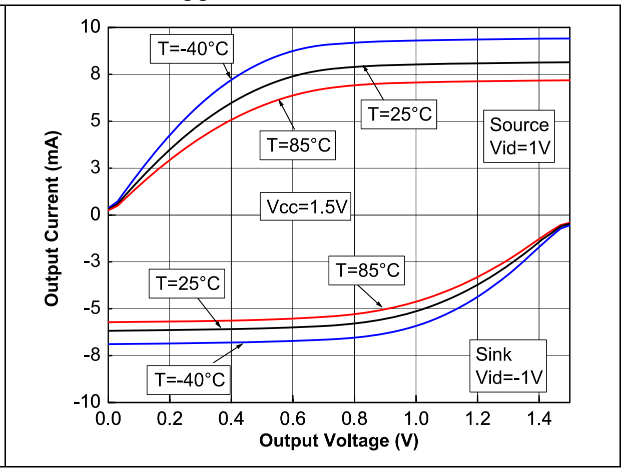


Figure 3. Output current vs. output voltage at V_{CC} = 5 V

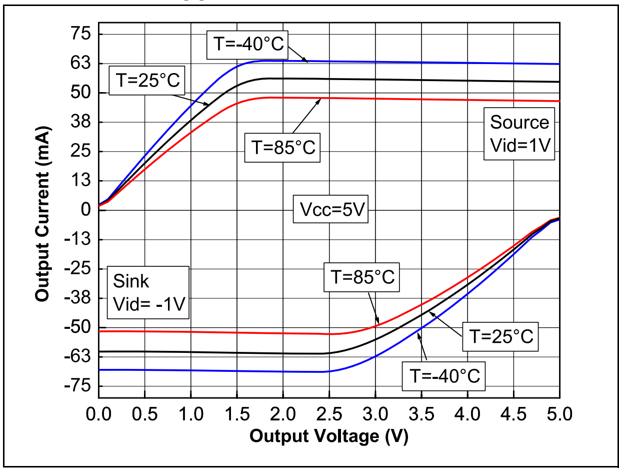


Figure 4. Voltage gain and phase vs. frequency at V_{CC} = 1.5 V

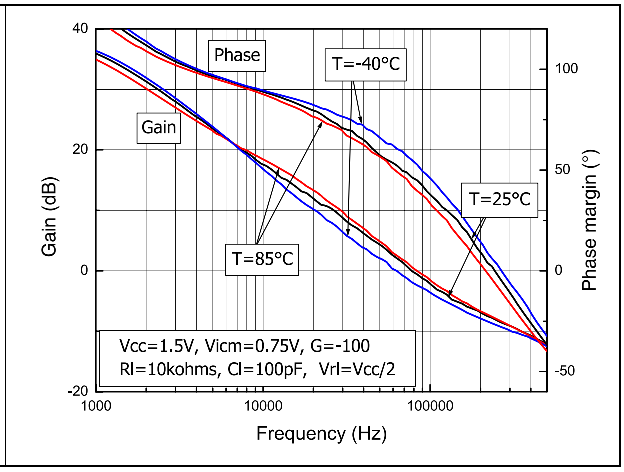


Figure 5. Voltage gain and phase vs. frequency at V_{CC} = 5 V

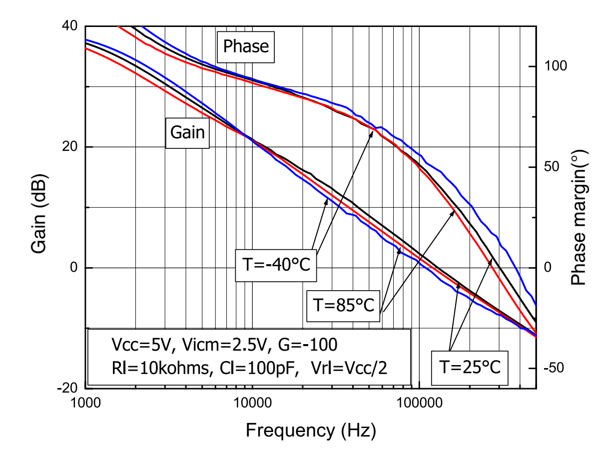


Figure 6. Phase margin vs. output current

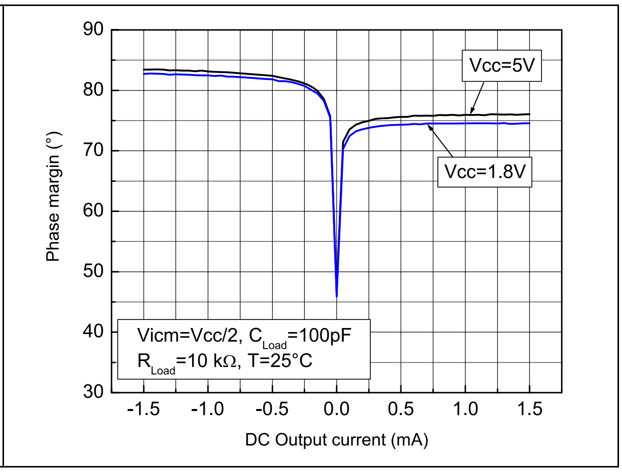


Figure 7. Positive slew rate vs. time, V_{CC} = 1.5 V, C_{Load} = 100 pF, R_{Load} = 10 kΩ

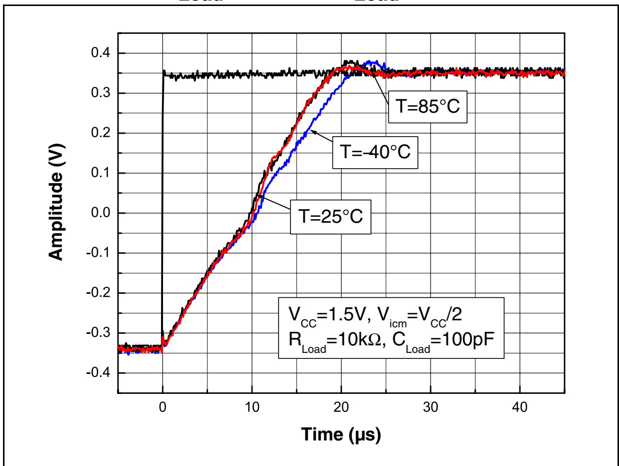


Figure 8. Negative slew rate vs. time, V_{CC} = 1.5 V, C_{Load} = 100 pF, R_{Load} = 10 kΩ

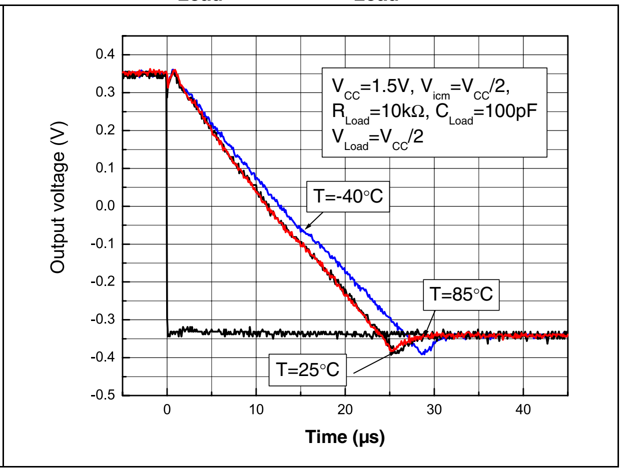


Figure 9. Positive slew rate vs. time, V_{CC} = 5.5 V, C_{Load} = 100 pF, R_{Load} = 100 kΩ

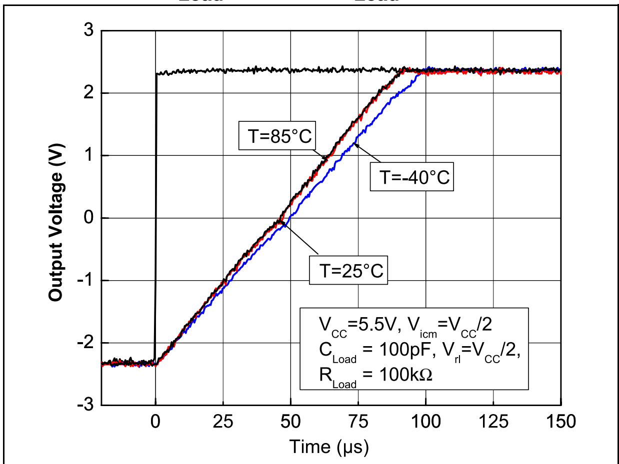


Figure 10. Negative slew rate vs. time, V_{CC} = 5.5 V, C_{Load} = 100 pF, R_{Load} = 100 kΩ

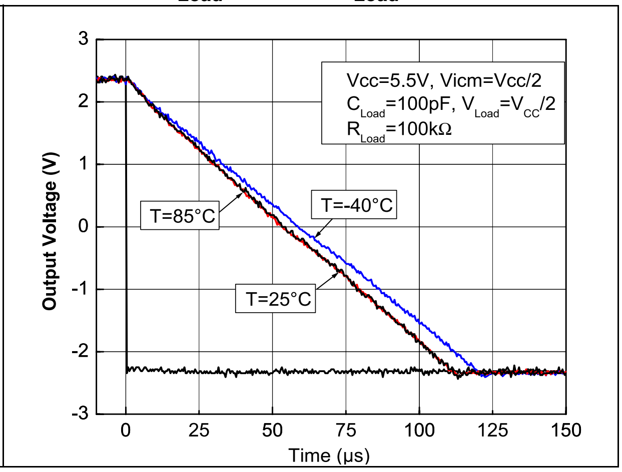


Figure 11. Slew rate vs. supply voltage

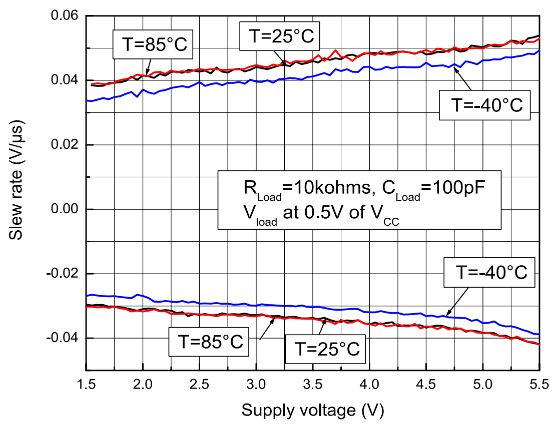


Figure 12. Noise vs. frequency at Vcc = 5 V

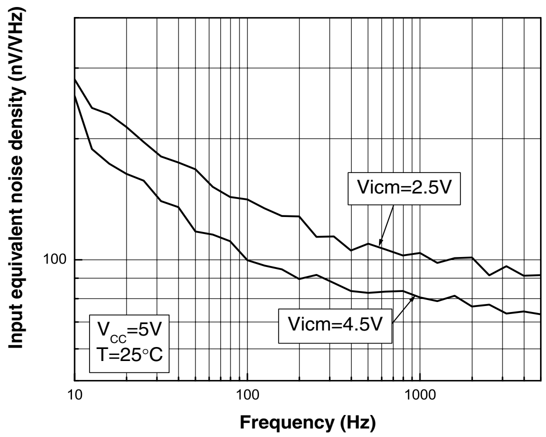


Figure 13. Distortion + noise vs. frequency

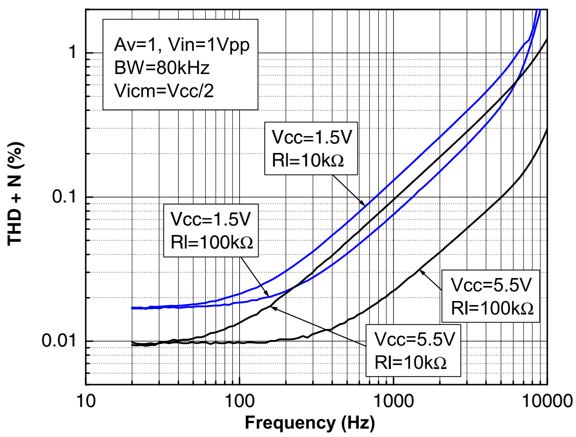


Figure 14. Distortion + noise vs. output voltage

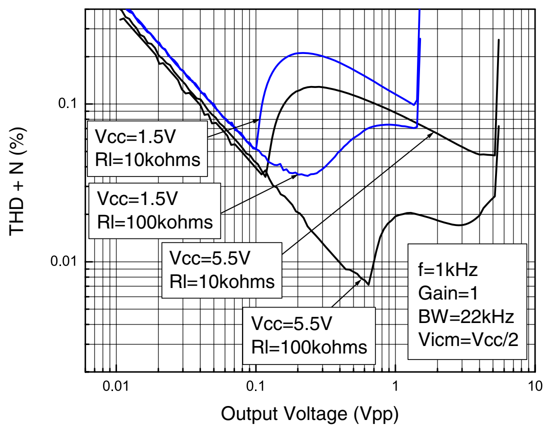


Figure 15. Voltage gain and phase vs. frequency at V_{CC} = 1.8 V (based on simulation results)

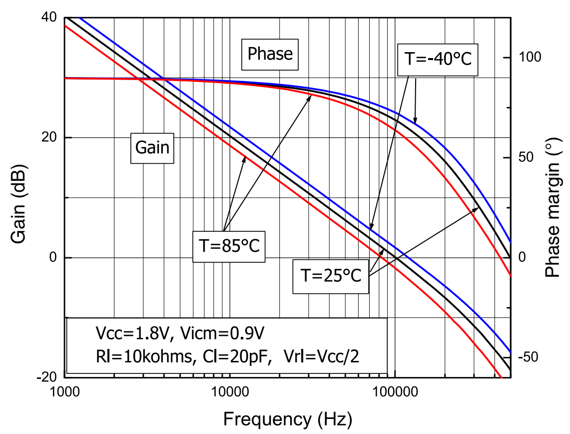
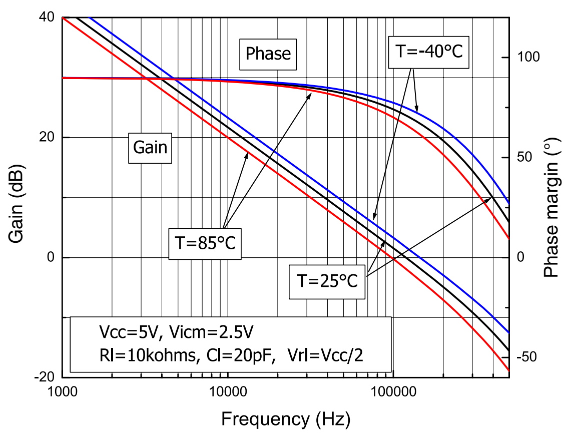


Figure 16. Voltage gain and phase vs. frequency at V_{CC} = 5 V (based on simulation results)



3 Application information

3.1 Operating voltages

The TSV61x can operate from 1.5 to 5.5 V. Their parameters are fully specified for 1.8, 3.3 and 5 V power supplies. However, the parameters are very stable in the full V_{CC} range and several characterization curves show the TSV61x characteristics at 1.5 V. Additionally, the main specifications are guaranteed in extended temperature ranges from -40° C to +85° C.

3.2 Rail-to-rail input

The TSV61x are built with two complementary PMOS and NMOS input differential pairs. The devices have a rail-to-rail input, and the input common mode range is extended from V_{CC-} -0.1 V to V_{CC+} +0.1 V. The transition between the two pairs appears at V_{CC+} -0.7 V. In the transition region, the performance of CMRR, PSRR, V_{io} and THD is slightly degraded (as shown in *Figure 17* and *Figure 18* for V_{io} vs. V_{icm}).

Figure 17. Input offset voltage vs input common mode at V_{CC} = 1.5 V

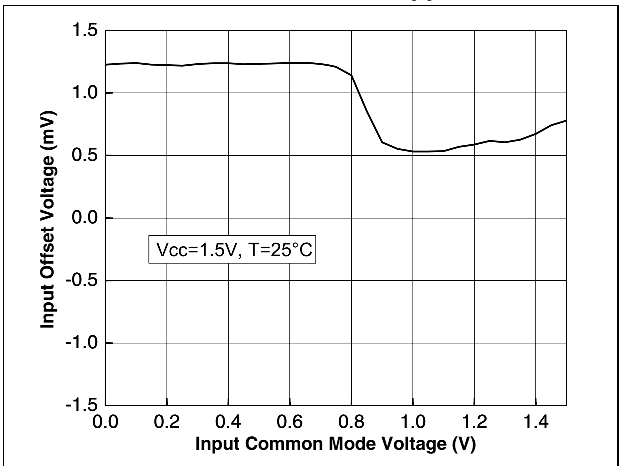
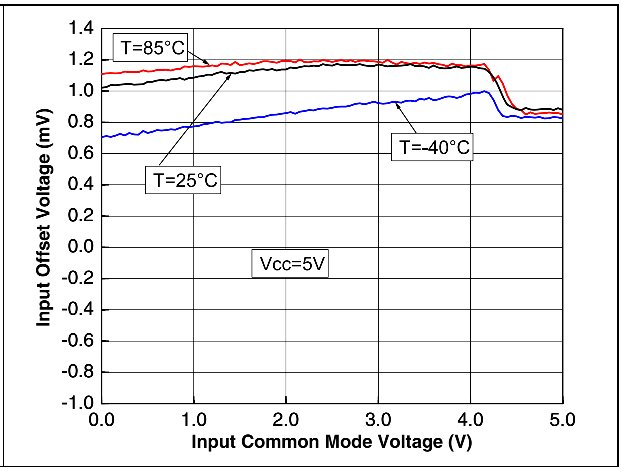


Figure 18. Input offset voltage vs input common mode at V_{CC} = 5 V



The device is guaranteed without phase reversal.

3.3 Rail-to-rail output

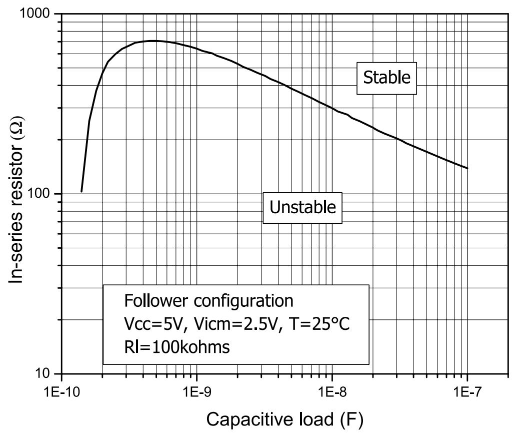
The operational amplifiers' output levels can go close to the rails: less than 35 mV above GND rail and less than 35 mV below V_{CC} rail when connected to 10 kΩ load to $V_{CC}/2$.

3.4 Driving resistive and capacitive loads

These products are micro-power, low-voltage operational amplifiers optimized to drive rather large resistive loads, above 10 kΩ For lower resistive loads, the THD level may significantly increase.

In a follower configuration, these operational amplifiers can drive capacitive loads up to 100 pF with no oscillations. When driving larger capacitive loads, adding an in-series resistor at the output can improve the stability of the devices (see *Figure 19* for recommended in-series resistor values). Once the in-series resistor value has been selected, the stability of the circuit should be tested on bench and simulated with the simulation model.

Figure 19. In-series resistor vs. capacitive load



3.5 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

3.6 Macromodel

An accurate macromodel of the TSV61x is available on STMicroelectronics' web site at www.st.com. This model is a trade-off between accuracy and complexity (that is, time simulation) of the TSV61x operational amplifiers. It emulates the nominal performances of a typical device within the specified operating conditions mentioned in the datasheet. It also helps to validate a design approach and to select the right operational amplifier, *but it does not replace on-board measurements*.

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.1 SOT23-5 package information

Figure 20. SOT23-5 package mechanical drawing

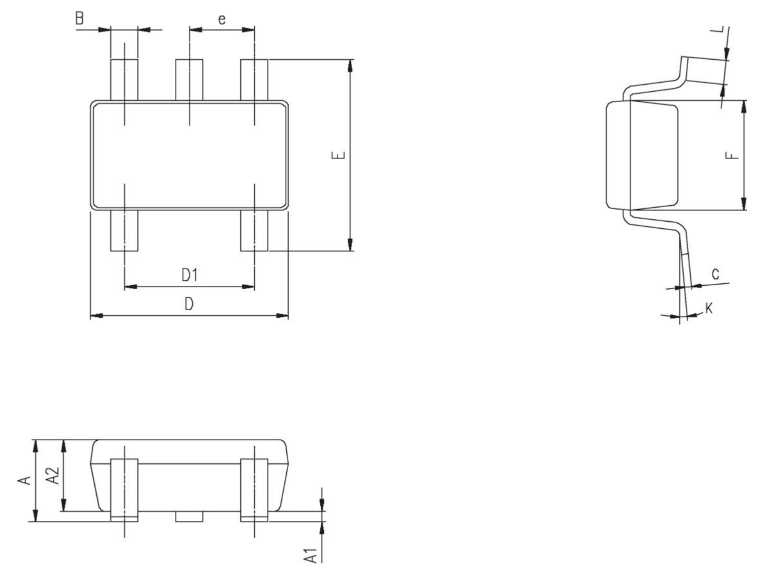


Table 6. SOT23-5 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.013	0.015	0.019
C	0.09	0.15	0.20	0.003	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.013	0.023
K	0 degrees		10 degrees			

4.2 SC70-5 (SOT323-5) package information

Figure 21. SC70-5 (SOT323-5) package mechanical drawing

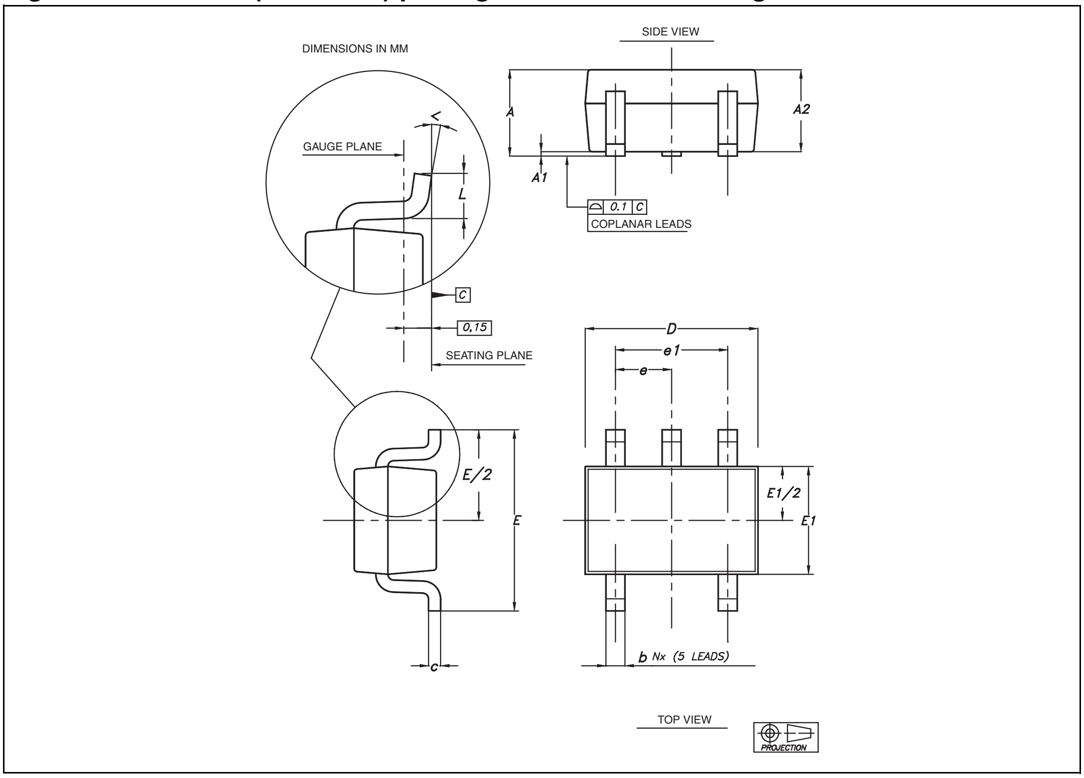


Table 7. SC70-5 (SOT323-5) package mechanical data

Ref	Dimensions					
	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	0.80		1.10	0.315		0.043
A1			0.10			0.004
A2	0.80	0.90	1.00	0.315	0.035	0.039
b	0.15		0.30	0.006		0.012
c	0.10		0.22	0.004		0.009
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E1	1.15	1.25	1.35	0.045	0.049	0.053
e		0.65			0.025	
e1		1.30			0.051	
L	0.26	0.36	0.46	0.010	0.014	0.018
<	0°		8°			

4.3 SO-8 package information

Figure 22. SO-8 package mechanical drawing

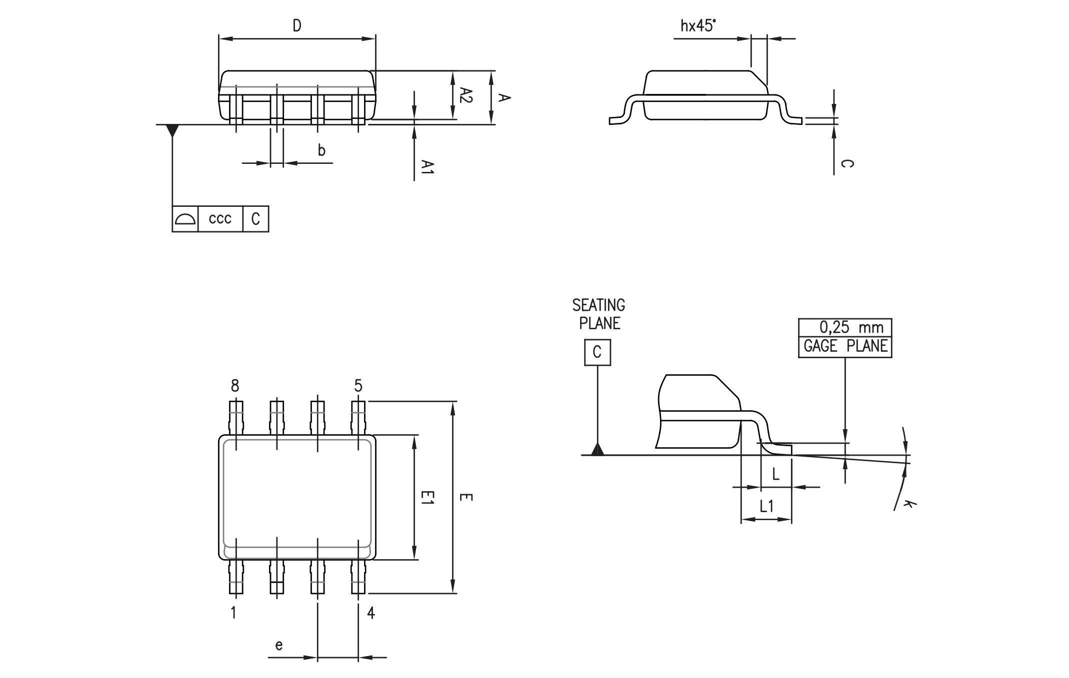


Table 8. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	1°		8°	1°		8°
ccc			0.10			0.004

4.4 MiniSO-8 package information

Figure 23. MiniSO-8 package mechanical drawing

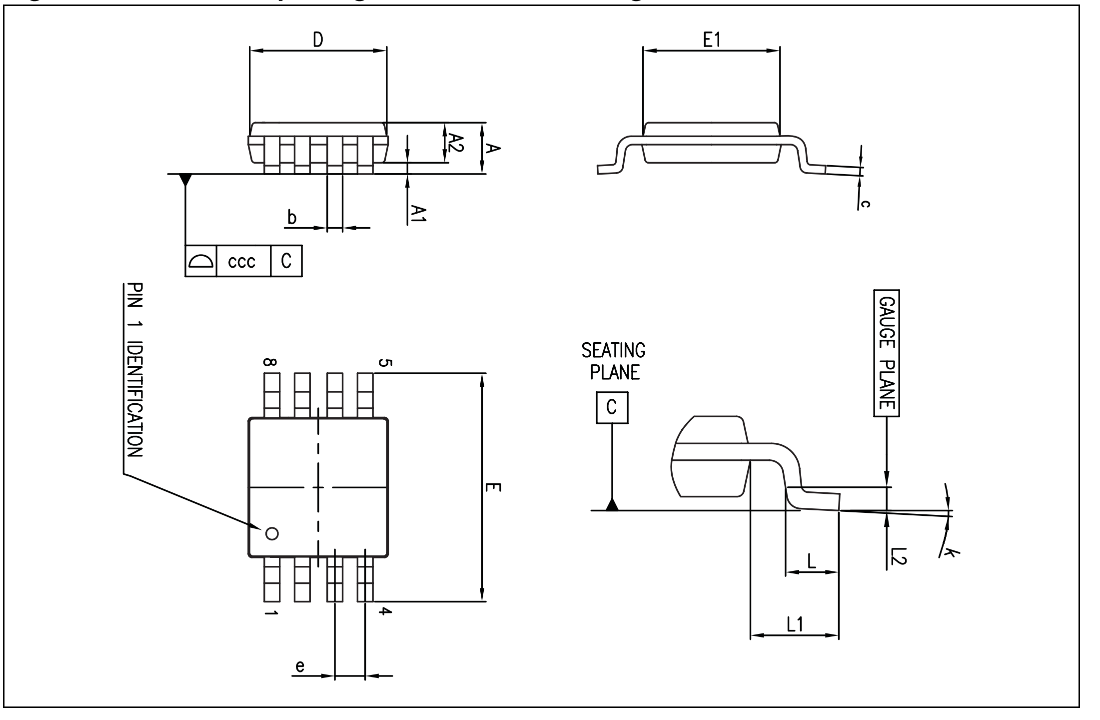


Table 9. MiniSO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

5 Ordering information

Table 10. Order codes

Order code	Temperature range	Package	Packing	Marking
TSV611ILT	-40° C to 85° C	SOT23-5	Tape & reel	K12
TSV611AILT				K11
TSV611ICT		SC70-5		K12
TSV611AICT				K11
TSV612ID/DT		SO-8	Tube & tape & reel	V612I
TSV612AID/DT				V612AI
TSV612IST		MiniSO-8	Tape & reel	K113
TSV612AIST				K115

6 Revision history

Table 11. Document revision history

Date	Revision	Changes
28-May-2009	1	Initial release.
18-Jan-2010	2	Full datasheet for product now in production. Added *Figure 1* to *Figure 19*.