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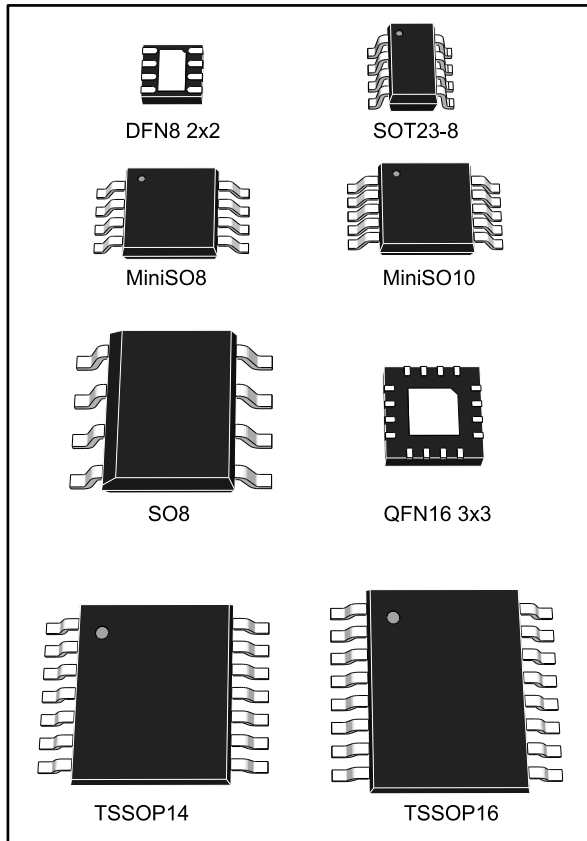
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## Dual and quad, rail-to-rail input/output, 60 $\mu$ A, 880 kHz operational amplifiers

Datasheet - production data



### Features

- Rail-to-rail input and output
- Low power consumption: 60  $\mu$ A typ at 5 V
- Low supply voltage: 1.5 V - 5.5 V
- Gain bandwidth product: 880 kHz typ
- Unity gain stable on 100 pF capacitor
- Low power shutdown mode: 5 nA typ
- Low offset voltage: 800  $\mu$ V max (A version)
- Low input bias current: 1 pA typ
- EMI hardened op amps
- Automotive qualification

### Related products

- See the TSV52x series for higher merit factor (1.15 MHz for 45  $\mu$ A)
- See the TSV61x (120 kHz for 9  $\mu$ A) or TSV62x (420 kHz for 29  $\mu$ A) for more power savings

### Applications

- Battery-powered applications
- Portable devices
- Signal conditioning
- Active filtering
- Medical instrumentation

### Description

The TSV63x and TSV63xA series of dual and quad operational amplifiers offers low voltage operation and rail-to-rail input and output.

This family features an excellent speed/power consumption ratio, offering an 880 kHz gain-bandwidth product while consuming only 60  $\mu$ A at 5 V supply voltage. The devices also feature an ultralow input bias current and TSV633 and TSV635 have a shutdown mode.

These features make the TSV63x and TSV63xA family ideal for sensor interfaces, battery-supplied and portable applications, and active filtering.

Table 1: Device summary

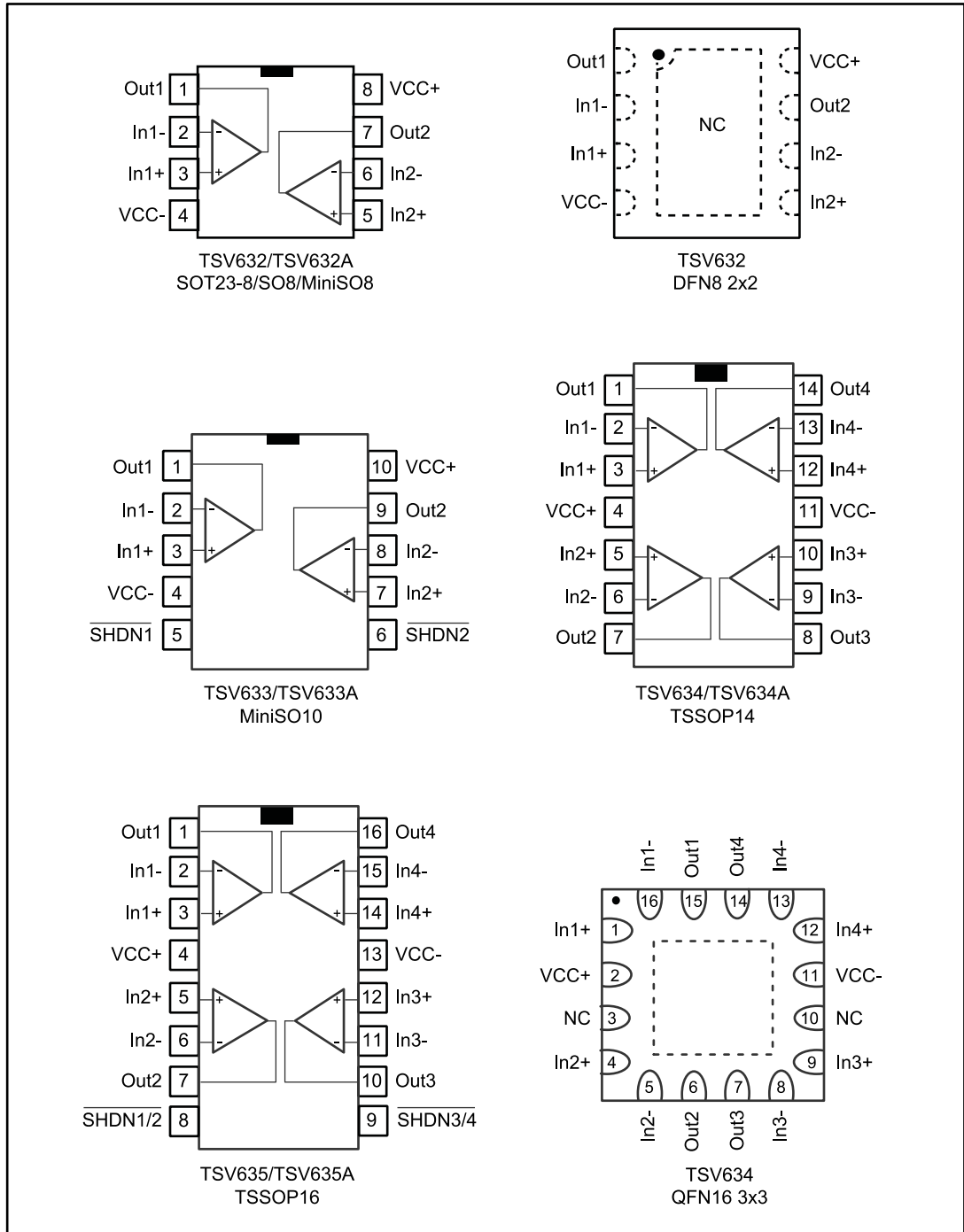
Reference	Dual version		Quad version	
	Without standby	With standby	Without standby	With standby
TSV63x	TSV632	TSV633	TSV634	TSV635
TSV63xA	TSV632A	TSV633A	TSV634A	TSV635A

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# 1 Package pin connections

Figure 1: Pin connections for each package (top view)



1. The exposed pads of the DFN8 2x2 and the QFN16 3x3 can be connected to  $V_{CC-}$  or left floating.



## 2 Absolute maximum ratings and operating conditions

Table 2: Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit	
V <sub>CC</sub>	Supply voltage <sup>(1)</sup>	6	V	
V <sub>id</sub>	Differential input voltage <sup>(2)</sup>	±V <sub>CC</sub>		
V <sub>in</sub>	Input voltage <sup>(3)</sup>	(V <sub>CC-</sub> ) - 0.2 to (V <sub>CC+</sub> ) + 0.2		
I <sub>in</sub>	Input current <sup>(4)</sup>	10	mA	
$\overline{\text{SHDN}}$ SHDN	Shutdown voltage <sup>(3)</sup>	(V <sub>CC-</sub> ) - 0.2 to (V <sub>CC+</sub> ) + 0.2	V	
T <sub>stg</sub>	Storage temperature	-65 to 150	°C	
R <sub>thja</sub>	Thermal resistance junction to ambient <sup>(5/6)</sup>	DFN8 2x2	57	°C/W
		SOT23-8	105	
		MiniSO8	190	
		MiniSO10	113	
		SO8	125	
		QFN16 3x3	39	
		TSSOP14	100	
TSSOP16	95			
T <sub>j</sub>	Maximum junction temperature	150	°C	
ESD	HBM: human body model <sup>(7)</sup>	4000	V	
	MM: machine model <sup>(8)</sup>	300		
	CDM: charged device model <sup>(9)</sup>	1500		
	Latch-up immunity	200	mA	

**Notes:**

- <sup>(1)</sup>All voltage values, except the differential voltage are with respect to the network ground terminal.
- <sup>(2)</sup>Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
- <sup>(3)</sup>V<sub>CC</sub> - V<sub>IN</sub> must not exceed 6 V, V<sub>IN</sub> must not exceed 6 V.
- <sup>(4)</sup>Input current must be limited by a resistor in series with the inputs
- <sup>(5)</sup>R<sub>th</sub> are typical values
- <sup>(6)</sup>Short-circuits can cause excessive heating and destructive dissipation
- <sup>(7)</sup>Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
- <sup>(8)</sup>Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating
- <sup>(9)</sup>Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

Table 3: Operating conditions

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	1.5 to 5.5	V
$V_{ICM}$	Common-mode input voltage range	$(V_{CC-}) - 0.1$ to $(V_{CC+}) + 0.1$	
$T_{oper}$	Operating free-air temperature range	-40 to 125	°C

### 3 Electrical characteristics

Table 4: Electrical characteristics at VCC+ = 1.8 V with VCC- = 0 V, Vicm = VCC/2, Tamb = 25° C, and RL connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
V <sub>io</sub>	Offset voltage	TSV63x			3	mV
		TSV63xA			0.8	
		TSV633AIST (MiniSO10)			1	
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub> - TSV63x			4.5	
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub> - TSV63xA			2	
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub> - TSV633AIST			2.2	
ΔV <sub>io</sub> /ΔT	Input offset voltage drift			2		μV/°C
I <sub>io</sub>	Input offset current	(V <sub>out</sub> = V <sub>CC</sub> /2)		1	10 <sup>(1)</sup>	pA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>		1	100	
I <sub>ib</sub>	Input bias current	(V <sub>out</sub> = V <sub>CC</sub> /2)		1	10 <sup>(1)</sup>	pA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>		1	100	
CMR	Common mode rejection ratio 20 log (ΔV <sub>ic</sub> /ΔV <sub>io</sub> )	0 V to 1.8 V, V <sub>out</sub> = 0.9 V	53	74		dB
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	51			
A <sub>vd</sub>	Large signal voltage gain	R <sub>L</sub> = 10 kΩ, V <sub>out</sub> = 0.5 V to 1.3 V	85	95		dB
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	80			
V <sub>OH</sub>	High level output voltage, (V <sub>OH</sub> = V <sub>CC</sub> - V <sub>out</sub> )	R <sub>L</sub> = 10 kΩ		5	35	mV
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			50	
V <sub>OL</sub>	Low level output voltage	R <sub>L</sub> = 10 kΩ		4	35	mV
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			50	
I <sub>out</sub>	I <sub>sink</sub>	V <sub>o</sub> = 1.8 V	6	12		mA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	4			
	I <sub>source</sub>	V <sub>o</sub> = 0 V	6	10		
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	4			
I <sub>CC</sub>	Supply current (per channel)	No load, V <sub>out</sub> = V <sub>CC</sub> /2	40	50	60	μA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			62	
<b>AC performance</b>						
GBP	Gain bandwidth product	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF, f = 100 kHz	700	790		kHz
φ <sub>m</sub>	Phase margin	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF		45		Degrees
G <sub>m</sub>	Gain margin	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF		13		dB
SR	Slew rate	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF, A <sub>v</sub> = 1	0.2	0.27		V/μs
e <sub>n</sub>	Equivalent input noise voltage	f = 1 kHz		60		nV/√Hz
		f = 10 kHz		33		

**Notes:**

<sup>(1)</sup>Guaranteed by design



Table 5: Shutdown characteristics VCC = 1.8 V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
I <sub>CC</sub>	Supply current in shutdown mode (all channels)	$\overline{\text{SHDN}} = V_{CC-}$		2.5	50	nA
		T <sub>min</sub> < T <sub>op</sub> < 85° C			200	
		T <sub>min</sub> < T <sub>op</sub> < 125° C				1.5
t <sub>on</sub>	Amplifier turn-on time	R <sub>L</sub> = 2 kΩ, V <sub>out</sub> = (V <sub>CC-</sub> ) to (V <sub>CC-</sub> ) + 0.2 V		200		ns
t <sub>off</sub>	Amplifier turn-off time	R <sub>L</sub> = 2 kΩ, V <sub>out</sub> = (V <sub>CC+</sub> ) - 0.5 V to (V <sub>CC+</sub> ) - 0.7 V		20		
V <sub>IH</sub>	$\overline{\text{SHDN}}$ logic high		1.35			V
V <sub>IL</sub>	$\overline{\text{SHDN}}$ logic low				0.6	
I <sub>IH</sub>	$\overline{\text{SHDN}}$ current high	$\overline{\text{SHDN}} = V_{CC+}$		10		pA
I <sub>IL</sub>	$\overline{\text{SHDN}}$ current low	$\overline{\text{SHDN}} = V_{CC-}$		10		
I <sub>OLeak</sub>	Output leakage in shutdown mode	$\overline{\text{SHDN}} = V_{CC-}$		50		
		T <sub>min</sub> < T <sub>op</sub> < 125° C		1		nA



Table 6: VCC+ = 3.3 V, VCC- = 0 V, Vicm = VCC/2, Tamb = 25° C, RL connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
V <sub>io</sub>	Offset voltage	TSV63x			3	mV
		TSV63xA			0.8	
		TSV633AIST (MiniSO10)			1	
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub> - TSV63x			4.5	
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub> - TSV63xA			2	
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub> - TSV633AIST			2.2	
ΔV <sub>io</sub> /ΔT	Input offset voltage drift			2		μV/°C
I <sub>io</sub>	Input offset current	V <sub>out</sub> = V <sub>CC</sub> /2		1	10 <sup>(1)</sup>	pA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>		1	100	
I <sub>ib</sub>	Input bias current	V <sub>out</sub> = V <sub>CC</sub> /2		1	10 <sup>(1)</sup>	pA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>		1	100	
CMR	Common mode rejection ratio 20 log (ΔV <sub>ic</sub> /ΔV <sub>io</sub> )	0 V to 3.3 V, V <sub>out</sub> = 1.65 V	57	79		dB
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	53			
A <sub>vd</sub>	Large signal voltage gain	R <sub>L</sub> = 10 kΩ, V <sub>out</sub> = 0.5 V to 2.8 V	88	98		dB
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	83			
V <sub>OH</sub>	High level output voltage, (V <sub>OH</sub> = V <sub>CC</sub> - V <sub>out</sub> )	R <sub>L</sub> = 10 kΩ		5	35	mV
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			50	
V <sub>OL</sub>	Low level output voltage	R <sub>L</sub> = 10 kΩ		4	35	mV
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			50	
I <sub>out</sub>	I <sub>sink</sub>	V <sub>o</sub> = 3.3 V	23	45		mA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	20			
	I <sub>source</sub>	V <sub>o</sub> = 0 V	23	38		
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	20			
I <sub>CC</sub>	Supply current, (per channel)	No load, V <sub>out</sub> = 1.75 V	43	55	64	μA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			66	
<b>AC performance</b>						
GBP	Gain bandwidth product	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF, f = 100 kHz	710	860		kHz
φ <sub>m</sub>	Phase margin	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF		46		Degrees
G <sub>m</sub>	Gain margin	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF		13		dB
SR	Slew rate	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF, A <sub>V</sub> = 1	0.22	0.29		V/μs

**Notes:**

<sup>(1)</sup>Guaranteed by design

Table 7: Electrical characteristics at VCC+ = 5 V with VCC- = 0 V, Vicm = VCC/2, Tamb = 25° C, and RL connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
V <sub>io</sub>	Offset voltages	TSV63x			3	mV
		TSV63xA			0.8	
		TSV633AIST ( MiniSO10)			1	
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub> - TSV63x			4.5	
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub> - TSV63xA			2	
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub> - TSV633AIST			2.2	
ΔV <sub>io</sub> /ΔT	Input offset voltage drift			2		μV/°C
I <sub>io</sub>	Input offset current	(V <sub>out</sub> = V <sub>CC</sub> /2)		1	10 <sup>(1)</sup>	pA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>		1	100	
I <sub>ib</sub>	Input bias current	(V <sub>out</sub> = V <sub>CC</sub> /2)		1	10 <sup>(1)</sup>	pA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>		1	100	
CMR	Common mode rejection ratio 20 log (ΔV <sub>ic</sub> /ΔV <sub>io</sub> )	0 V to 5 V, V <sub>out</sub> = 2.5 V	60	80		dB
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	55			
SVR	Supply voltage rejection ratio 20 log (ΔV <sub>CC</sub> /ΔV <sub>io</sub> )	V <sub>CC</sub> = 1.8 to 5 V	75	102		dB
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	73			
A <sub>vd</sub>	Large signal voltage gain	R <sub>L</sub> = 10 kΩ, V <sub>out</sub> = 0.5 V to 4.5 V	89	98		dB
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	84			
EMIRR	EMI rejection ratio, EMIRR = -20 log (V <sub>RFpeak</sub> /ΔV <sub>io</sub> )	V <sub>RF</sub> = 100 mV <sub>rms</sub> , f = 400 MHz		61		dB
		V <sub>RF</sub> = 100 mV <sub>rms</sub> , f = 900 MHz		85		
		V <sub>RF</sub> = 100 mV <sub>rms</sub> , f = 1800 MHz		92		
		V <sub>RF</sub> = 100 mV <sub>rms</sub> , f = 2400 MHz		83		
V <sub>OH</sub>	High level output voltage, (V <sub>OH</sub> = V <sub>CC</sub> - V <sub>out</sub> )	R <sub>L</sub> = 10 kΩ		7	35	mV
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			50	
V <sub>OL</sub>	Low level output voltage	R <sub>L</sub> = 10 kΩ		6	35	mV
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			50	
I <sub>out</sub>	I <sub>sink</sub>	V <sub>o</sub> = 5 V	40	69		mA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	35			
	I <sub>source</sub>	V <sub>o</sub> = 0 V	40	74		
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	35			
I <sub>CC</sub>	Supply current, (per channel)	No load, V <sub>out</sub> = V <sub>CC</sub> /2	50	60	69	μA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			72	
<b>AC performance</b>						
GBP	Gain bandwidth product	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF, f = 100 kHz	730	880		kHz
F <sub>u</sub>	Unity gain frequency	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF		830		
φ <sub>m</sub>	Phase margin	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF		48		Degrees

Electrical characteristics

TSV632, TSV632A, TSV633, TSV633A, TSV634, TSV634A, TSV635, TSV635A

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$G_m$	Gain margin	$R_L = 2\text{ k}\Omega, C_L = 100\text{ pF}$		13		dB
SR	Slew rate	$R_L = 2\text{ k}\Omega, C_L = 100\text{ pF}, A_v = 1$	0.25	0.34		V/ $\mu$ s
$e_n$	Equivalent input noise voltage	$f = 1\text{ kHz}$		60		nV/ $\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		33		
THD+ $e_n$	Total harmonic distortion + noise	$V_{CC} = 5\text{V}, f = 1\text{ kHz}, A_v = 1, R_L = 100\text{ k}\Omega, V_{icm} = V_{CC}/2, V_{out} = 2V_{pp}$		0.002		%

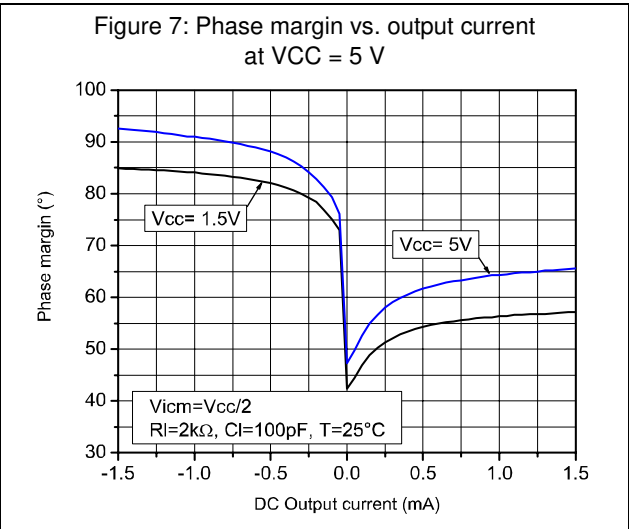
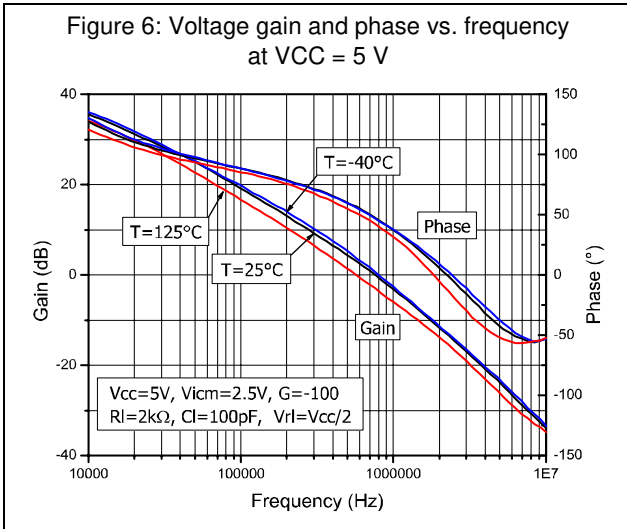
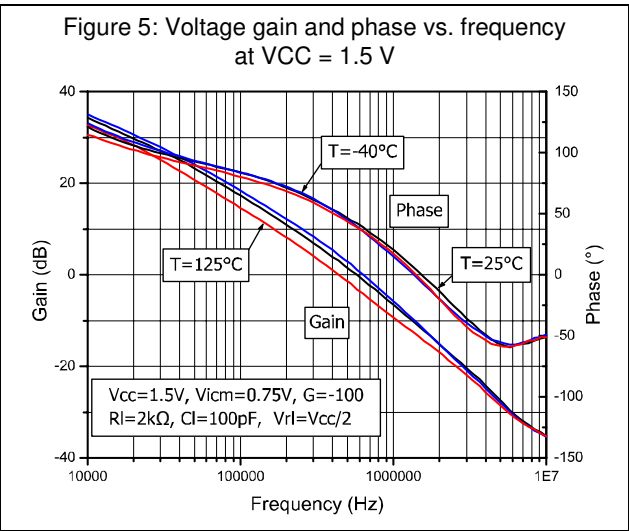
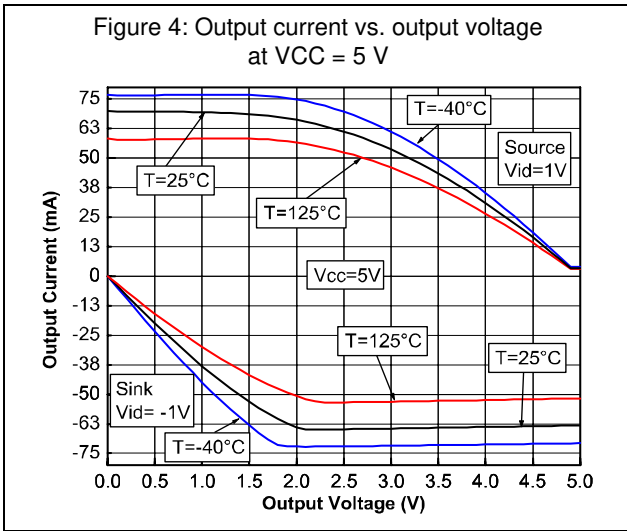
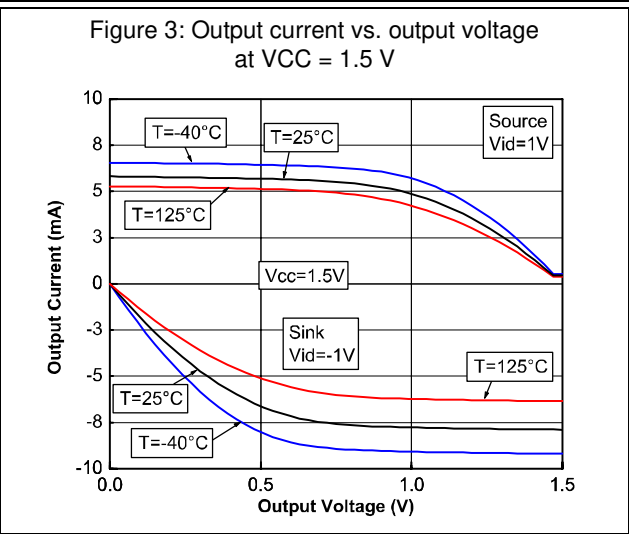
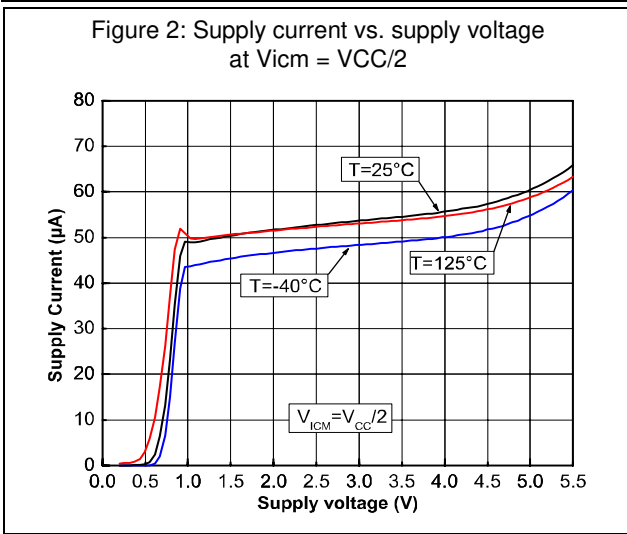
Notes:

(1) Guaranteed by design

Table 8: Shutdown characteristics at  $V_{CC} = 5\text{ V}$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
$I_{CC}$	Supply current in shutdown mode (all channels)	$\overline{\text{SHDN}} = V_{CC-}$		5	50	nA
		$T_{min} < T_{op} < 85^\circ\text{ C}$			200	
		$T_{min} < T_{op} < 125^\circ\text{ C}$				1.5
$t_{on}$	Amplifier turn-on time	$R_L = 2\text{ k}\Omega, V_{out} = (V_{CC-})$ to $(V_{CC-}) + 0.2\text{ V}$		200		ns
$t_{off}$	Amplifier turn-off time	$R_L = 2\text{ k}\Omega, V_{out} = (V_{CC+}) - 0.5\text{ V}$ to $(V_{CC+}) - 0.7\text{ V}$		20		
$V_{IH}$	$\overline{\text{SHDN}}$ logic high		2			V
$V_{IL}$	$\overline{\text{SHDN}}$ logic low				0.8	
$I_{IH}$	$\overline{\text{SHDN}}$ current high	$\overline{\text{SHDN}} = V_{CC+}$		10		pA
$I_{IL}$	$\overline{\text{SHDN}}$ current low	$\overline{\text{SHDN}} = V_{CC-}$		10		
$I_{OLeak}$	Output leakage in shutdown mode	$\overline{\text{SHDN}} = V_{CC-}$		50		
		$T_{min} < T_{op} < 125^\circ\text{ C}$		1		nA





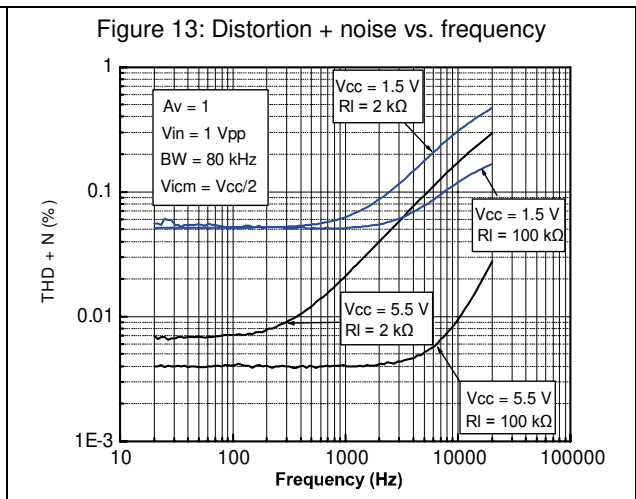
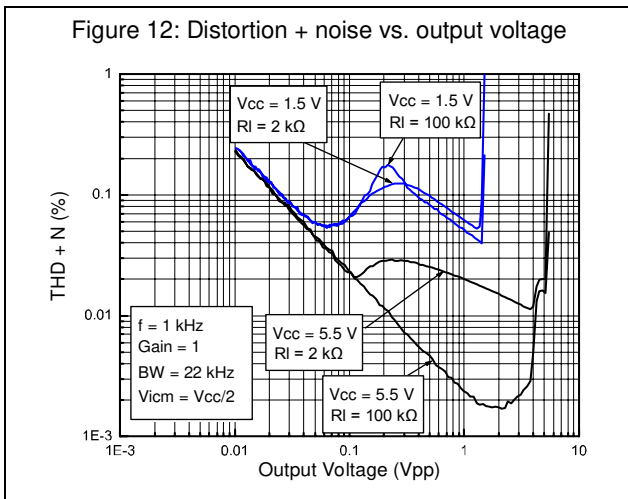
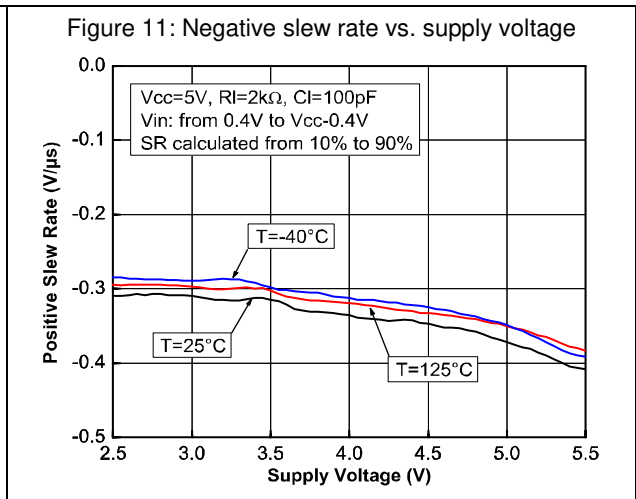
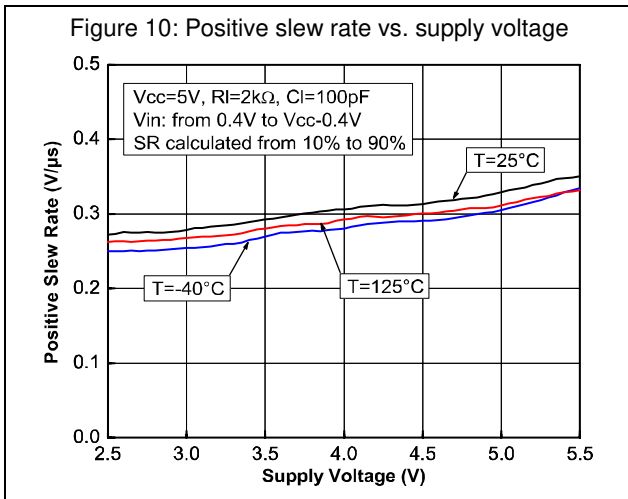
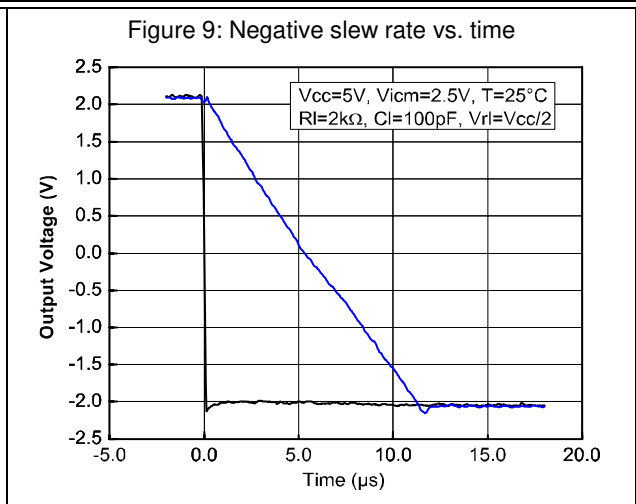
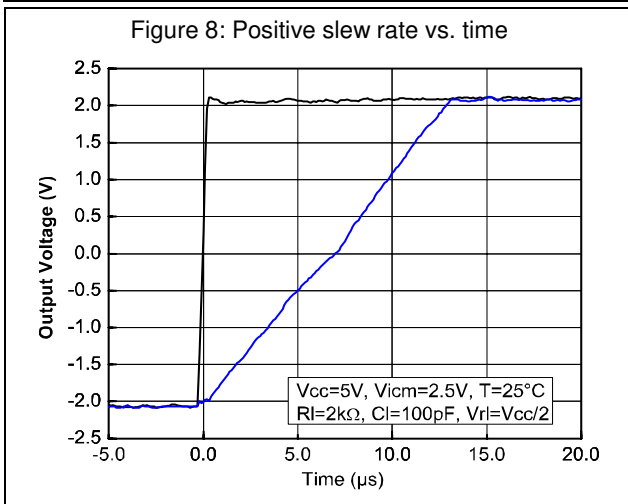


Figure 14: Noise vs. frequency

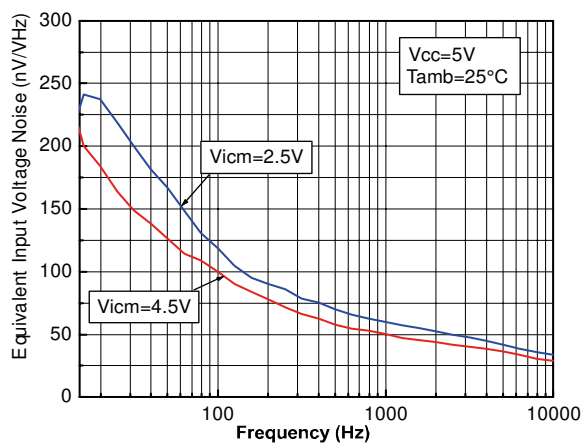
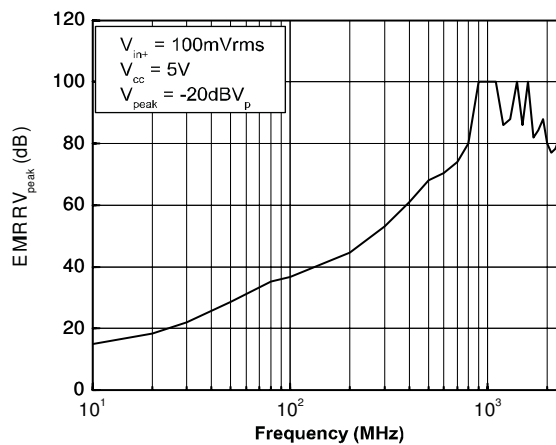


Figure 15: EMIRR vs. frequency at VCC = 5 V,  
T = 25 °C





## 4 Application information

### 4.1 Operating voltages

The TSV63x and TSV63xA can operate from 1.5 to 5.5 V. Their parameters are fully specified for 1.8 V, 3.3 V, and 5 V power supplies. However, the parameters are very stable in the full  $V_{CC}$  range and several characterization curves show the TSV63x and TSV63xA characteristics at 1.5 V. Additionally, the main specifications are guaranteed in extended temperature ranges from  $-40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ .

### 4.2 Rail-to-rail input

The TSV63x and TSV63xA are built with two complementary PMOS and NMOS input differential pairs. The devices have a rail-to-rail input and the input common mode range is extended from  $(V_{CC-}) - 0.1\text{ V}$  to  $(V_{CC+}) + 0.1\text{ V}$ . The transition between the two pairs appears at  $(V_{CC+}) - 0.7\text{ V}$ . In the transition region, the performance of CMRR, PSRR,  $V_{io}$  (Figure 16 and Figure 17), and THD is slightly degraded.

Figure 16: Input offset voltage vs input common mode voltage at  $V_{CC} = 1.5\text{ V}$

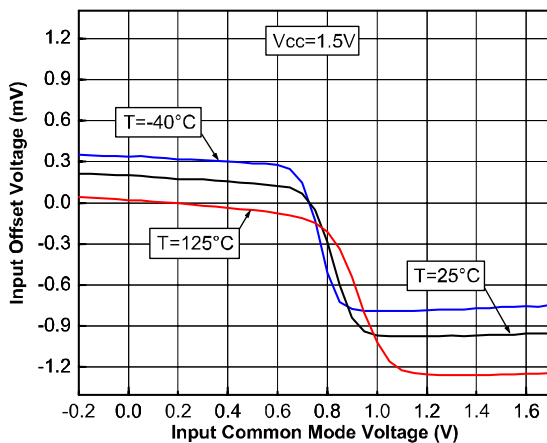
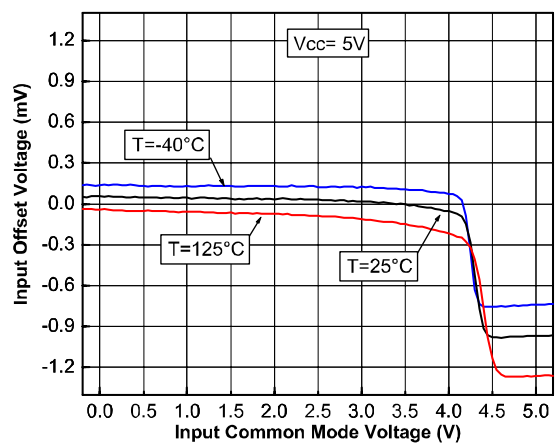


Figure 17: Input offset voltage vs input common mode voltage at  $V_{CC} = 5\text{ V}$



The devices are guaranteed without phase reversal.

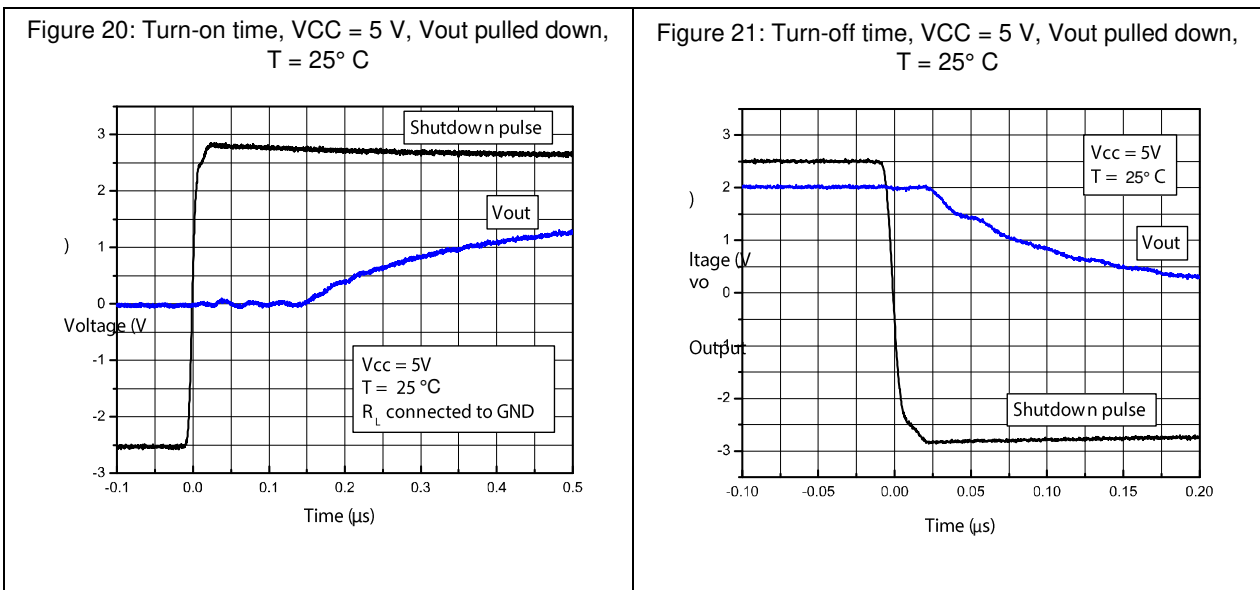
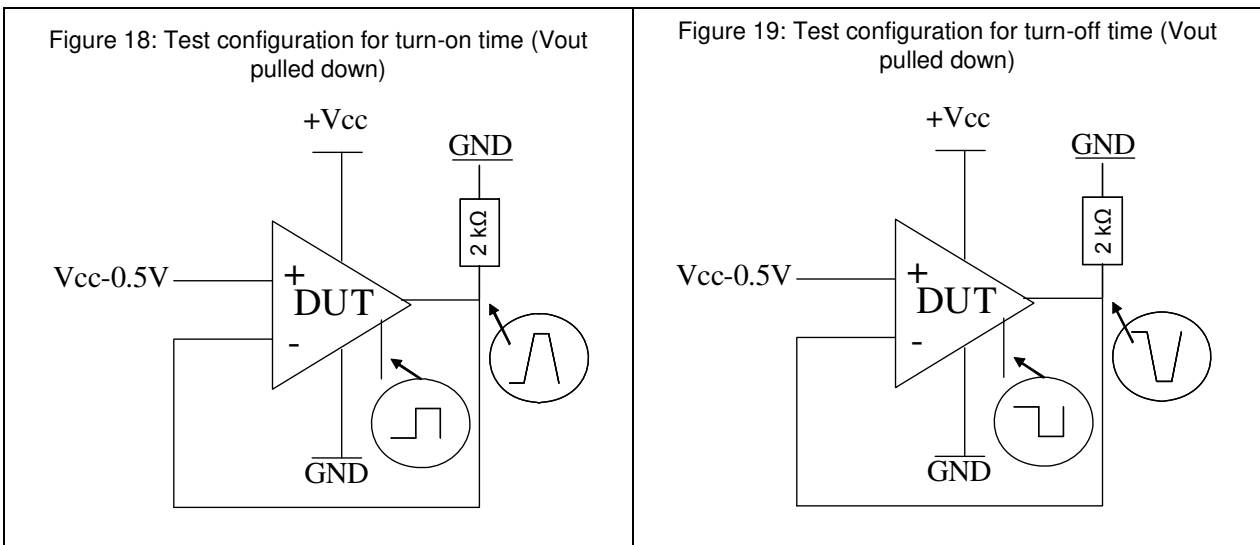
### 4.3 Rail-to-rail output

The operational amplifiers' output levels can go close to the rails: 35 mV maximum above and below the rail when connected to a  $10\text{ k}\Omega$  resistive load to  $V_{CC}/2$ .

### 4.4 Shutdown function (TSV633, TSV635)

The operational amplifiers are enabled when the  $\overline{\text{SHDN}}$  pin is pulled high. To disable the amplifiers, the  $\overline{\text{SHDN}}$  must be pulled down to  $V_{CC-}$ . When in shutdown mode, the amplifiers' output is in a high impedance state. The  $\overline{\text{SHDN}}$  pin must never be left floating, but tied to  $V_{CC+}$  or  $V_{CC-}$ .

The turn-on and turn-off times are calculated for an output variation of  $\pm 200$  mV. [Figure 18](#) and [Figure 19](#) show the test configurations. [Figure 20](#) shows the time it takes the product to come out of shutdown mode and [Figure 21](#) shows the time it takes the product to enter shutdown mode.



## 4.5 Optimization of DC and AC parameters

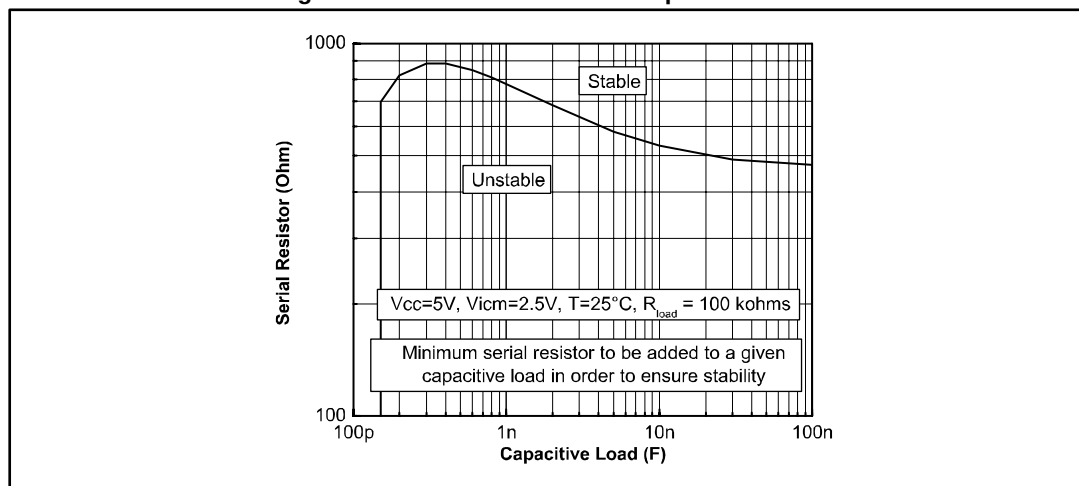
These devices use an innovative approach to reduce the spread of the main DC and AC parameters. An internal adjustment achieves a very narrow spread of the current consumption (60  $\mu\text{A}$  typical, min/max at  $\pm 17\%$ ). Parameters linked to the current consumption value, such as GBP, SR, and  $A_{vd}$ , benefit from this narrow dispersion. All parts present a similar speed and the same behavior in terms of stability. In addition, the minimum values of GBP and SR are guaranteed (GBP = 730 kHz minimum and SR = 0.25 V/ $\mu\text{s}$  minimum).

## 4.6 Driving resistive and capacitive loads

These products are micropower, low-voltage, operational amplifiers optimized to drive rather large resistive loads, above 2 k $\Omega$ . For lower resistive loads, the THD level may significantly increase.

In a *follower* configuration, these operational amplifiers can drive capacitive loads up to 100 pF with no oscillations. When driving larger capacitive loads, adding an in-series resistor at the output can improve the stability of the devices (see [Figure 22](#) for recommended in-series resistor values). Once the in-series resistor value has been selected, the stability of the circuit should be tested on the bench and simulated with the simulation model.

Figure 22: In-series resistor vs. capacitive load



## 4.7 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

## 4.8 Macromodel

Two accurate macromodels (with or without the shutdown feature) of the TSV63x and TSV63xA are available on STMicroelectronics' web site at [www.st.com](http://www.st.com). These models are a trade-off between accuracy and complexity (that is, time simulation) of the TSV63x and TSV63xA operational amplifiers. They emulate the nominal performances of a typical device within the specified operating conditions mentioned in the datasheet. They also help to validate a design approach and to select the right operational amplifier, *but they do not replace on-board measurements*.

## 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

## 5.1 DFN8 2 x 2 (NB) package information

Figure 23: DFN8 2 x 2 mm (NB) package outline

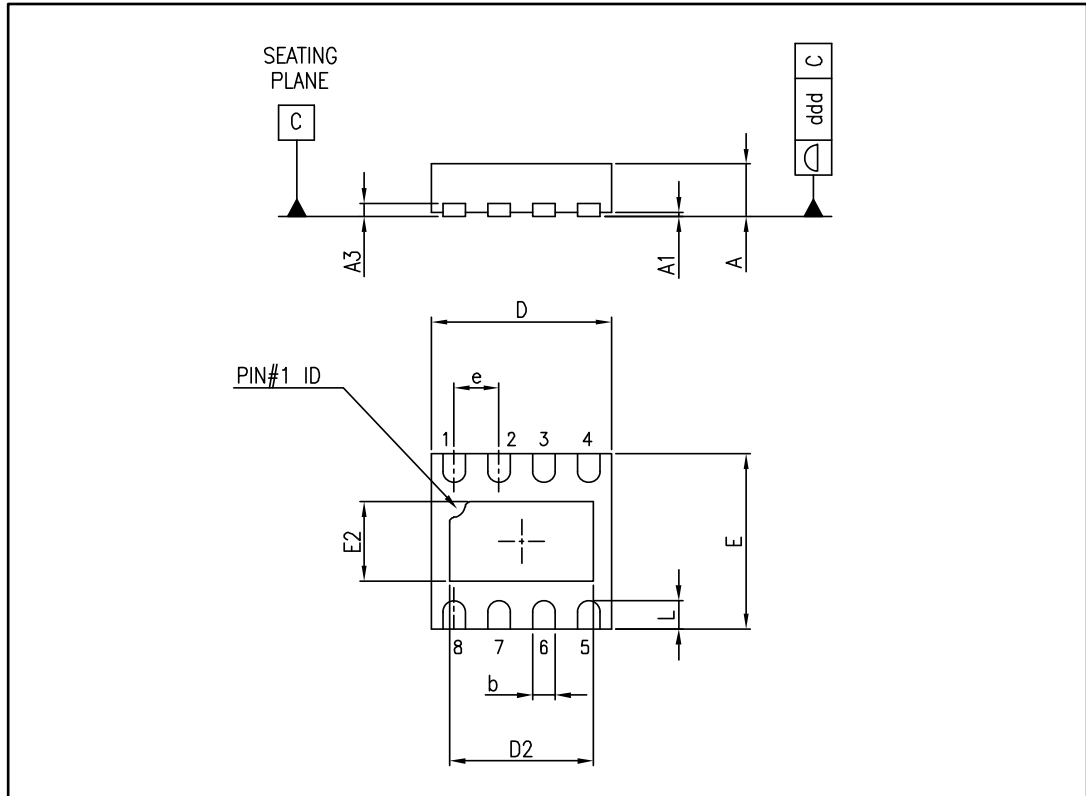
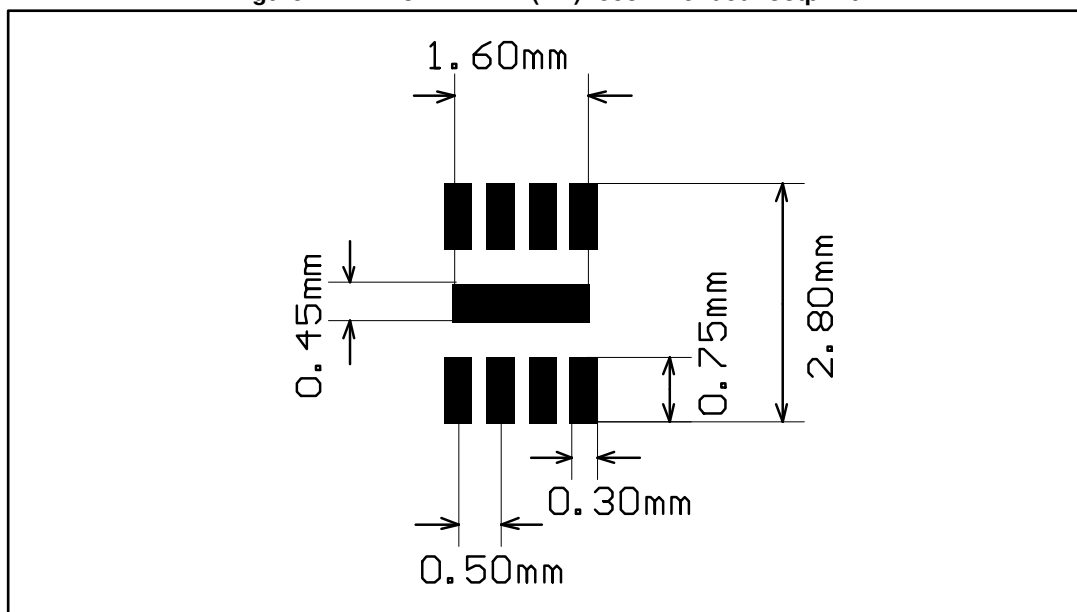


Table 9: DFN8 2 x 2 x 0.6 mm (NB) package mechanical data (pitch 0.5 mm)

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002
A3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.039
e		0.50			0.020	
L			0.425			0.017
ddd			0.08			0.003



Figure 24: DFN8 2 x 2 mm (NB) recommended footprint



## 5.2 SOT23-8 package information

Figure 25: SOT23-8 package outline

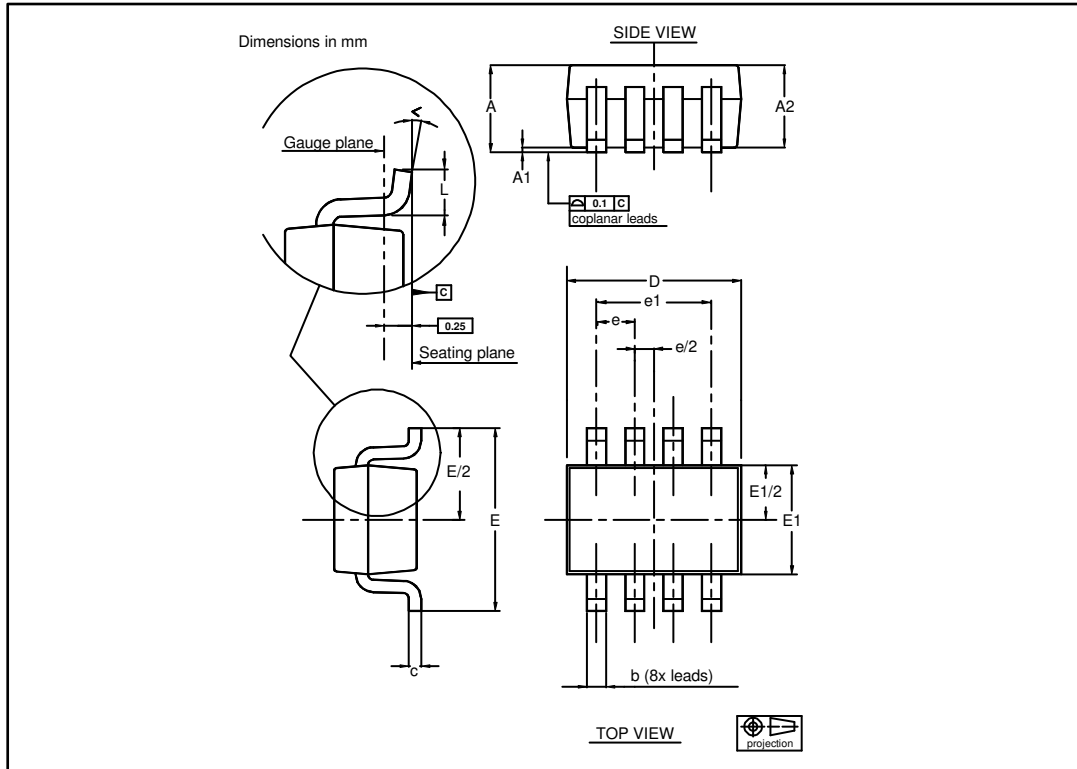


Table 10: SOT23-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.45			0.057
A1			0.15			0.006
A2	0.90		1.30	0.035		0.051
b	0.22		0.38	0.009		0.015
c	0.08		0.22	0.003		0.009
D	2.80		3.00	0.110		0.118
E	2.60		3.00	0.102		0.118
E1	1.50		1.75	0.059		0.069
e		0.65			0.026	
e1		1.95			0.077	
L	0.30		0.60	0.012		0.024
<	0°		8°	0°		8°

### 5.3 MiniSO8 package information

Figure 26: MiniSO8 package outline

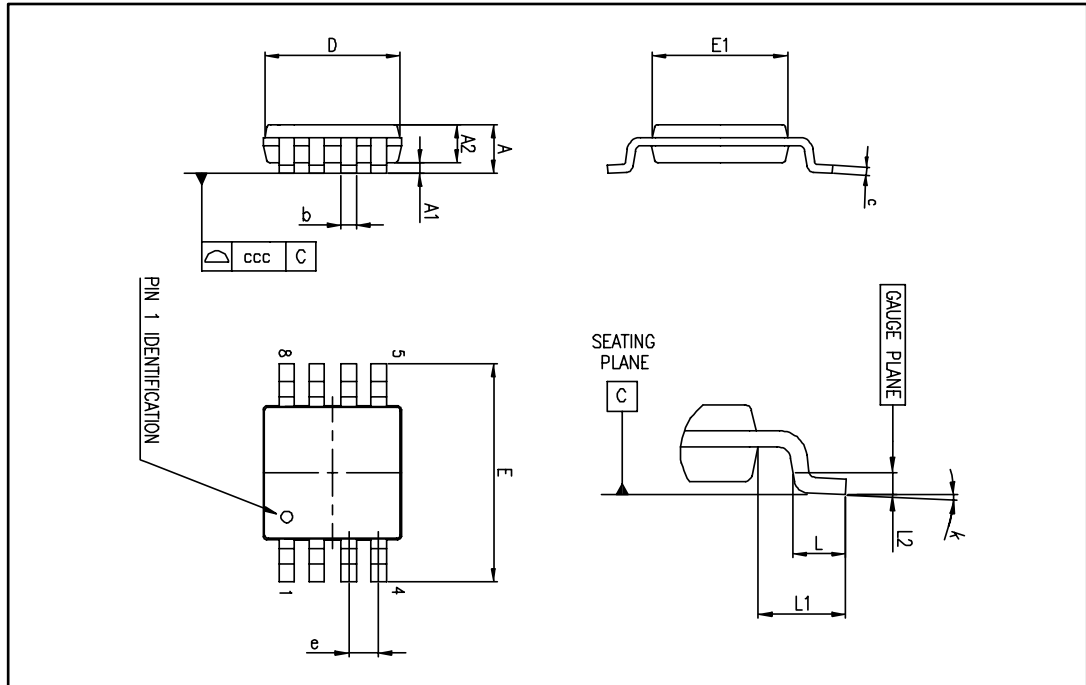


Table 11: MiniSO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

## 5.4 MiniSO10 package information

Figure 27: MiniSO10 package outline

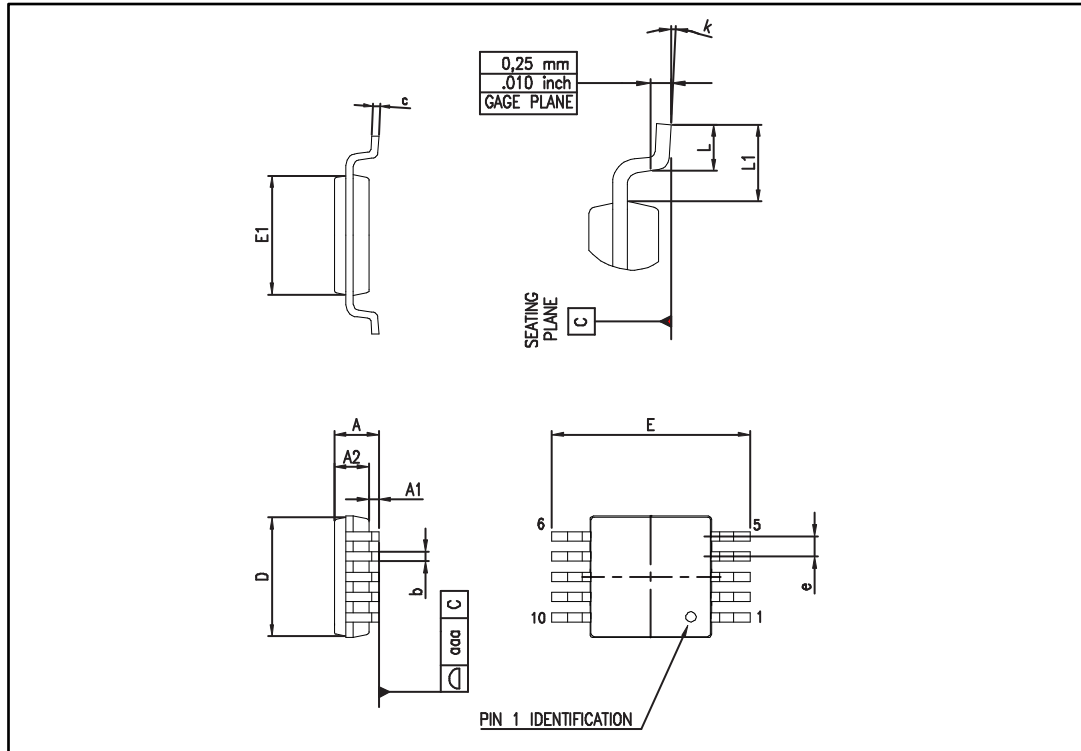


Table 12: MiniSO-10 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.10			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.78	0.86	0.94	0.031	0.034	0.037
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.15	0.23	0.30	0.006	0.009	0.012
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	0.114	0.118	0.122
e		0.50			0.020	
L	0.40	0.55	0.70	0.016	0.022	0.028
L1		0.95			0.037	
k	0°	3°	6°	0°	3°	6°
aaa			0.10			0.004

### 5.5 SO8 package information

Figure 28: SO8 package outline

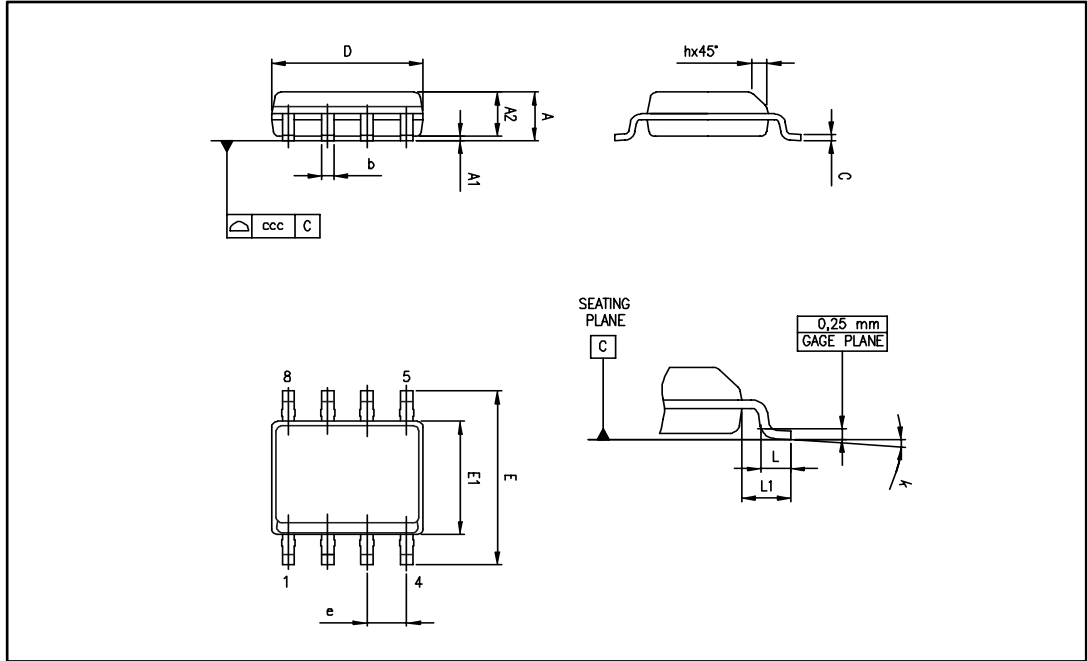


Table 13: SO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	1°		8°	1°		8°
ccc			0.10			0.004

### 5.6 QFN16 3x3 package information

Figure 29: QFN16 3x3 mm package outline

