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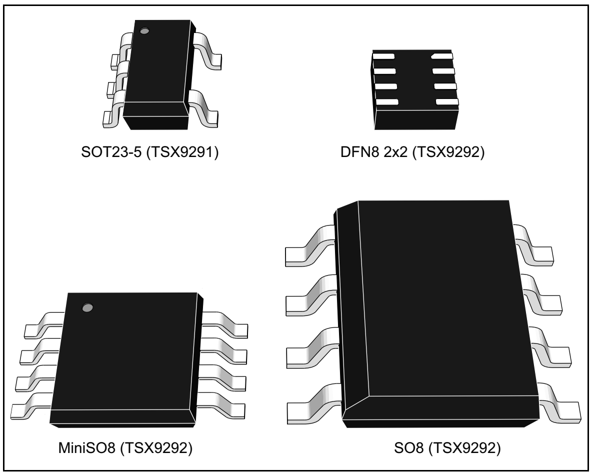
TSX9291, TSX9292

16 MHz rail-to-rail CMOS 16 V operational amplifiers

Datasheet - production data



Features

- Rail-to-rail input and output
- Wide supply voltage: 4 V - 16 V
- Gain bandwidth product: 16 MHz typ at 16 V
- Low power consumption: 2.8 mA typ at 16 V
- Slew rate: 27 V/µs
- Stable when used in gain configuration
- Low input bias current: 10 pA typ
- High tolerance to ESD: 4 kV HBM
- Extended temperature range: -40° C to +125° C
- Automotive qualification

Related products

- See the TSX5 series for low power features
- See the TSX6 series for micro power features
- See the TSX92 series for unity gain stability
- See the TSV9 series for lower voltage

Applications

- Communications
- Process control
- Active filtering
- Test equipment

Description

The TSX9291 and TSX9292 operational amplifiers (op-amps) offer excellent AC characteristics such as 16 MHz gain bandwidth, 27 V/µs slew rate, and 0.0003 % THD+N. They are decompensated amplifiers which are stable when used with a gain higher than 2 or lower than -1. The rail-to-rail input and output capability of these devices operates on a wide supply voltage range of 4 V to 16 V. These last two features make the TSX929x series particularly well-adapted for a wide range of applications such as communications, I/V amplifiers for ADCs, and active filtering applications.

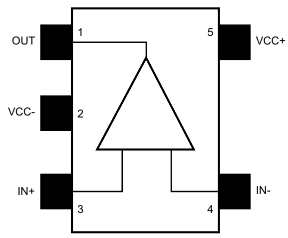
Table 1. Device summary

	Single	Dual
Op-amp version	TSX9291	TSX9292

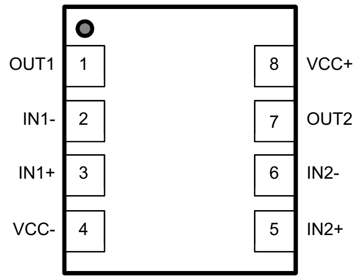
Contents

1 Package pin connections

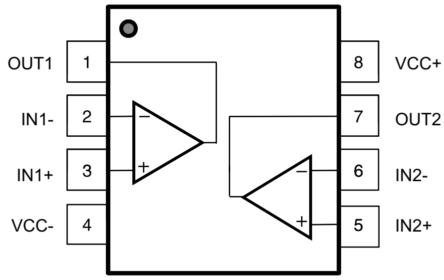
Figure 1. Pin connections (top view)



SOT23-5 (TSX9291)



DFN8 2x2 (TSX9292)



MiniSO8/SO8 (TSX9292)

2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	18	V
V_{id}	Differential input voltage(2)	$\pm V_{CC}$	mV
V_{in}	Input voltage	V_{CC-} - 0.2 to V_{CC+} + 0.2	V
I_{in}	Input current(3)	10	mA
T_{stg}	Storage temperature	-65 to +150	°C
R_{thja}	Thermal resistance junction to ambient(4)(5) SOT23-5 DFN8 2x2 MiniSO8 SO8	 250 57 190 125	°C/W
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model(6)	4000	V
	MM: machine model(7)	100	
	CDM: charged device model(8)	1500	
	Latch-up immunity	200	mA

1. All voltage values, except the differential voltage are with respect to network ground terminal.
2. The differential voltage is the non-inverting input terminal with respect to the inverting input terminal.
3. Input current must be limited by a resistor in series with the inputs.
4. Short-circuits can cause excessive heating and destructive dissipation.
5. R_{th} are typical values.
6. According to JEDEC standard JESD22-A114F
7. According to JEDEC standard JESD22-A115A
8. According to ANSI/ESD STM5.3.1

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	4 to 16	V
V_{icm}	Common mode input voltage range	V_{CC-} - 0.1 to V_{CC+} + 0.1	
T_{oper}	Operating free air temperature range	-40 to +125	°C

3 Electrical characteristics

Table 4. Electrical characteristics at V_{CC+} = +4.5 V with V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, T_{amb} = 25 ° C, and R_L = 10 kΩ connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	V_{icm} = 2 V $T_{min} < T_{op} < T_{max}$			4 5	mV
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2	10	µV/°C
ΔV_{io}	Long-term input offset voltage drift(1)(2)	TSX9291 TSX9292		6 9		$\frac{nV}{\sqrt{month}}$
I_{ib}	Input bias current	$V_{out} = V_{CC}/2$ $T_{min} < T_{op} < T_{max}$		10	100 200	pA
I_{io}	Input offset current	$V_{out} = V_{CC}/2$ $T_{min} < T_{op} < T_{max}$		10	100 200	
R_{IN}	Input resistance			1		TΩ
C_{IN}	Input capacitance			8		pF
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	V_{icm} = -0.1 V to 2 V, $V_{OUT} = V_{CC}/2$ $T_{min} < T_{op} < T_{max}$ V_{icm} = -0.1 V to 4.6 V, $V_{OUT} = V_{CC}/2$ $T_{min} < T_{op} < T_{max}$	61 59 59 57	82 72		dB
A_{vd}	Large signal voltage gain	R_L= 2 kΩ, V_{out} = 0.3 V to 4.2 V $T_{min} < T_{op} < T_{max}$ R_L= 10 kΩ, V_{out} = 0.2 V to 4.3 V $T_{min} < T_{op} < T_{max}$	100 90 100 90	108 112		
V_{OH}	High level output voltage	R_L= 2 kΩ to $V_{CC}/2$ $T_{min} < T_{op} < T_{max}$ R_L= 10 kΩ to $V_{CC}/2$ $T_{min} < T_{op} < T_{max}$		50 10	80 100 16 20	mV from V_{CC}+
V_{OL}	Low level output voltage	R_L= 2 kΩ to $V_{CC}/2$ $T_{min} < T_{op} < T_{max}$ R_L= 10 kΩ to $V_{CC}/2$ $T_{min} < T_{op} < T_{max}$		42 9	80 100 16 20	mV
I_{out}	I_{sink}	V_{out} = 4.5 V $T_{min} < T_{op} < T_{max}$	16 13	21		mA
	I_{source}	V_{out} = 0 V $T_{min} < T_{op} < T_{max}$	16 13	21		
I_{CC}	Supply current (per amplifier)	No load, $V_{out} = V_{CC}/2$ $T_{min} < T_{op} < T_{max}$		2.9	3.4 3.5	
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 20 pF, G = 20 dB		15.6		MHz
F_U	Unity gain frequency	R_L = 10 kΩ, C_L = 20 pF		14.2		

Table 4. Electrical characteristics at V_{CC+} = +4.5 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 ° C, and R_L = 10 kΩ connected to V_{CC}/2 (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Gain	Minimum gain for stability	Phase margin = 60 °, R_g = R_f = 1 kΩ R_L = 10 kΩ, C_L = 20 pF		-1 +2		
SR+	Positive slew rate	Av = +1, V_{out} = 0.5 to 4.0 V Measured between 10 % to 90 %		27		V/µs
SR-	Negative slew rate	Av = +1, V_{out} = 4.0 to 0.5 V Measured between 90 % to 10 %		22		
e_n	Equivalent input noise voltage	f = 10 kHz f = 100 kHz		17.9 12.9		$\frac{nV}{\sqrt{Hz}}$
$\int e_n$	Low-frequency peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		8.1		μV_{pp}
THD+N	Total harmonic distortion + noise	f = 1 kHz, Av = +1, R_L = 10 kΩ, V_{out} = 2 V_{rms}		0.002		%

1. Typical value is based on the Vio drift observed after 1000h at 125°C extrapolated to 25°C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration. See *Section 4.6: Long-term input offset voltage drift*.

2. When used in comparator mode, with high differential input voltage, during a long period of time with V_{CC} close to 16V and V_{icm}>V_{CC}/2, Vio can experience a permanent drift of few mV drift. The phenomenon is particularly worsen at low temperatures.

Table 5. Electrical characteristics at V_{CC+} = +10 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 ° C, and R_L = 10 kΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	 T_{min} < T_{op} < T_{max}			4 5	mV
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2	10	μV/°C
ΔV_{io}	Long-term input offset voltage drift(1) (2)	TSX9291 TSX9292		92 128		$\frac{nV}{\sqrt{month}}$
I_{ib}	Input bias current	V_{out} = V_{CC}/2 T_{min} < T_{op} < T_{max}		10	100 200	pA
I_{io}	Input offset current	V_{out} = V_{CC}/2 T_{min} < T_{op} < T_{max}		10	100 200	pA
R_{IN}	Input resistance			1		TΩ
C_{IN}	Input capacitance			8		pF
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	V_{icm} = -0.1 V to 7 V, V_{OUT} = V_{CC}/2 T_{min} < T_{op} < T_{max} V_{icm} = -0.1 V to 10.1 V, V_{OUT} = V_{CC}/2 T_{min} < T_{op} < T_{max}	72 70 64 62	85 75		dB
A_{vd}	Large signal voltage gain	R_L = 2 kΩ, V_{out} = 0.3 V to 9.7 V T_{min} < T_{op} < T_{max} R_L = 10 kΩ, V_{out} = 0.2 V to 9.8 V T_{min} < T_{op} < T_{max}	100 90 100 90	107 117		dB
V_{OH}	High level output voltage	R_L = 2 kΩ to V_{CC}/2 T_{min} < T_{op} < T_{max} R_L = 10 kΩ to V_{CC}/2 T_{min} < T_{op} < T_{max}		94 31	110 130 40 50	mV from V_{CC+}
V_{OL}	Low level output voltage	R_L = 2 kΩ to V_{CC}/2 T_{min} < T_{op} < T_{max} R_L = 10 kΩ to V_{CC}/2 T_{min} < T_{op} < T_{max}		80 14	110 130 40 50	mV
I_{out}	I_{sink}	V_{out} = 10 V T_{min} < T_{op} < T_{max}	50 42	55		mA
I_{out}	I_{source}	V_{out} = 0 V T_{min} < T_{op} < T_{max}	75 70	82		mA
I_{CC}	Supply current (per amplifier)	No load, V_{out} = V_{CC}/2 T_{min} < T_{op} < T_{max}		3.1	3.6 3.6	mA
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 20 pF, G = 20 dB		16		MHz
F_U	Unity gain frequency	R_L = 10 kΩ, C_L = 20 pF		15.4		MHz
Gain	Minimum gain for stability	Phase margin = 60 °, R_g = R_f = 1 kΩ R_L = 10 kΩ, C_L = 20 pF		-1 +2		

Table 5. Electrical characteristics at V_{CC+} = +10 V with V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, T_{amb} = 25 ° C, and R_L= 10 kΩ connected to $V_{CC}/2$ (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SR+	Positive slew rate	Av = +1, V_{out} = 0.5 to 9.5 V Measured between 10 % to 90 %		29		V/µs
SR-	Negative slew rate	Av = +1, V_{out} = 9.5 to 0.5 V Measured between 90 % to 10 %		30		
e_n	Equivalent input noise voltage	f = 10 kHz f = 100 kHz		16.8 12		$\frac{nV}{\sqrt{Hz}}$
$\int e_n$	Low-frequency peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		8.64		μV_{pp}
THD+N	Total harmonic distortion + noise	f = 1 kHz, Av = +1, R_L = 10 kΩ, V_{out} = 2 V_{rms}		0.0006		%

1. Typical value is based on the Vio drift observed after 1000h at 125°C extrapolated to 25°C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration. See *Section 4.6: Long-term input offset voltage drift*.

2. When used in comparator mode, with high differential input voltage, during a long period of time with V_{CC} close to 16V and V_{icm}>$V_{CC}/2$, Vio can experience a permanent drift of few mV drift. The phenomenon is particularly worsen at low temperatures.

Table 6. Electrical characteristics at V_{CC+} = +16 V with V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, T_{amb} = 25 ° C, and R_L = 10 kΩ connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	 $T_{min} < T_{op} < T_{max}$			4 5	mV
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2	10	μV/°C
ΔV_{io}	Long-term input offset voltage drift(1) (2)	TSX9291 TSX9292		1.73 2.26		$\frac{\mu V}{\sqrt{month}}$
I_{ib}	Input bias current	$V_{out} = V_{CC}/2$ $T_{min} < T_{op} < T_{max}$		10	100 200	pA
I_{io}	Input offset current	$V_{out} = V_{CC}/2$ $T_{min} < T_{op} < T_{max}$		10	100 200	
R_{IN}	Input resistance			1		TΩ
C_{IN}	Input capacitance			8		pF
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	V_{icm} = -0.1 V to 13 V, $V_{OUT} = V_{CC}/2$ $T_{min} < T_{op} < T_{max}$ V_{icm} = -0.1 V to 16.1 V, $V_{OUT} = V_{CC}/2$ $T_{min} < T_{op} < T_{max}$	73 71 67 65	85 76		dB
SVR	Supply voltage rejection ratio	V_{cc} = 4.5 V to 16 V $T_{min} < T_{op} < T_{max}$	73 71	85		
A_{vd}	Large signal voltage gain	R_L = 2 kΩ, V_{out} = 0.3 V to 15.7 V $T_{min} < T_{op} < T_{max}$ R_L = 10 kΩ, V_{out} = 0.2 V to 15.8 V $T_{min} < T_{op} < T_{max}$	100 90 100 90	105 113		
V_{OH}	High level output voltage	R_L = 2 kΩ to $V_{CC}/2$ $T_{min} < T_{op} < T_{max}$ R_L = 10 kΩ to $V_{CC}/2$ $T_{min} < T_{op} < T_{max}$		150 43	200 230 50 70	mV from V_{CC+}
V_{OL}	Low level output voltage	R_L = 2 kΩ to $V_{CC}/2$ $T_{min} < T_{op} < T_{max}$ R_L = 10 kΩ to $V_{CC}/2$ $T_{min} < T_{op} < T_{max}$		140 30	200 230 50 70	mV
I_{out}	I_{sink}	V_{out} = 16 V $T_{min} < T_{op} < T_{max}$	45 40	50		mA
	I_{source}	V_{out} = 0 V $T_{min} < T_{op} < T_{max}$	65 60	74		
I_{CC}	Supply current (per amplifier)	No load, $V_{out} = V_{CC}/2$ $T_{min} < T_{op} < T_{max}$		2.8	3.4 3.4	
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 20 pF, G = 20 dB		16		MHz
F_U	Unity gain frequency	R_L = 10 kΩ, C_L = 20 pF		15.7		

Table 6. Electrical characteristics at V_{CC+} = +16 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 ° C, and R_L= 10 kΩ connected to V_{CC}/2 (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Gain	Minimum gain for stability	Phase margin = 60 °, R_g = R_f = 1 kΩ R_L = 10 kΩ, C_L = 20 pF		-1 +2		
SR+	Positive slew rate	Av = +1, V_{out} = 0.5 to 15.5 V Measured between 10 % to 90 %		26		V/μs
SR-	Negative slew rate	Av = +1, V_{out} = 15.5 to 0.5 V Measured between 90 % to 10 %		27		V/μs
e_n	Equivalent input noise voltage	f = 10 kHz f = 100 kHz		16.5 11.8		$\frac{nV}{\sqrt{Hz}}$
$\int e_n$	Low-frequency peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		8.58		μV_{pp}
THD+N	Total harmonic distortion + Noise	f = 1 kHz, Av = +1, R_L= 10 kΩ, V_{out} = 4V_{rms}		0.0003		%
t_S	Settling time	Gain = +1, 100 mV input voltage 0.1 % of final value 1 % of final value		 245 178		ns

1. Typical value is based on the Vio drift observed after 1000h at 125°C extrapolated to 25°C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration. See *Section 4.6: Long-term input offset voltage drift*.
2. When used in comparator mode, with high differential input voltage, during a long period of time with V_{CC} close to 16V and V_{icm}>V_{CC}/2, Vio can experience a permanent drift of few mV drift. The phenomenon is particularly worsen at low temperatures.

Figure 2. Supply current vs. supply voltage

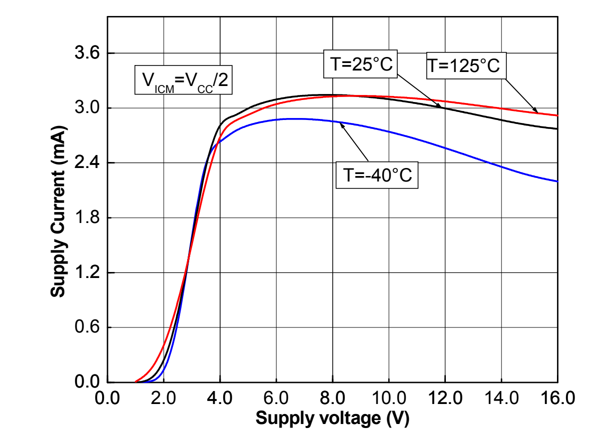


Figure 3. Distribution of input offset voltage at V_{CC} = 4.5 V

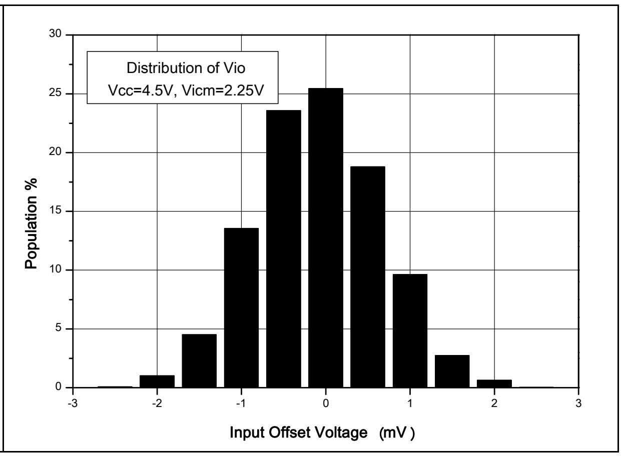


Figure 4. Distribution of input offset voltage at V_{CC} = 16 V

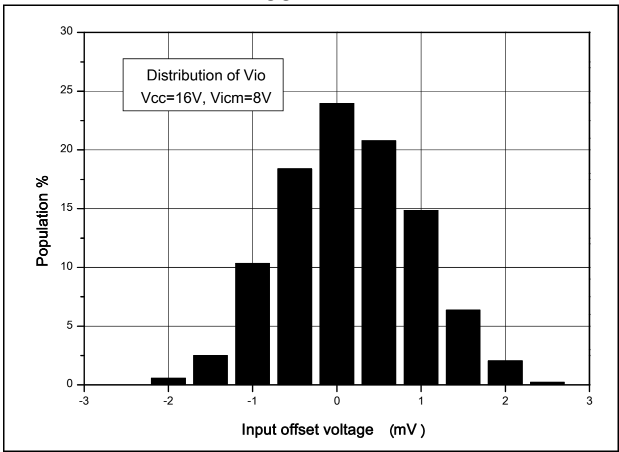


Figure 5. Input offset voltage vs. temperature at V_{CC} = 16 V

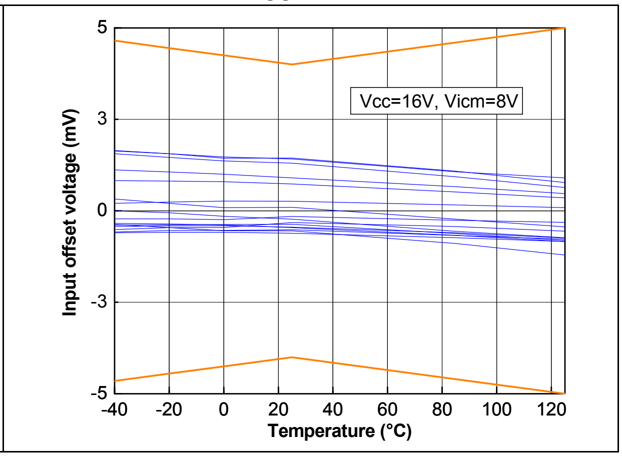


Figure 6. Distribution of input offset voltage drift over temperature

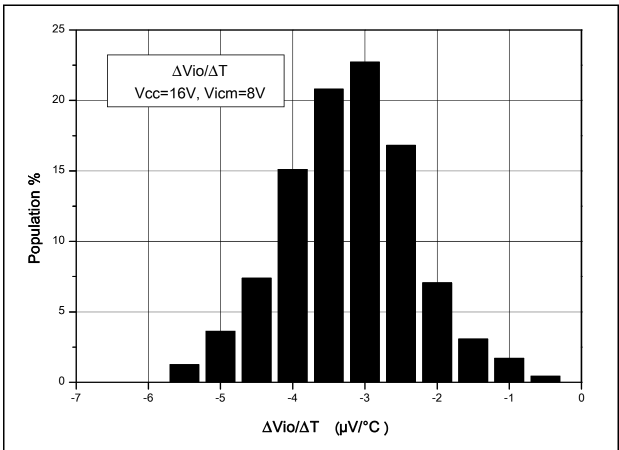


Figure 7. Input offset voltage vs. common mode voltage at V_{CC} = 4 V

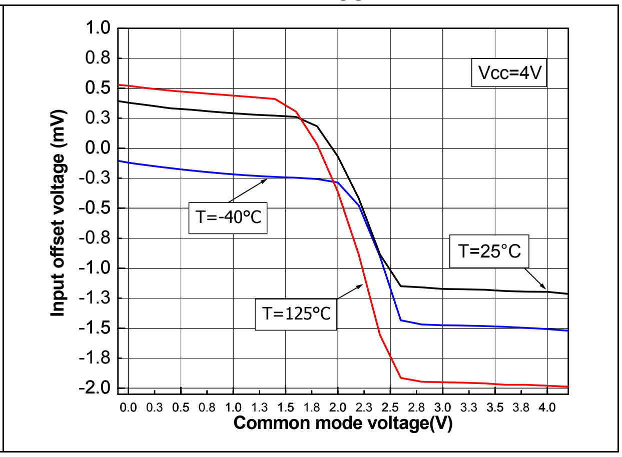


Figure 8. Input offset voltage vs. common mode voltage at V_{CC} = 16 V

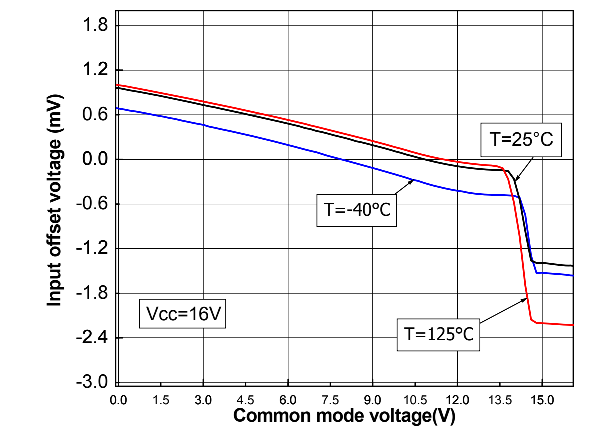


Figure 9. Output current vs. output voltage at V_{CC} = 4 V

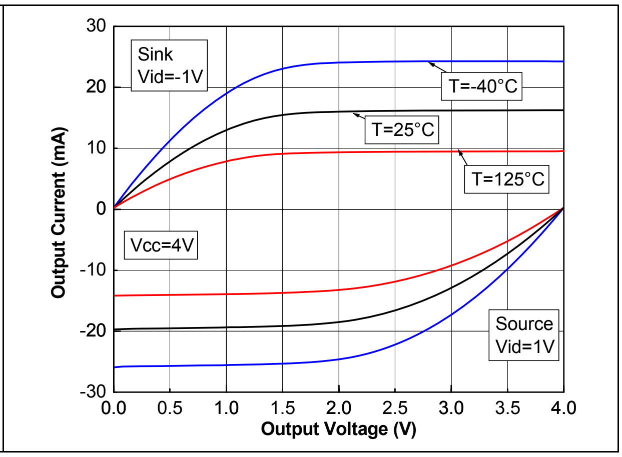


Figure 10. Output current vs. output voltage at V_{CC} = 10 V

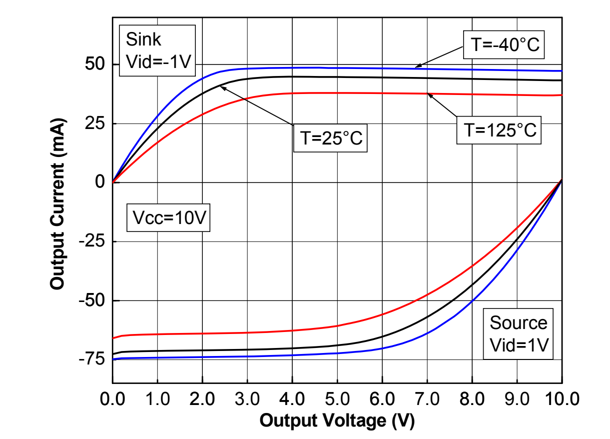


Figure 11. Output current vs. output voltage at V_{CC} = 16 V

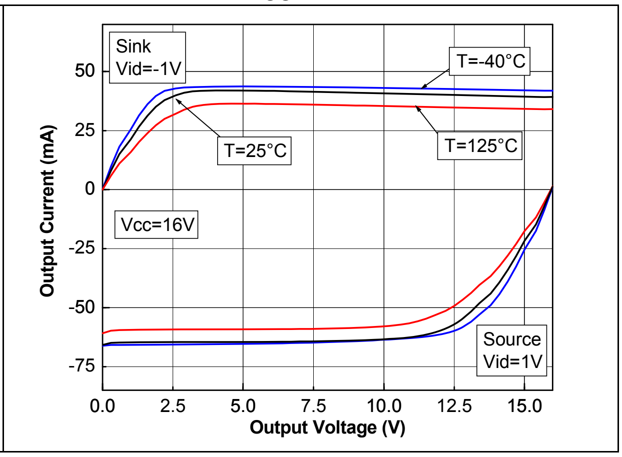


Figure 12. Output rail linearity

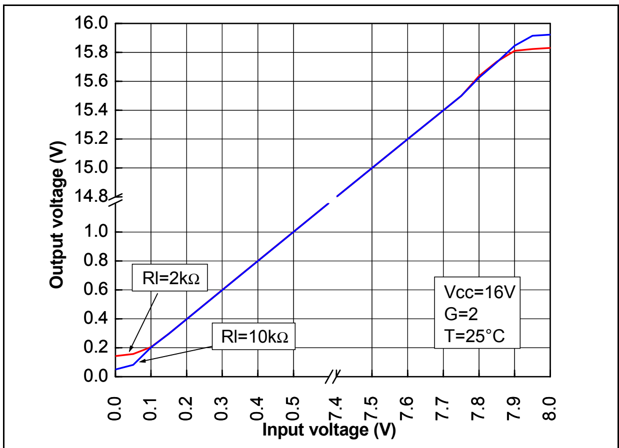


Figure 13. Open loop gain vs. frequency

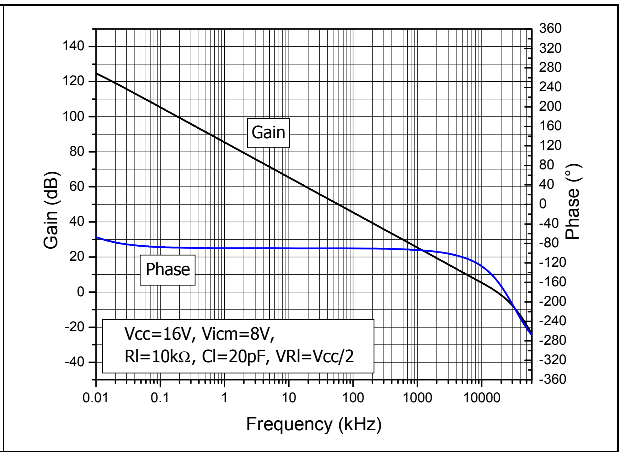


Figure 14. Bode diagram vs. temperature for V_{CC} = 4 V

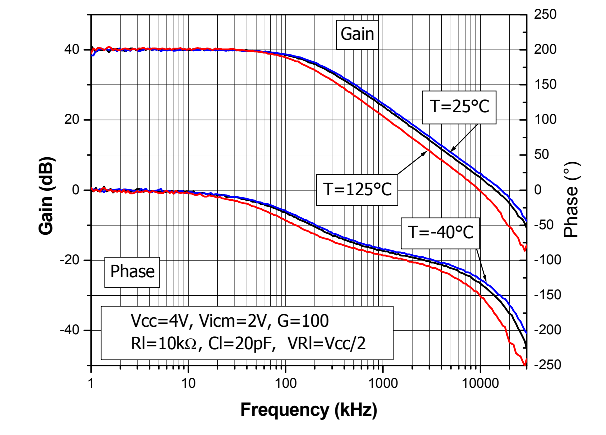


Figure 15. Bode diagram vs. temperature for V_{CC} = 10 V

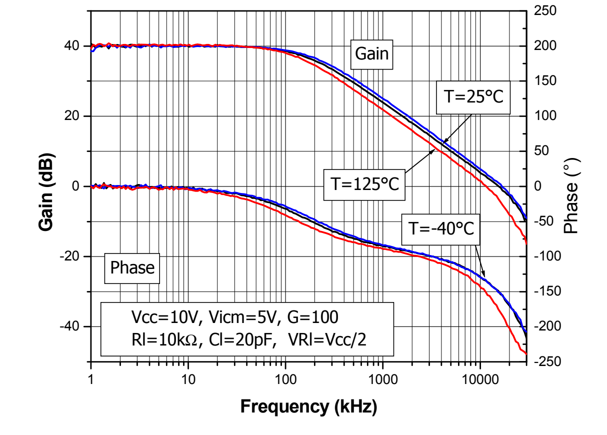


Figure 16. Bode diagram vs. temperature for V_{CC} = 16 V

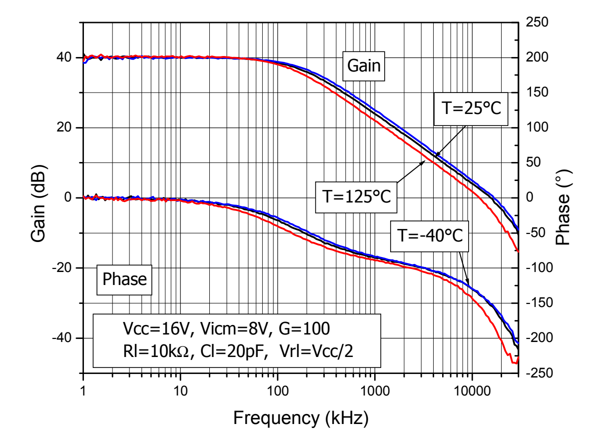


Figure 17. Bode diagram at V_{CC} = 16 V with low common mode voltage

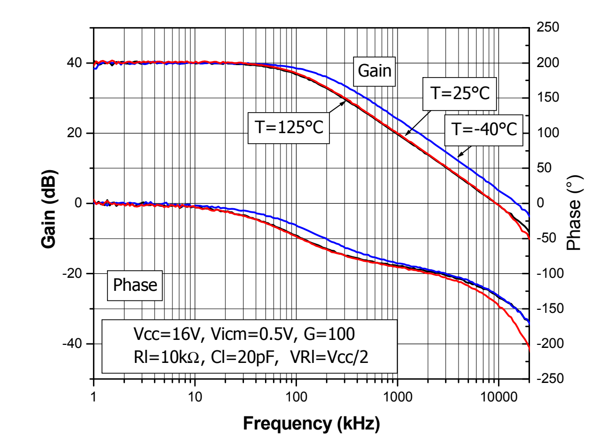


Figure 18. Bode diagram at V_{CC} = 16 V with high common mode voltage

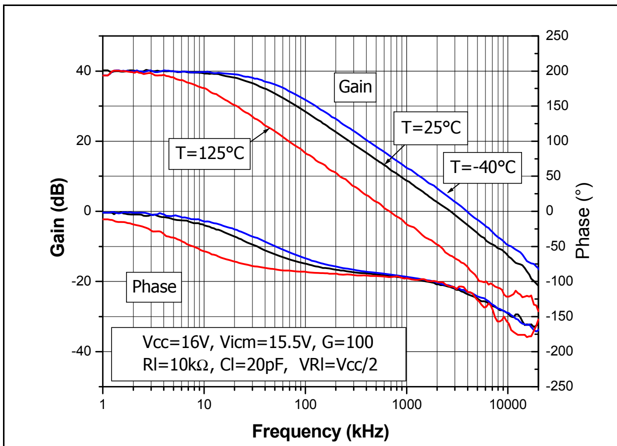


Figure 19. Bode diagram at V_{CC} = 16 V and R_L = 10 kΩ, C_L = 47 pF

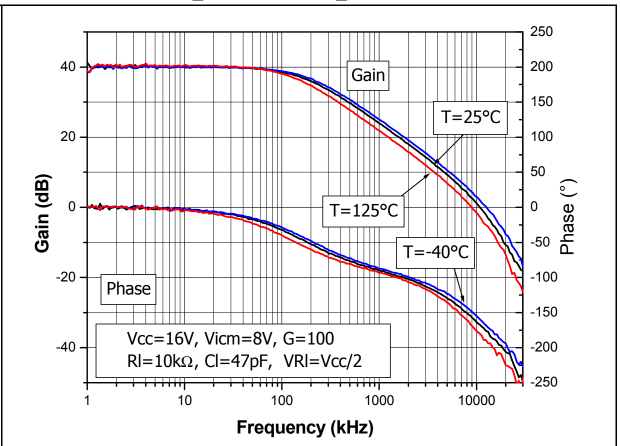


Figure 20. Bode diagram at V_{CC} = 16 V and R_L = 2 kΩ, C_L = 20 pF

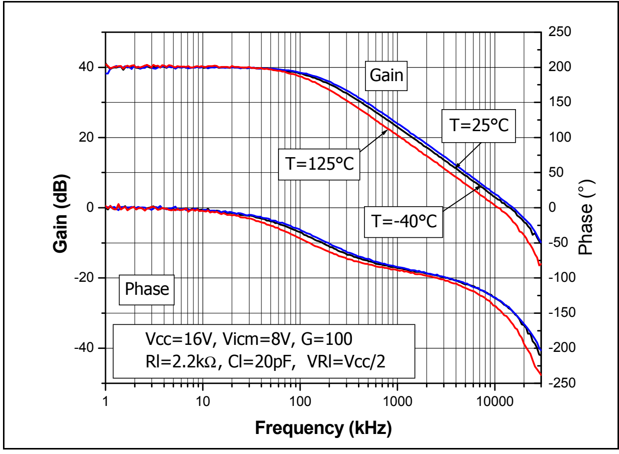


Figure 21. Slew rate vs. supply voltage and temperature

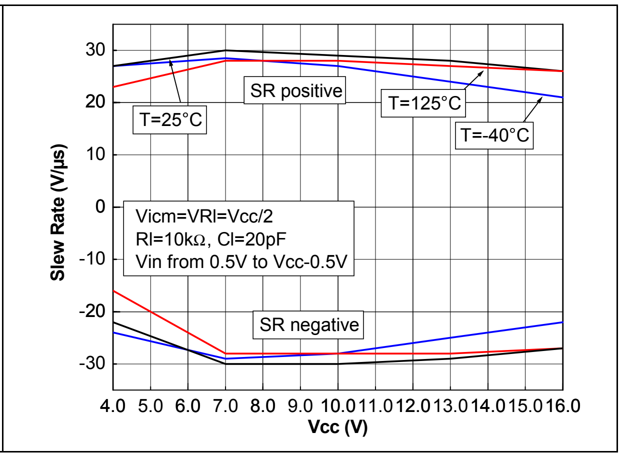


Figure 22. Small signal overshoot vs capacitive load without feedback capacitor Cf

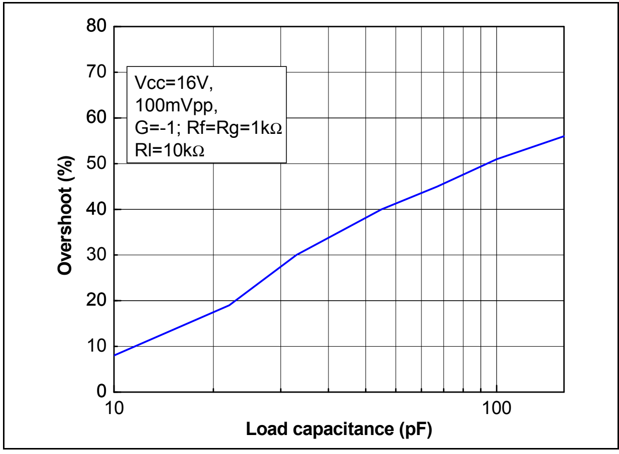


Figure 23. Small step response with G = +2

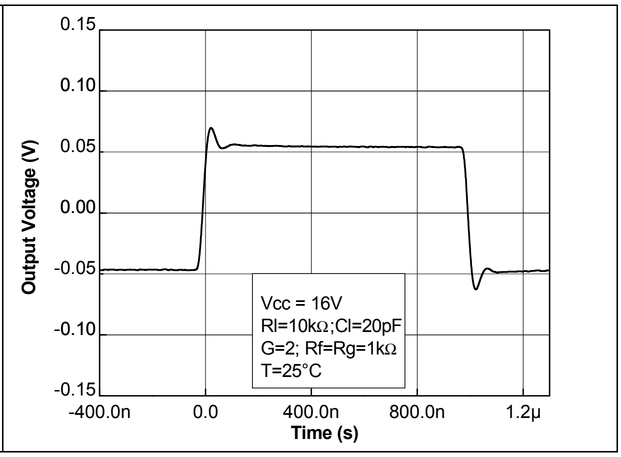


Figure 24. Small step response with feedback capacitor

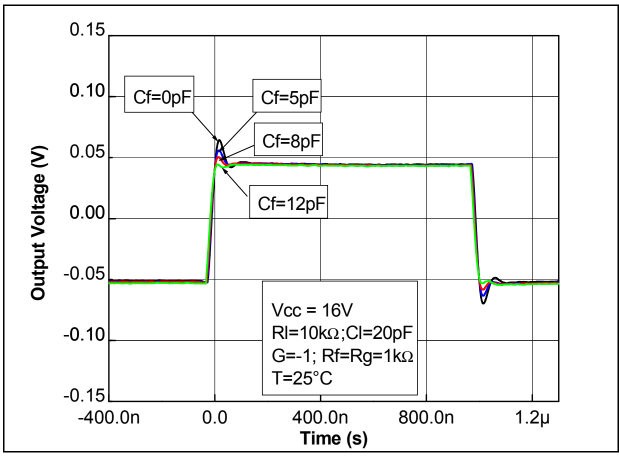


Figure 25. Large step response

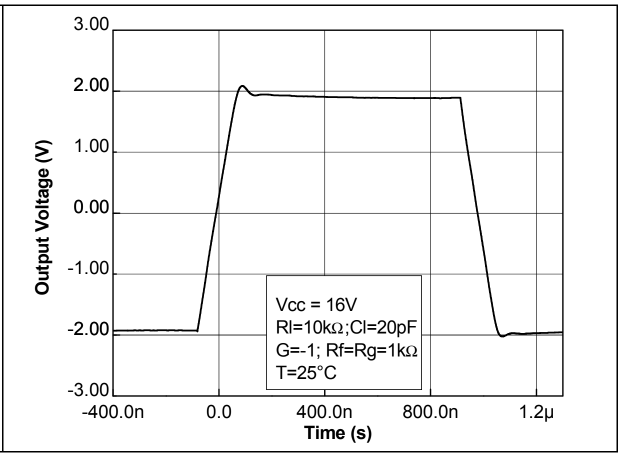


Figure 26. Desaturation time

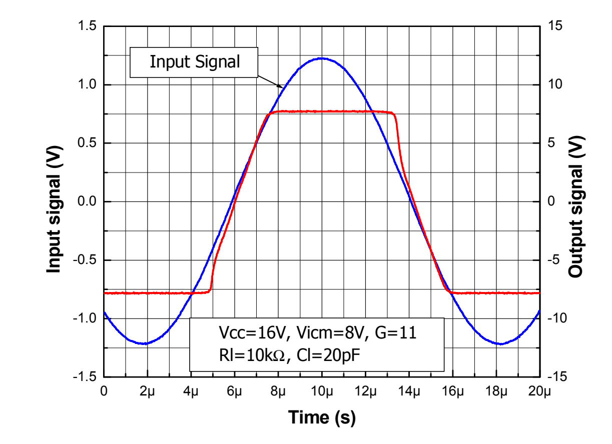


Figure 27. Peaking close loop with different Rl

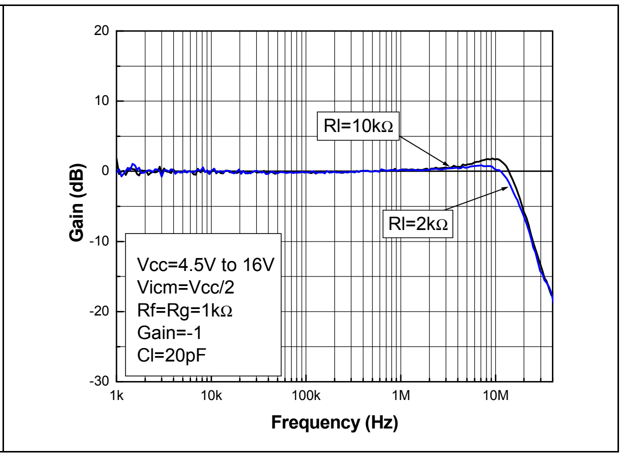


Figure 28. Output impedance vs frequency in close loop configuration

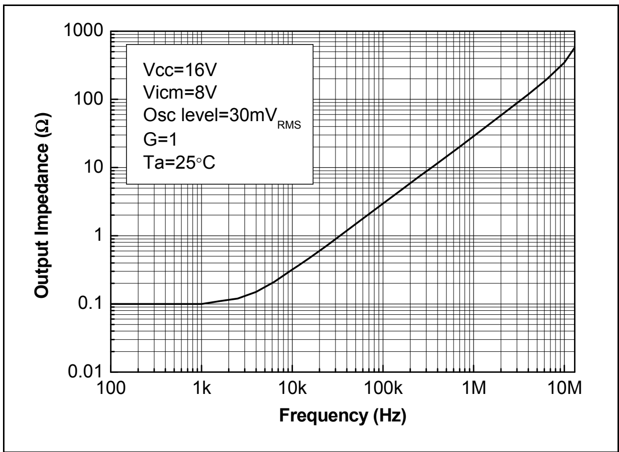


Figure 29. Noise vs. frequency with 16 V supply voltage

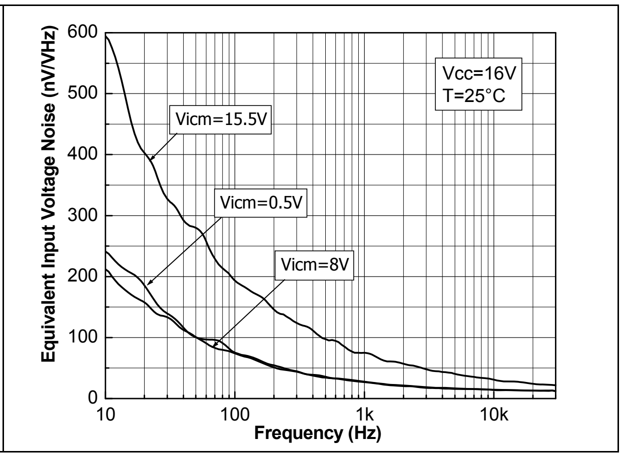


Figure 30. 0.1 to 10 Hz noise with 16 V supply voltage

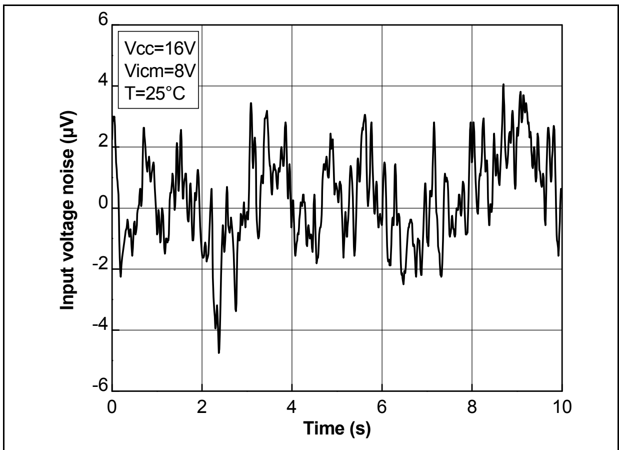


Figure 31. THD+N vs. frequency at V_{CC} = 16 V

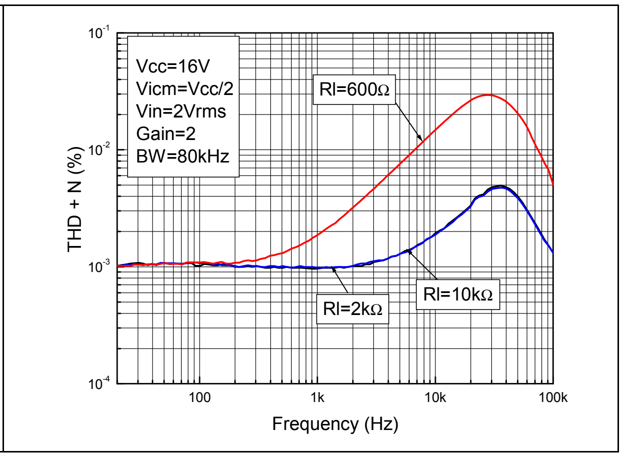


Figure 32. THD+N vs. output voltage at V_{CC} = 16 V

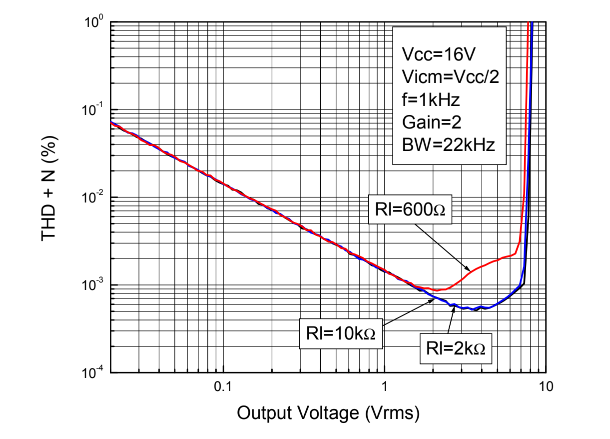


Figure 33. Power supply rejection ratio (PSRR) vs. frequency

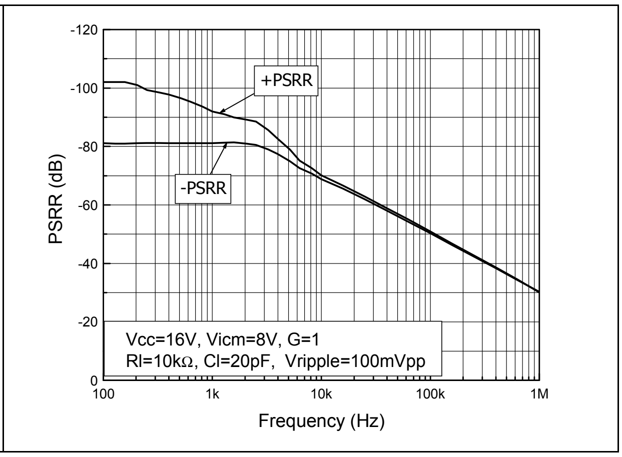
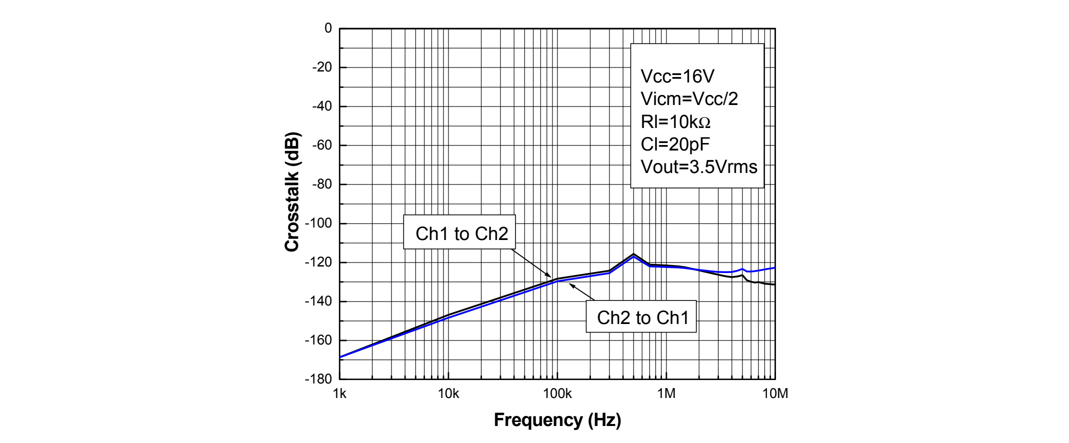


Figure 34. Crosstalk vs. frequency between operators on TSX9292 at V_{CC} = 16 V



4 Application information

4.1 Operating voltages

The TSX929x series of operation amplifiers can operate from 4 V to 16 V. Parameters are fully specified at 4.5 V, 10 V, and 16 V power supplies. However, parameters are very stable in the full V_{CC} range. Additionally, the main specifications are guaranteed in the extended temperature range of -40 to +125 °C.

4.2 Rail-to-rail input

The TSX9291 and TSX9292 are designed with two complementary PMOS and NMOS input differential pairs. The devices have a rail-to-rail input and the input common mode range is extended from (V_{CC-}) - 0.1 V to (V_{CC+}) + 0.1 V. However, the performance of these devices is clearly optimized for the PMOS differential pairs (which means from (V_{CC-}) - 0.1 V to (V_{CC+}) - 2 V).

Beyond (V_{CC+}) - 2 V, the operational amplifiers are still functional but with downgraded performances (see *Figure 19*). Performances are still suitable for a large number of applications requiring the rail-to-rail input feature.

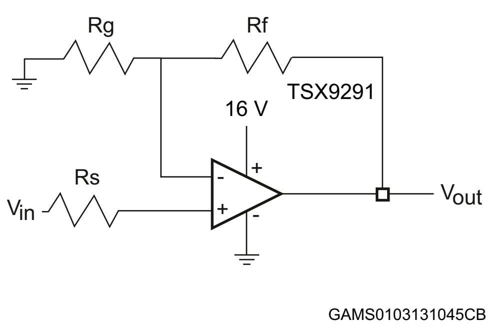
TSX9291 and TSX9292 are designed to prevent phase reversal.

4.3 Input pin voltage range

The TSX929x series has internal ESD diode protection on the inputs. These diodes are connected between the input and each supply rail to protect MOSFETs inputs from electrostatic discharges.

Thus, if the input pin voltage exceeds the power supply by 0.5 V, the ESD diodes become conductive and excessive current could flow through them. To prevent any permanent damage, this current must be limited to 10 mA. This can be done by adding a resistor, Rs, in series with the input pin (*Figure 35*). The Rs resistor value has to be calculated for a 10 mA current limitation on the input pins.

Figure 35. Limiting input current with a series resistor



4.4 Stability for gain = -1

TSX9291 and TSX9292 can be used in gain = -1 configuration (see *Figure 36*). However some precautions must be taken regarding the setting of the Rg and Rf resistors. Effectively, the input capacitance of the TSX929x series creates a pole with Rf and Rg. In high frequency, this pole decreases the phase margin and also causes gain peaking. This effect has a direct impact on the stability.

Figure 37 shows the peaking, depending on the values of the gain and feedback resistances.

Figure 36. Configuration for gain = -1

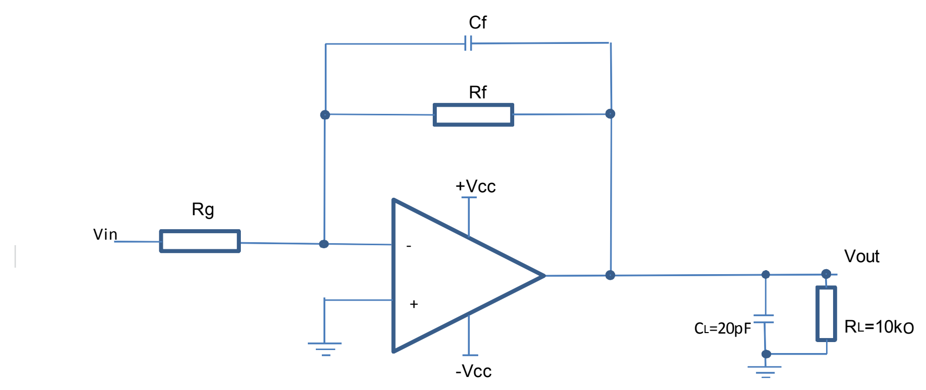
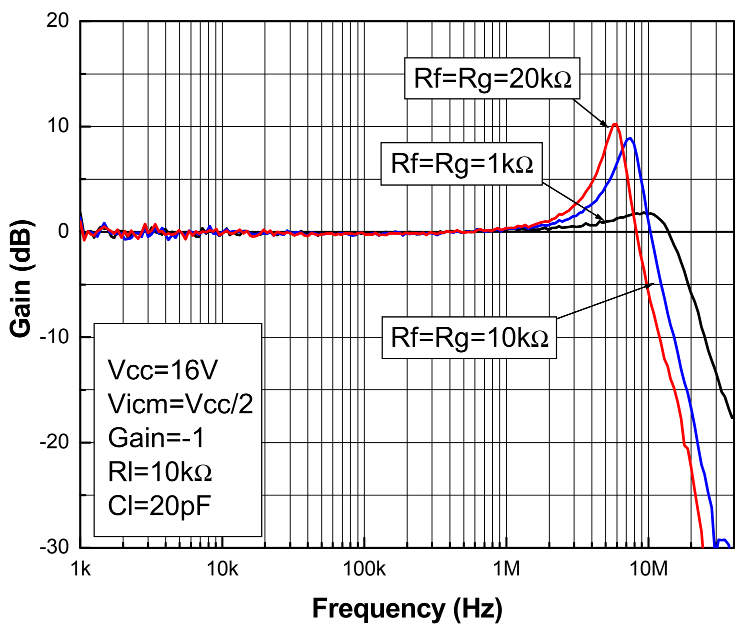


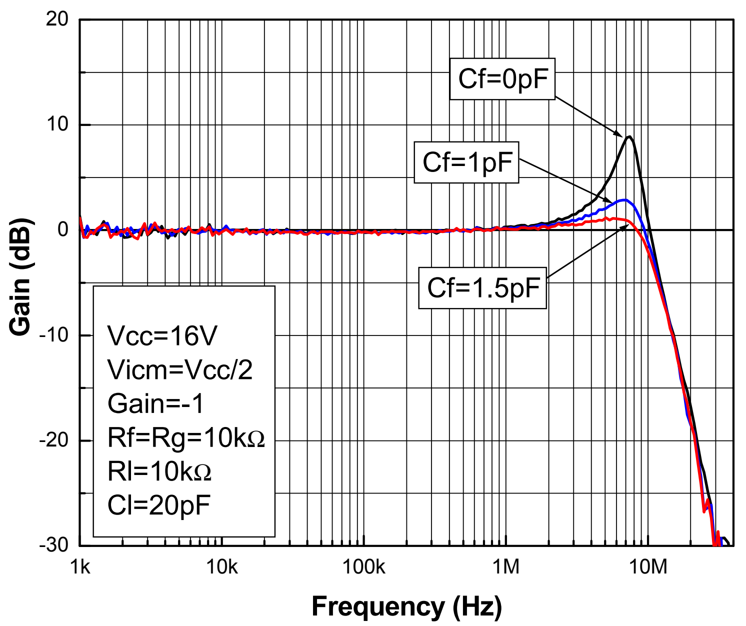
Figure 37. Close loop gain vs. frequency



Whenever possible, it is best to choose smaller feedback resistors. It is recommended to use 1 kΩ gain and feedback resistance (Rf and Rg) when gain = -1 is necessary. In the application, if a large value of Rf and Rg has to be used, a feedback capacitance can be added in parallel with Rf, to reduce or eliminate the gain peaking. Additionally, Cf helps to compensate the input capacitance and to increase stability.

Figure 38 shows how Cf reduces the gain peaking.

Figure 38. Close loop gain vs. frequency with capacitive compensation



4.5 Input offset voltage drift over temperature

The maximum input voltage drift over the temperature variation is defined as the offset variation related to offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift over temperature is computed using *Equation 1*.

Equation 1

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) - V_{io}(25°C)}{T - 25°C}\right|$$

with T = -40 °C and 125 °C.

The datasheet maximum value is guaranteed by a measurement on a representative sample size ensuring a C_{pk} (process capability index) greater than 2.

4.6 Long-term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using *Equation 2*.

Equation 2

$$A_{FV} = e^{\beta \cdot (V_S - V_U)}$$

Where:

A_{FV} is the voltage acceleration factor

β is the voltage acceleration constant in 1/V, constant technology parameter (β = 1)

V_S is the stress voltage used for the accelerated test

V_U is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined in *Equation 3*.

Equation 3

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S}\right)}$$

Where:

A_{FT} is the temperature acceleration factor

E_a is the activation energy of the technology based on the failure rate

k is the Boltzmann constant (8.6173×10^{-5} eV.K^{-1})

T_U is the temperature of the die when V_U is used (K)

T_S is the temperature of the die under temperature stress (K)

The final acceleration factor, A_F, is the multiplication of the voltage acceleration factor and the temperature acceleration factor (*Equation 4*).

Equation 4

$$A_F = A_{FT} \times A_{FV}$$

A_F is calculated using the temperature and voltage defined in the mission profile of the product. The A_F value can then be used in *Equation 5* to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

Equation 5

$$Months = A_F \times 1000\ h \times 12\ months / (24\ h \times 365.25\ days)$$

To evaluate the op-amp reliability, a follower stress condition is used where V_{CC} is defined as a function of the maximum operating voltage and the absolute maximum rating (as recommended by JEDEC rules).

The V_{io} drift (in µV) of the product after 1000 h of stress is tracked with parameters at different measurement conditions (see *Equation 6*).

Equation 6

$$V_{CC} = maxV_{op} \text{ with } V_{icm} = V_{CC} / 2$$

The long-term drift parameter (ΔV_{io}), estimating the reliability performance of the product, is obtained using the ratio of the V_{io} (input offset voltage value) drift over the square root of the calculated number of months (*Equation 7*).

Equation 7

$$\Delta V_{io} = \frac{V_{io} drift}{\sqrt{(months)}}$$

where V_{io} drift is the measured drift value in the specified test conditions after 1000 h stress duration.

4.7 Capacitive load

Driving a large capacitive load can cause stability issues. Increasing the load capacitance produces gain peaking in the frequency response, with overshooting and ringing in the step response. It is usually considered that with a gain peaking higher than 2.3 dB the op-amp might become unstable. Generally, the unity gain configuration is the worst configuration for stability and the ability to drive large capacitive loads. *Figure 39* shows the serial resistor (Riso) that must be added to the output, to make the system stable. *Figure 40* shows the test configuration for Riso.

Figure 39. Stability criteria with a serial resistor

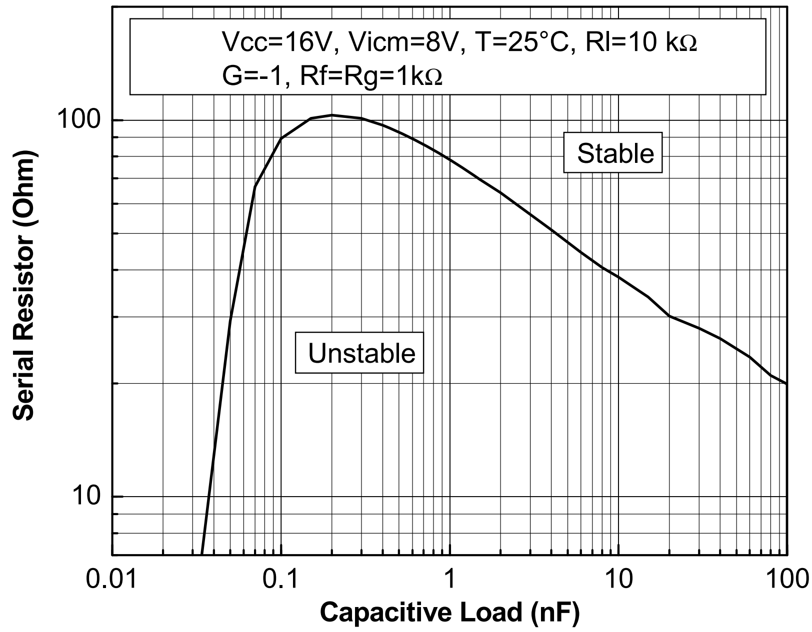
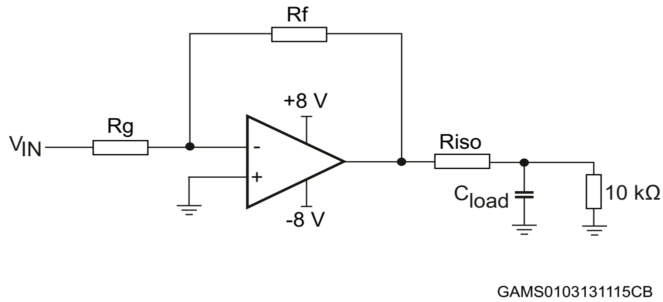


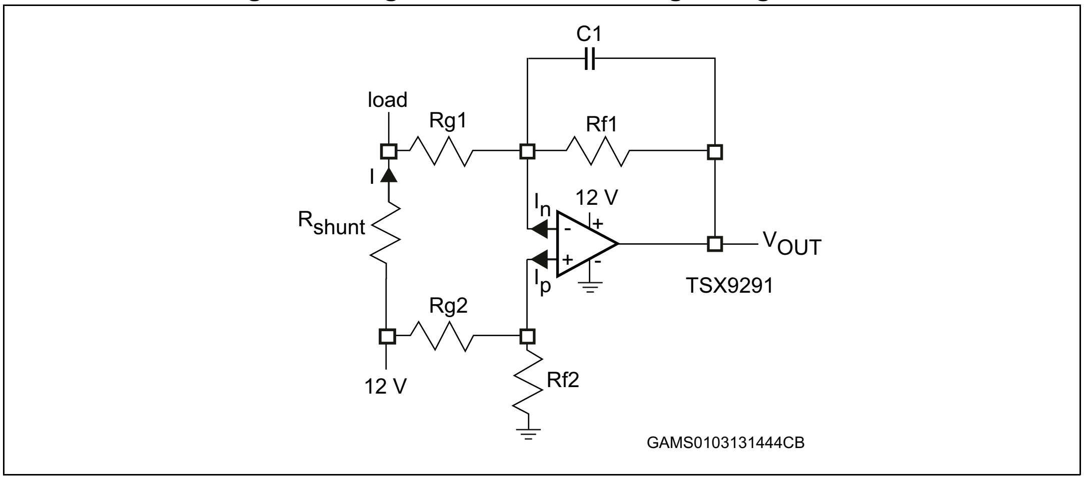
Figure 40. Test configuration for Riso



4.8 High side current sensing

TSX9291 and TSX9292 rail to rail input devices can be used to measure a small differential voltage on a high side shunt resistor and translate it into a ground referenced output voltage. The gain is fixed by external resistance.

Figure 41. High side current sensing configuration



V_{OUT} can be expressed as shown in *Equation 8*.

Equation 8

$$V_{out} = R_{shunt} \times I\left(1 - \frac{R_{g2}}{R_{g2} + R_{f2}}\right)\left(1 + \frac{R_{f1}}{R_{g1}}\right) + I_p\left(\frac{R_{g2}R_{f2}}{R_{g2} + R_{f2}}\right) \times \left(1 + \frac{R_{f1}}{R_{g1}}\right) - I_n x R_{f1} - V_{io}\left(1 + \frac{R_{f1}}{R_{g1}}\right)$$

Assuming that $R_{f2} = R_{f1} = R_f$ and $R_{g2} = R_{g1} = R_g$, *Equation 8* can be simplified as *Equation 9*.

Equation 9

$$V_{out} = R_{shunt} \times I\left(\frac{R_f}{R_g}\right) - V_{io}\left(1 + \frac{R_f}{R_g}\right) + R_f \times I_{io}$$

With the TSX929x series, the high side current measurement must be made by respecting the common mode voltage of the amplifier: (V_{CC-}) - 0.1V to (V_{CC+}) + 0.1V. If the application requires a higher common voltage, please refer to the TSC high side current sensing family.

4.9 High speed photodiode

The TSX929x series is an excellent choice for current to voltage (I-V) conversions. Due to the CMOS technology, the input bias currents are extremely low. Moreover, the low noise and high unity-gain bandwidth of TSX9291 TSX9292 make them particularly suitable for high-speed photodiode preamplifier applications.

The photodiode is considered as a capacitive current source. The input capacitance, C_{IN}, includes the parasitic input common mode capacitance, C_{CM} (3pF), and the input differential mode capacitance, C_{DIFF} (8pF). C_{IN} acts in parallel with the intrinsic capacitance of the photodiode, C_D. At higher frequencies, the capacitors affect the circuit response. The output capacitance of a current sensor has a strong effect on the stability of the op-amp feedback loop.

C_F stabilizes the gain and limits the transimpedance bandwidth. To ensure good stability and to obtain good noise performance, C_F can be set as shown in *Equation 10*.

Equation 10

$$C_F > \sqrt{\frac{C_{IN} + C_D}{2 \cdot \pi \cdot R_F \cdot F_{GBP}}} - C_{SMR}$$

where,

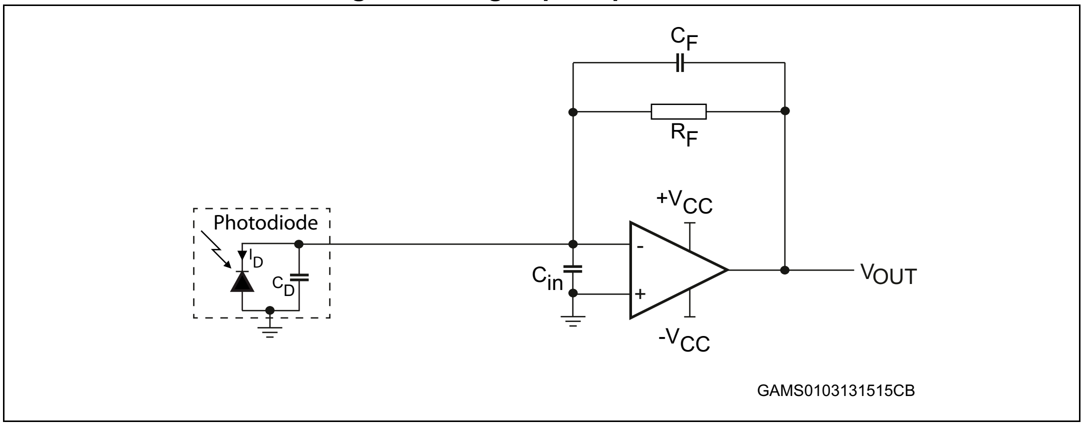
- $C_{IN} = C_{CM} + C_{DIFF} = 11$ pF
- C_{DIFF} is the differential input capacitance: 8 pF typical
- C_{CM} is the Common mode input capacitance: 3 pF typical
- C_D is the intrinsic capacitance of the photodiode
- C_{SMR} is the parasitic capacitance of the surface mount R_F resistor: 0.2 pF typical
- F_{GBP} is the gain bandwidth product: 10 MHz at 16 V

R_F fixes the gain as shown in *Equation 11*.

Equation 11

$$V_{OUT} = R_F \times I_D$$

Figure 42. High speed photodiode



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.