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2.5V Drive Nch MOSFET

1.5V Drive Pch MOSFET

TT8M2

●Structure

Silicon N-channel MOSFET/
Silicon P-channel MOSFET

●Features

- 1) Low on-state resistance.
- 2) Low voltage drive.
- 3) High power package.

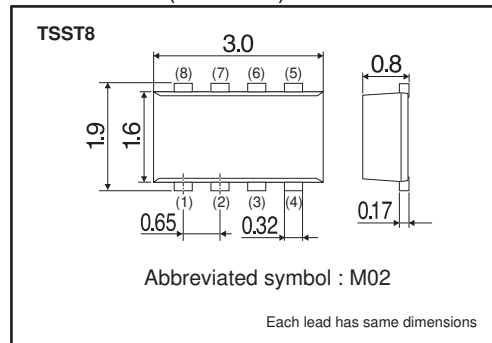
●Application

Switching

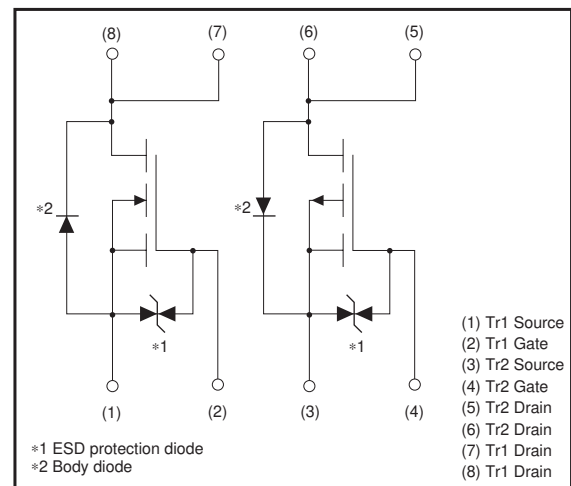
●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
TT8M2		○

●Dimensions (Unit : mm)



●Inner circuit



●Absolute maximum ratings (Ta=25°C)

<Tr1 : Nch>

Parameter	Symbol	Limits	Unit	
Drain-source voltage	V _{DSS}	30	V	
Gate-source voltage	V _{GSS}	±12	V	
Drain current	Continuous	I _D	±2.5	A
	Pulsed	I _{DP} *1	±10	A
Source current (Body diode)	Continuous	I _S	0.8	A
	Pulsed	I _{SP} *1	10	A

*1 Pw≤10μs, Duty cycle≤1%

<Tr2 : Pch>

Parameter	Symbol	Limits	Unit	
Drain-source voltage	V_{DSS}	-20	V	
Gate-source voltage	V_{GSS}	± 10	V	
Drain current	Continuous	I_D	± 2.5	A
	Pulsed	I_{DP} *1	± 10	A
Source current (Body diode)	Continuous	I_S	-0.8	A
	Pulsed	I_{SP} *1	-10	A

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

<Tr1 AND Tr2>

Parameter	Symbol	Limits	Unit
Total power dissipation	P_D *2	1.25	W / TOTAL
		1.0	W / ELEMENT
Channel temperature	T_{ch}	150	$^{\circ}C$
Range of Storage temperature	T_{stg}	-55 to +150	$^{\circ}C$

*2 Mounted on a ceramic board

●Electrical characteristics (Ta=25°C)

< Characteristics for the Tr1(Nch).>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	± 10	μA	$V_{GS} = \pm 12V$, $V_{DS} = 0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	$I_D = 1mA$, $V_{GS} = 0V$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS} = 30V$, $V_{GS} = 0V$
Gate threshold voltage	$V_{GS(th)}$	0.5	-	1.5	V	$V_{DS} = 10V$, $I_D = 1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	-	65	90	$m\Omega$	$I_D = 2.5A$, $V_{GS} = 4.5V$
		-	70	95	$m\Omega$	$I_D = 2.5A$, $V_{GS} = 4V$
		-	95	130	$m\Omega$	$I_D = 2.5A$, $V_{GS} = 2.5V$
Forward transfer admittance	$ Y_{fs} $ *	2.2	-	-	S	$V_{DS} = 10V$, $I_D = 2.5A$
Input capacitance	C_{iss}	-	180	-	pF	$V_{DS} = 10V$
Output capacitance	C_{oss}	-	60	-	pF	$V_{GS} = 0V$
Reverse transfer capacitance	C_{rss}	-	35	-	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}$ *	-	7	-	ns	$V_{DD} \doteq 15V$
Rise time	t_r *	-	30	-	ns	$I_D = 1.2A$
Turn-off delay time	$t_{d(off)}$ *	-	20	-	ns	$V_{GS} = 4.5V$
Fall time	t_f *	-	20	-	ns	$R_L \doteq 12.5\Omega$
Total gate charge	Q_g *	-	3.2	-	nC	$V_{DD} \doteq 15V$, $I_D = 2.5A$
Gate-source charge	Q_{gs} *	-	0.9	-	nC	$V_{GS} = 4.5V$
Gate-drain charge	Q_{gd} *	-	0.4	-	nC	$R_L \doteq 6\Omega$, $R_G = 10\Omega$

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	-	-	1.2	V	$I_S = 2.5A$, $V_{GS} = 0V$

*Pulsed

●Electrical characteristics (Ta=25°C)

< Characteristics for the Tr2(Pch).>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	± 10	μA	$V_{GS}=\pm 10V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	–20	–	–	V	$I_D = -1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	–	–	–1	μA	$V_{DS} = -20V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	–0.3	–	–1.0	V	$V_{DS} = -10V, I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	–	49	68	m Ω	$I_D = -2.5A, V_{GS} = -4.5V$
		–	68	95	m Ω	$I_D = -1.2A, V_{GS} = -2.5V$
		–	100	150	m Ω	$I_D = -1.2A, V_{GS} = -1.8V$
		–	140	280	m Ω	$I_D = -0.5A, V_{GS} = -1.5V$
Forward transfer admittance	$ Y_{fs} $ *	2.5	–	–	S	$V_{DS} = -10V, I_D = -2.5A$
Input capacitance	C_{iss}	–	1270	–	pF	$V_{DS} = -10V$
Output capacitance	C_{oss}	–	100	–	pF	$V_{GS} = 0V$
Reverse transfer capacitance	C_{rss}	–	90	–	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}$ *	–	9	–	ns	$V_{DD} \doteq -10V$
Rise time	t_r *	–	30	–	ns	$I_D = -1.2A$
Turn-off delay time	$t_{d(off)}$ *	–	120	–	ns	$V_{GS} = -4.5V$
Fall time	t_f *	–	85	–	ns	$R_L \doteq 8.3\Omega$
Total gate charge	Q_g *	–	12	–	nC	$V_{DD} \doteq -10V, I_D = -2.5A$
Gate-source charge	Q_{gs} *	–	2.5	–	nC	$V_{GS} = -4.5V$
Gate-drain charge	Q_{gd} *	–	2.0	–	nC	$R_L \doteq 4\Omega, R_G = 10\Omega$

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	–	–	–1.2	V	$I_S = -2.5A, V_{GS} = 0V$

*Pulsed

●Electrical characteristics curves
<Nch>

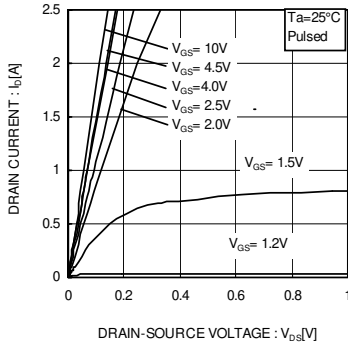


Fig.1 Typical Output Characteristics(I)

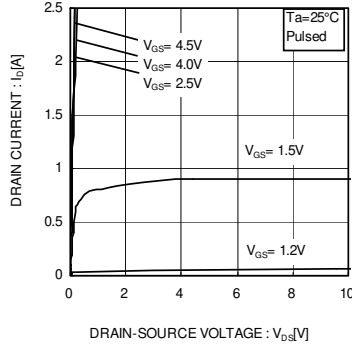


Fig.2 Typical Output Characteristics(II)

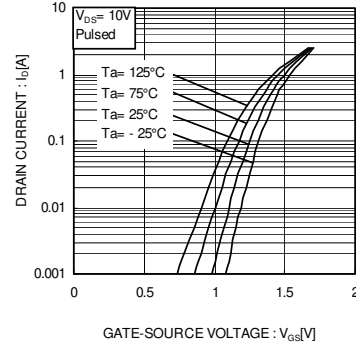


Fig.3 Typical Transfer Characteristics

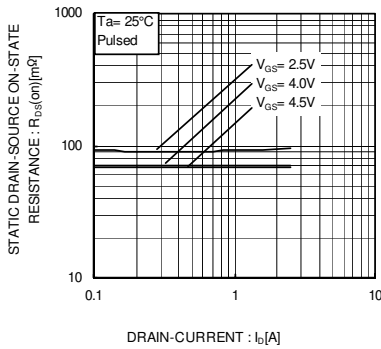


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

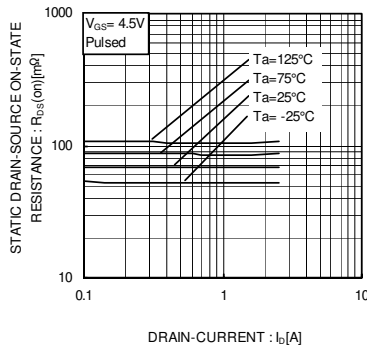


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

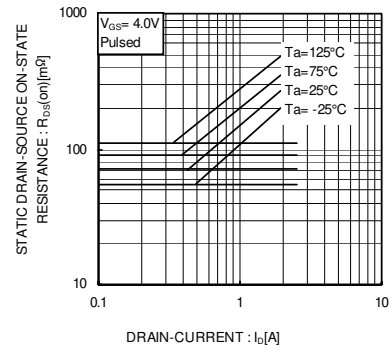


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

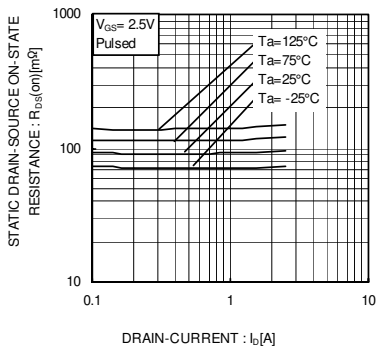


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

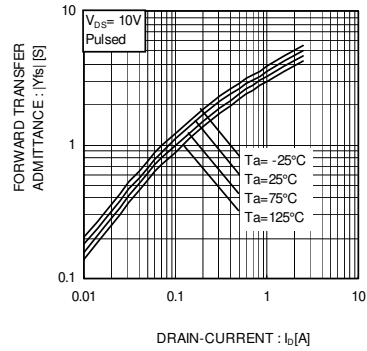


Fig.8 Forward Transfer Admittance vs. Drain Current

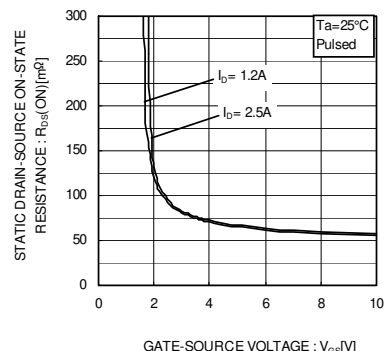


Fig.9 Static Drain-Source On-State Resistance vs. Gate Source Voltage

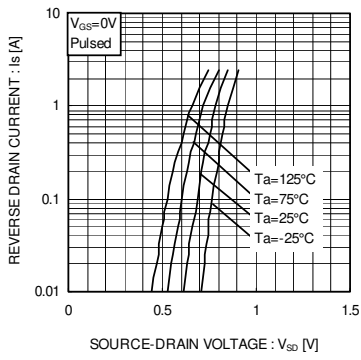


Fig.10 Reverse Drain Current vs. Source-Drain Voltage

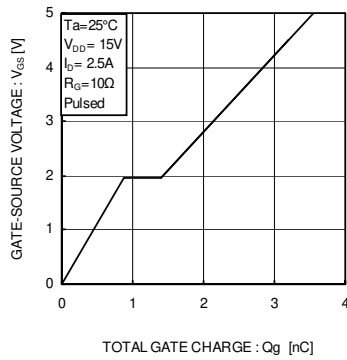


Fig.11 Dynamic Input Characteristics

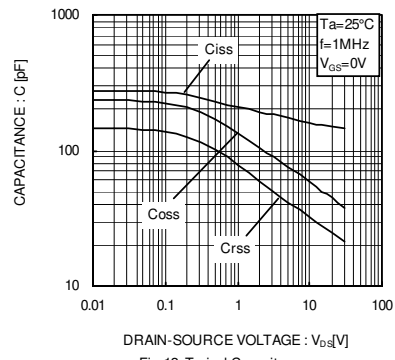


Fig.12 Typical Capacitance vs. Drain-Source Voltage

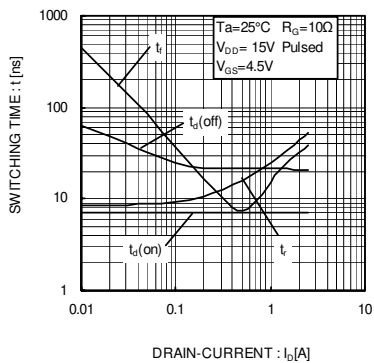


Fig.13 Switching Characteristics

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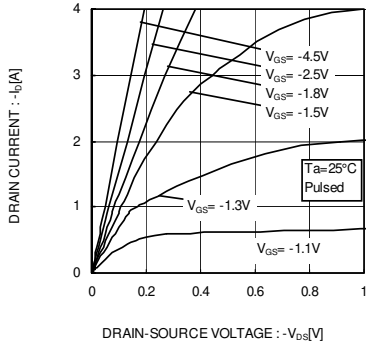


Fig.1 Typical Output Characteristics (I)

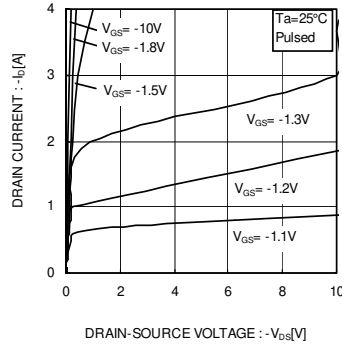


Fig.2 Typical Output Characteristics (II)

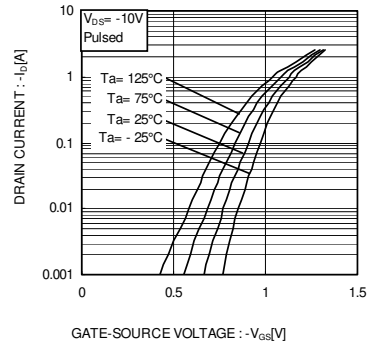


Fig.3 Typical Transfer Characteristics

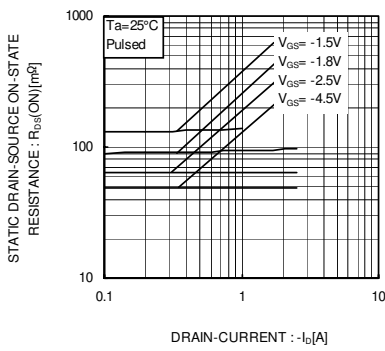


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (I)

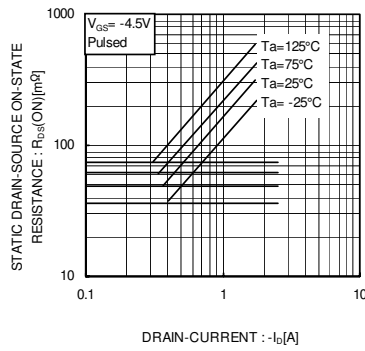


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current (II)

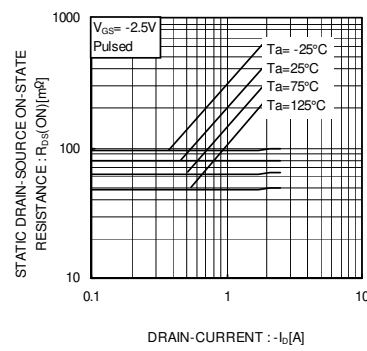


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current (III)

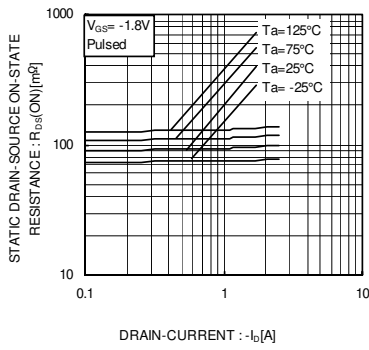


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

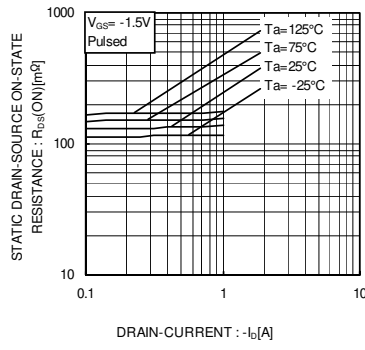


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(IV)

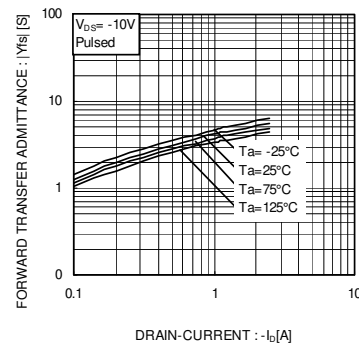
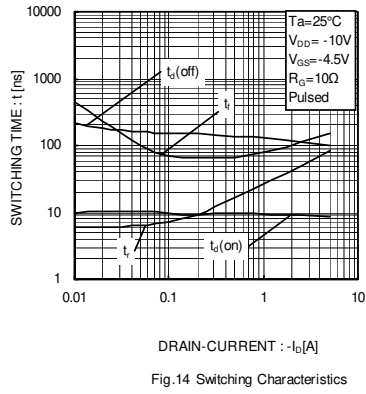
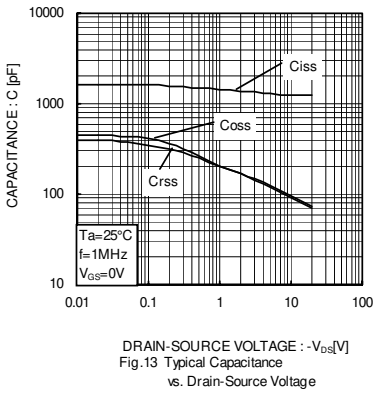
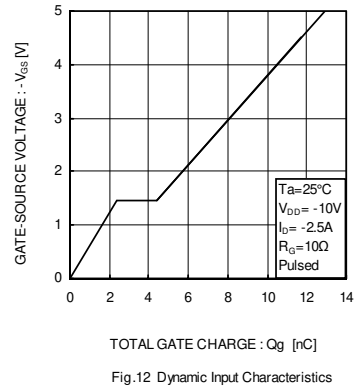
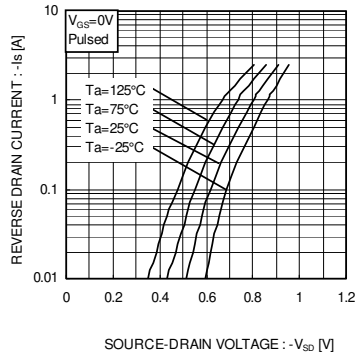
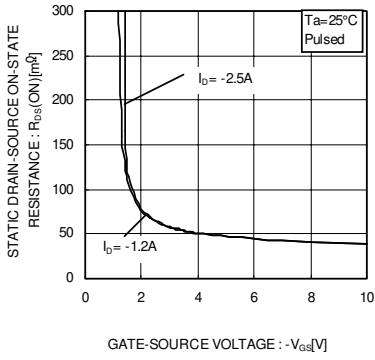


Fig.9 Forward Transfer Admittance vs. Drain Current



●Measurement circuits

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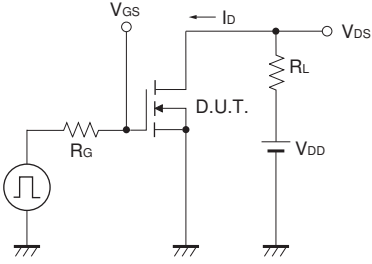


Fig.1-1 Switching Time Measurement Circuit

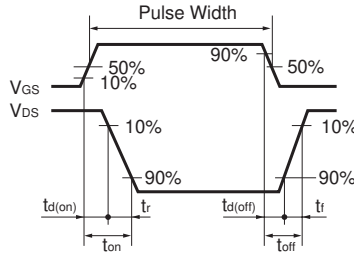


Fig.1-2 Switching Waveforms

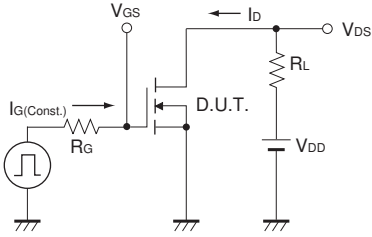


Fig.2-1 Gate charge measurement circuit

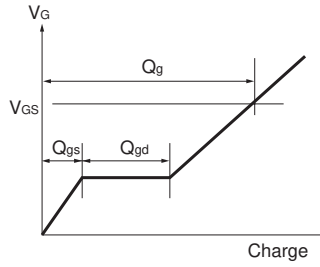


Fig.2-2 Gate Charge Waveform

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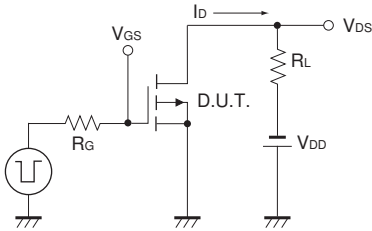


Fig.3-1 Switching time measurement circuit

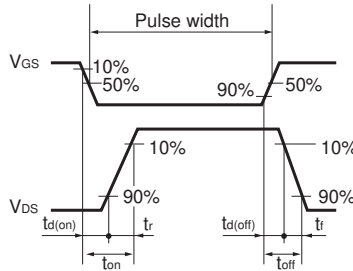


Fig.3-2 Switching waveforms

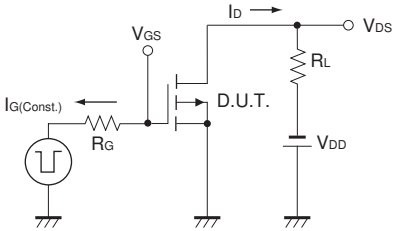


Fig.4-1 Gate charge measurement circuit

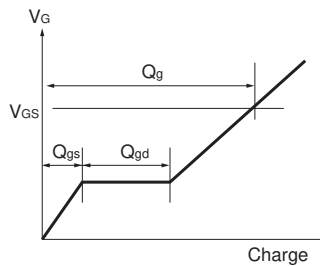


Fig.4-2 Gate charge waveform

●Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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