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1.5V Drive Nch + Pch MOSFET

TT8M3

●Structure

Silicon N-channel MOSFET/
Silicon P-channel MOSFET

●Features

- 1) Low On-state resistance.
- 2) Low voltage drive(1.5V).
- 3) High power package.

●Application

Switching

●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
TT8M3		○

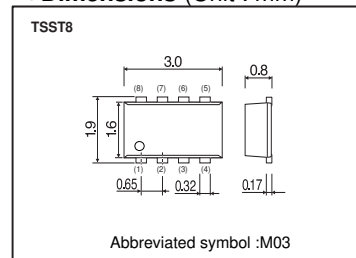
●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits		Unit
		Tr1 : N-ch	Tr2 : P-ch	
Drain-source voltage	V_{DSS}	20	-20	V
Gate-source voltage	V_{GSS}	± 10	± 10	V
Drain current	Continuous	I_D	± 2.5	A
	Pulsed	I_{DP}^{*1}	± 10	A
Source current (Body Diode)	Continuous	I_S	0.8	A
	Pulsed	I_{SP}^{*1}	10	A
Power dissipation	P_D^{*2}	1.25		W / TOTAL
		1.0		W / ELEMENT
Channel temperature	Tch	150		°C
Range of storage temperature	Tstg	-55 to +150		°C

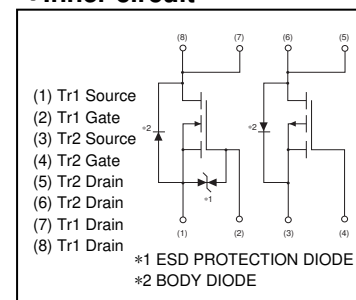
*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

*2 Mounted on a ceramic board.

●Dimensions (Unit : mm)



●Inner circuit



●Electrical characteristics (Ta = 25°C)

<Tr1(Nch)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	±10	μA	$V_{GS}=\pm 10V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	20	-	-	V	$I_D=1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=20V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	0.3	-	1.0	V	$V_{DS}=10V, I_D=1mA$
Static drain-source on-state resistance	$R_{DS(on)}^*$	-	52	72	mΩ	$I_D=2.5A, V_{GS}=4.5V$
		-	65	90		$I_D=2.5A, V_{GS}=2.5V$
		-	85	120		$I_D=1.2A, V_{GS}=1.8V$
		-	100	140		$I_D=0.5A, V_{GS}=1.5V$
Forward transfer admittance	$ Y_{fs} ^*$	2.7	-	-	S	$V_{DS}=10V, I_D=2.5A$
Input capacitance	C_{iss}	-	260	-	pF	$V_{DS}=10V$
Output capacitance	C_{oss}	-	65	-	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	-	35	-	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}^*$	-	9	-	ns	$I_D=1.2A, V_{DD}=10V$
Rise time	t_r^*	-	17	-	ns	$V_{GS}=4.5V$
Turn-off delay time	$t_{d(off)}^*$	-	28	-	ns	$R_L=8.3\Omega$
Fall time	t_f^*	-	17	-	ns	$R_G=10\Omega$
Total gate charge	Q_g^*	-	3.6	-	nC	$I_D=2.5A, V_{DD}=10V$
Gate-source charge	Q_{gs}^*	-	0.7	-	nC	$V_{GS}=4.5V, R_L=4\Omega$
Gate-drain charge	Q_{gd}^*	-	0.6	-	nC	$R_G=10\Omega$

*Pulsed

●Body diode characteristics (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}^*	-	-	1.2	V	$I_s=2.5A, V_{GS}=0V$

*Pulsed

● **Electrical characteristics** (Ta = 25°C)

<Tr2(Pch)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	±100	μA	$V_{GS}=\pm 10V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	-20	-	-	V	$I_D=-1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}		-	-1	μA	$V_{DS}=-20V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	-0.3	-	-1.0	V	$V_{DS}=-10V, I_D=-1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	-	80	105	mΩ	$I_D=-2.4A, V_{GS}=-4.5V$
		-	105	140		$I_D=-1.2A, V_{GS}=-2.5V$
		-	150	225		$I_D=-1.2A, V_{GS}=-1.8V$
		-	180	360		$I_D=-0.5A, V_{GS}=-1.5V$
Forward transfer admittance	$ Y_{fs} ^*$	2.4	-	-	S	$I_D=-2.4A, V_{DS}=-10V$
Input capacitance	C_{iss}	-	850	-	pF	$V_{DS}=-10V$
Output capacitance	C_{oss}	-	60	-	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rfs}	-	50	-	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	-	9	-	ns	$I_D=-1.2A, V_{DD} \approx -10V$
Rise time	t_r *	-	25	-	ns	$V_{GS}=-4.5V$
Turn-off delay time	$t_{d(off)}$ *	-	55	-	ns	$R_L=8.3\Omega$
Fall time	t_f *	-	45	-	ns	$R_G=10\Omega$
Total gate charge	Q_g *	-	6.7	-	nC	$I_D=-2.4A$
Gate-source charge	Q_{gs} *	-	1.7	-	nC	$V_{DD} \approx -10V$
Gate-drain charge	Q_{gd} *	-	0.6	-	nC	$V_{GS}=-4.5V$

*Pulsed

● **Body diode characteristics** (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD} *	-	-	-1.2	V	$I_s=-2.4A, V_{GS}=0V$

*Pulsed

●Electrical characteristic curves<Tr1(Nch)>

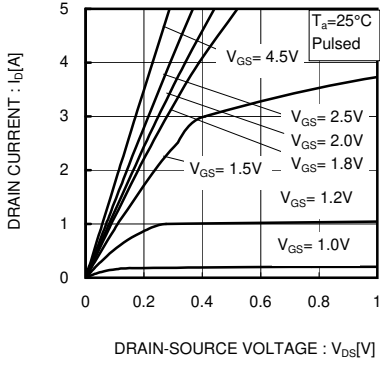


Fig.1 Typical Output Characteristics(I)

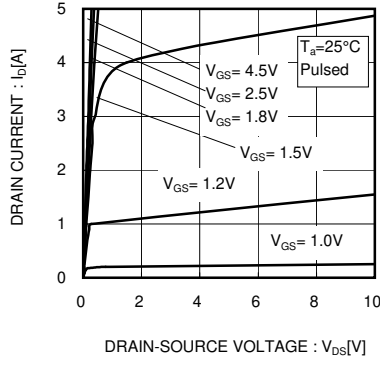


Fig.2 Typical Output Characteristics(II)

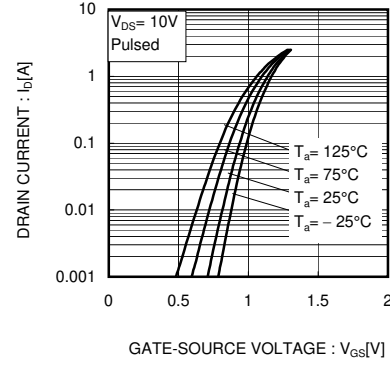


Fig.3 Typical Transfer Characteristics

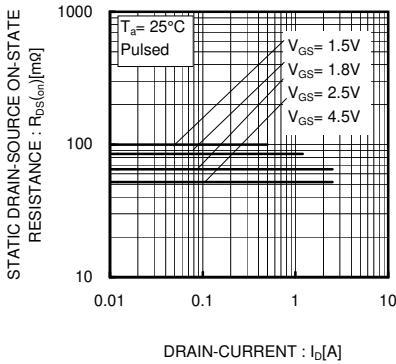


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

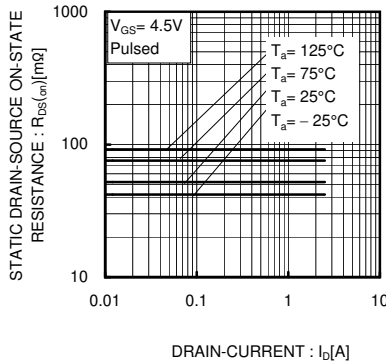


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

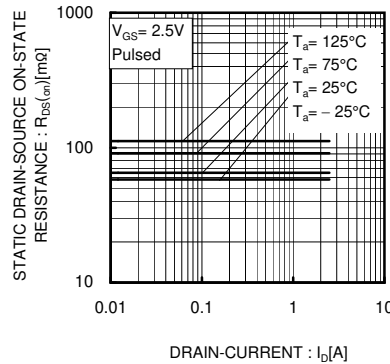


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

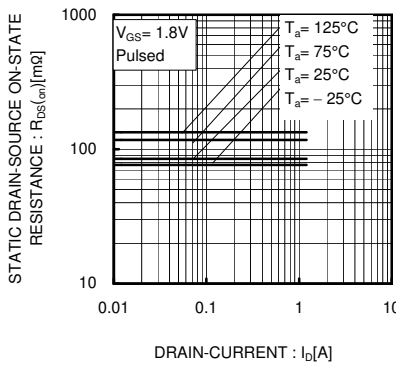


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

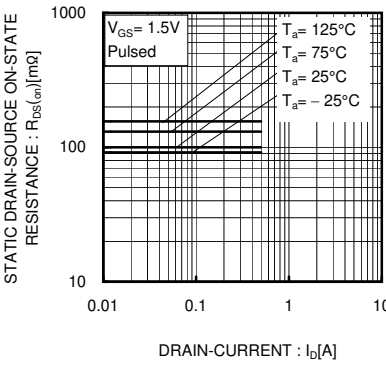


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(V)

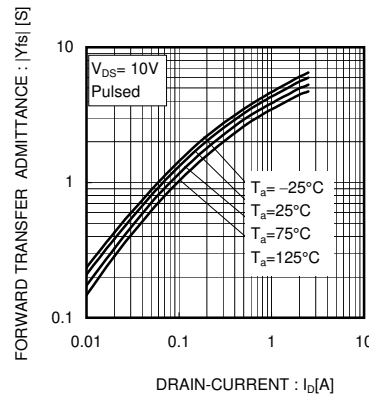


Fig.9 Forward Transfer Admittance vs. Drain Current

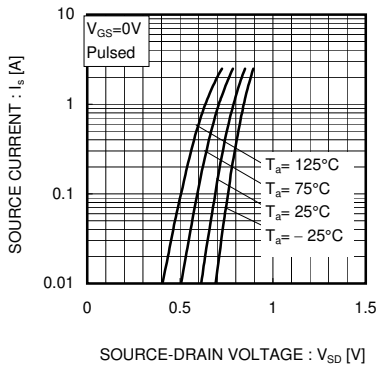


Fig.10 Reverse Drain Current vs. Source-Drain Voltage

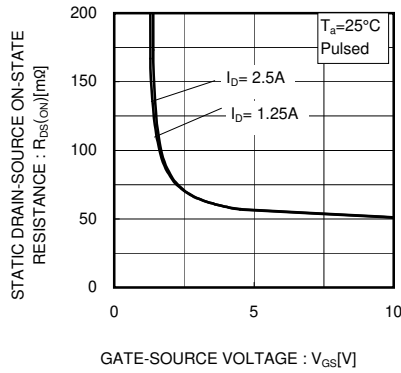


Fig.11 Static Drain-Source On-State Resistance vs. Gate Source Voltage

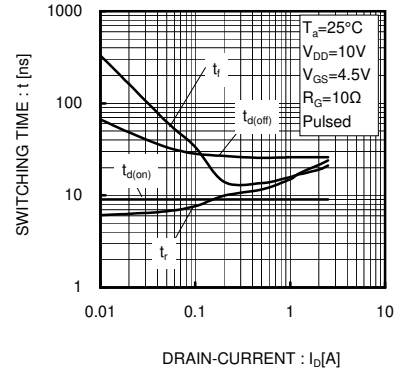


Fig.12 Switching Characteristics

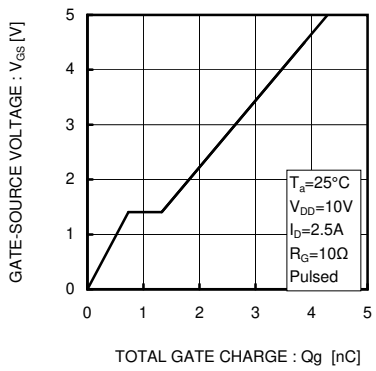


Fig.13 Dynamic Input Characteristics

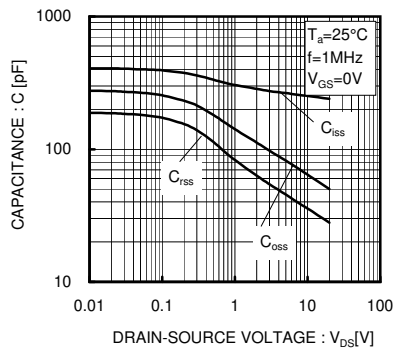
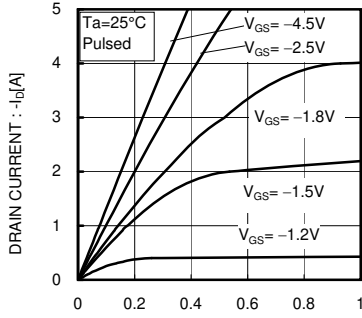
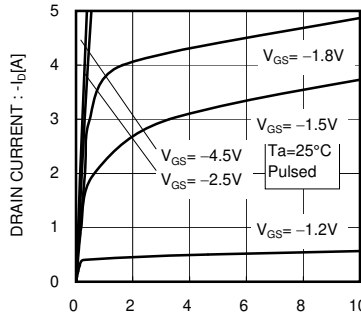


Fig.14 Typical Capacitance vs. Drain-Source Voltage

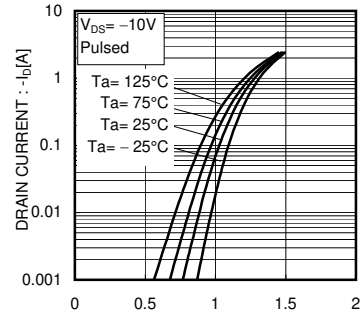
●Electrical characteristic curves<Tr2(Pch)>



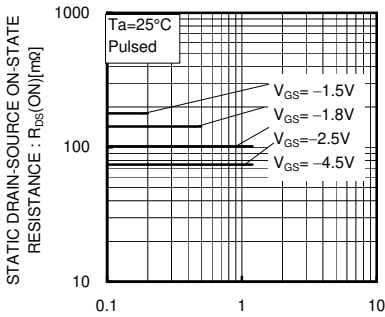
DRAIN-SOURCE VOLTAGE : $-V_{DS}$ [V]
Fig.1 Typical output characteristics(I)



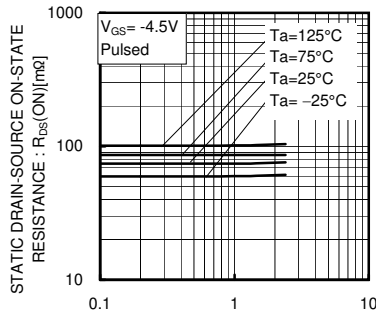
DRAIN-SOURCE VOLTAGE : $-V_{DS}$ [V]
Fig.2 Typical output characteristics(II)



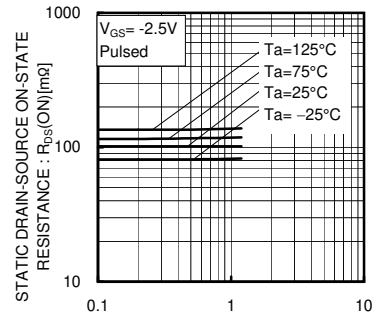
GATE-SOURCE VOLTAGE : $-V_{GS}$ [V]
Fig.3 Typical Transfer Characteristics



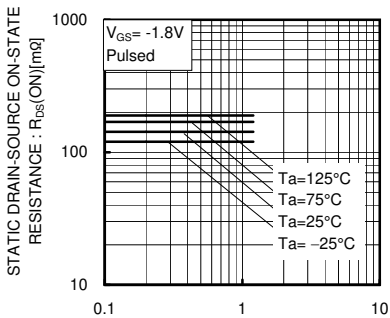
DRAIN-CURRENT : $-I_D$ [A]
Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)



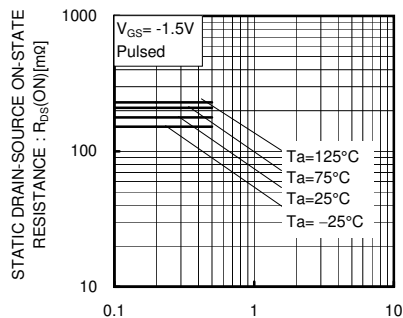
DRAIN-CURRENT : $-I_D$ [A]
Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)



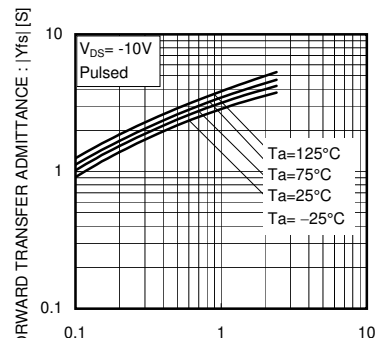
DRAIN-CURRENT : $-I_D$ [A]
Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)



DRAIN-CURRENT : $-I_D$ [A]
Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)



DRAIN-CURRENT : $-I_D$ [A]
Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(V)



DRAIN-CURRENT : $-I_D$ [A]
Fig.9 Forward Transfer Admittance vs. Drain Current

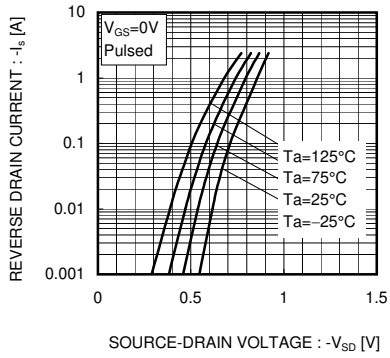


Fig.10 Reverse Drain Current vs. Source-Drain Voltage

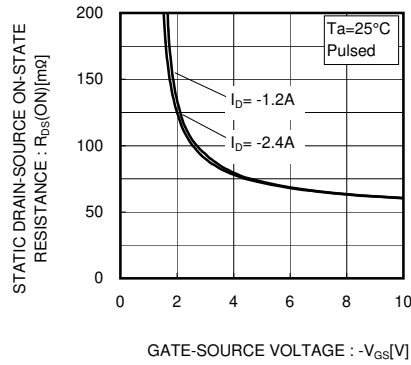


Fig.11 Static Drain-Source On-State Resistance vs. Gate Source Voltage

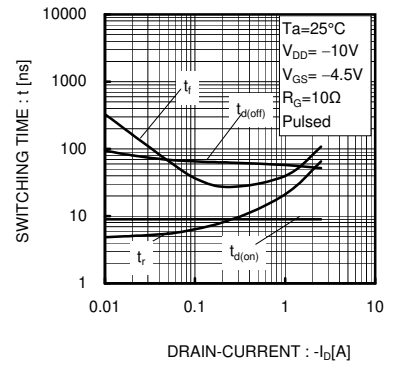


Fig.12 Switching Characteristics

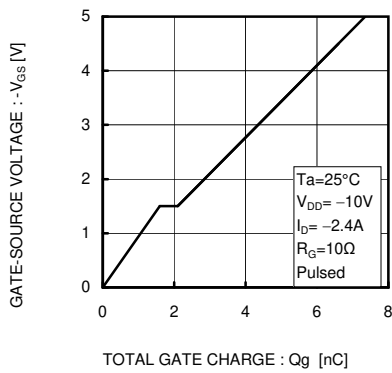


Fig.12 Dynamic Input Characteristics

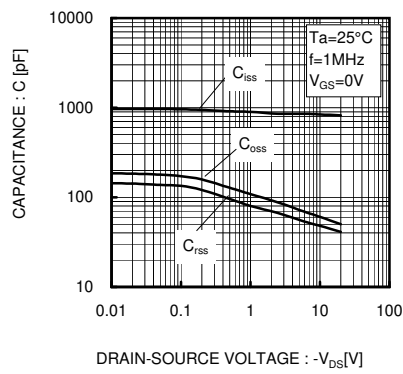


Fig.13 Typical Capacitance vs. Drain-Source Voltage

●Measurement circuits

<Tr1(Nch)>

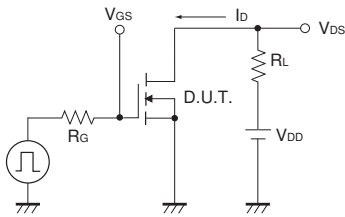


Fig.1-1 Switching time measurement circuit

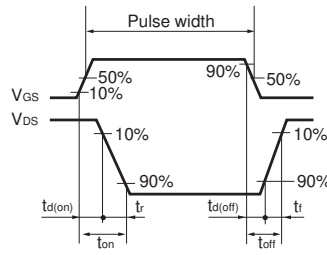


Fig.1-2 Switching waveforms

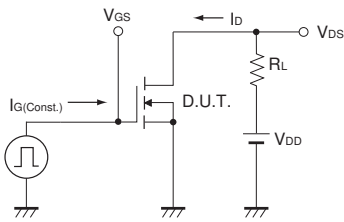


Fig.2-1 Gate charge measurement circuit

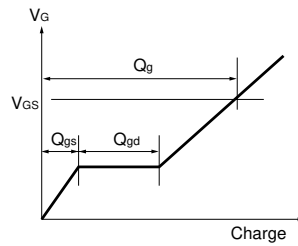


Fig.2-2 Gate Charge Waveform

<Tr2(Pch)>

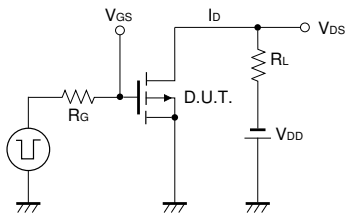


Fig 3-1 Switching Time Measurement Circuit

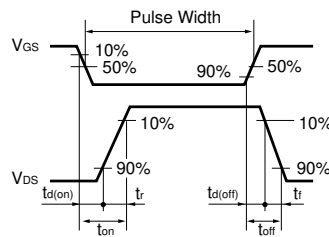


Fig 3-2 Switching Waveforms

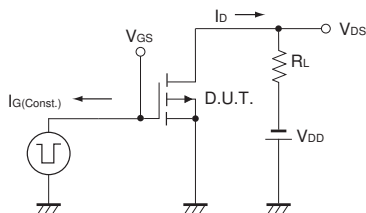


Fig 4-1 Gate charge measurement circuit

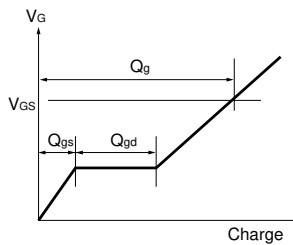


Fig 4-2 Gate Charge Waveform

●Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

Notes

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