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Wireless Components

2 Band TV Tuner Mixer-Oscillator-PLL with balanced IF-Amplifier

TUA6020 Version 1.2

Specification April 2000

preliminary

Revision History: Current Version: 04.00		
Previous Version:Target Data Sheet		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
5-8, 5-9	5-8, 5-9	oscillator phase noise data
all	all	status: target to preliminary
5-27		Input impedance of VHF mixer
5-29		Output impedance of IF output

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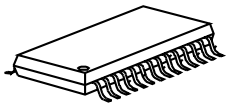
Product Info

General Description

The **TUA6020** is a 5 V mixer/oscillator and synthesizer for analog and digital TV and VCR tuners.

Package



Features

General

- Suitable for analog and digital terrestrial TV tuner
- Full ESD protection

Mixer/Oscillator

- High impedance mixer input for LOW/MID band
- Low impedance mixer input for HIGH band
- 4 pin oscillator for LOW/MID band
- 4 pin oscillator for HIGH band

IF-Amplifier

- balanced SAW preamplifier
- Low output impedance

PLL

- PLL with short lock-in time
- High voltage VCO tuning output
- Fast I^2C bus
- 3 NPN bandswitch buffers
- Internal LOW-MID/HIGH switch
- Lock-in flag
- Power-down reset
- Programmable reference divider ratios: 24, 64, 80, 128
- Programmable charge pump current

Application

- The IC is suitable for PAL tuner in TV- and VCR-sets or set-top receivers for analog TV and **D**igital **V**ideo **B**roadcasting.

Ordering Information

Type	Ordering Code	Package
TUA6020	Q67037-A1127-A701 (tape and reel)	P-TSSOP-28-1

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2 Product Description

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2.1 General Description

The **TUA6020** device combines a digitally programmable phase locked loop (PLL), with a mixer-oscillator block including two balanced mixers and oscillators for use in TV and VCR tuners.

The PLL block with four selectable chip addresses forms a digitally programmable phase locked loop. With a 4 MHz quartz crystal, the PLL permits precise setting of the frequency of the tuner oscillator up to 1024 MHz in increments of 31.25, 50, 62.5 or 166.7 kHz. The tuning process is controlled by a microprocessor via an I^2C bus. The device has three output ports. A flag is set when the loop is locked. It can be read by the processor via the I^2C bus.

The mixer-oscillator block includes two balanced mixers (one mixer with high-impedance input and one mixer with a balanced low-impedance input), two frequency and amplitude-stable balanced oscillators for LOW/MID and HIGH, an IF amplifier, a low-noise reference voltage source, and a band switch.

2.2 Features

General

- Suitable for analog and digital terrestrial TV tuner
- Full ESD protection

Mixer/Oscillator

- High impedance mixer input for LOW/MID band
- Low impedance mixer input for HIGH band
- 4 pin oscillator for LOW/MID band
- 4 pin oscillator for HIGH band

IF-Amplifier

- balanced SAW preamplifier
- Low output impedance

PLL

- PLL with short lock-in time
- High voltage VCO tuning output
- Fast I^2C bus
- 3 NPN bandswitch buffers
- Internal LOW-MID/HIGH switch
- Lock-in flag
- Power-down reset

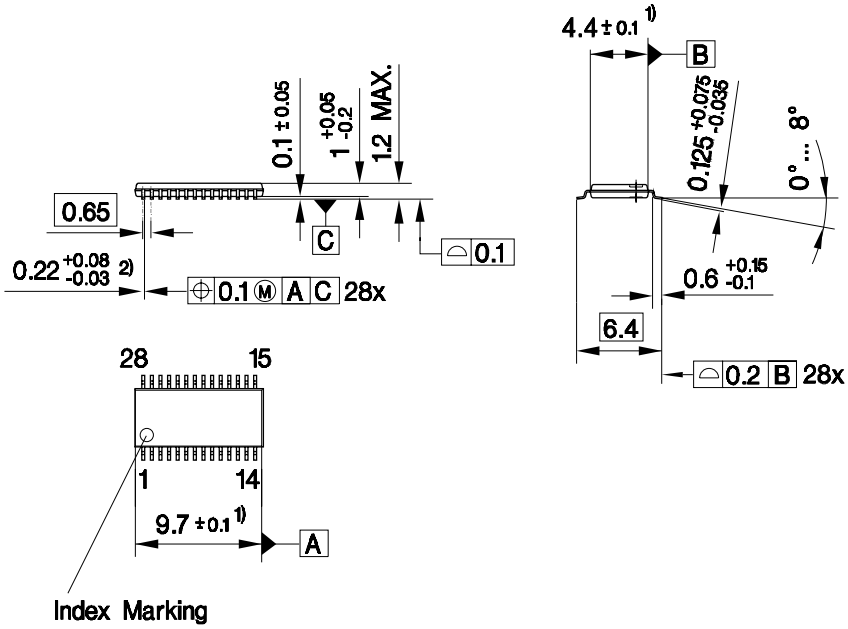
- Programmable reference divider ratios: 24, 64, 80, 128
- Programmable charge pump current

2.3 Application

- The IC is suitable for PAL tuners in TV- and VCR-sets or set-top receivers for analog TV and **D**igital **V**ideo **B**roadcasting.

2.4 Package Outlines

P-TSSOP-28-1



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

3 Functional Description

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3.1 Pin Configuration

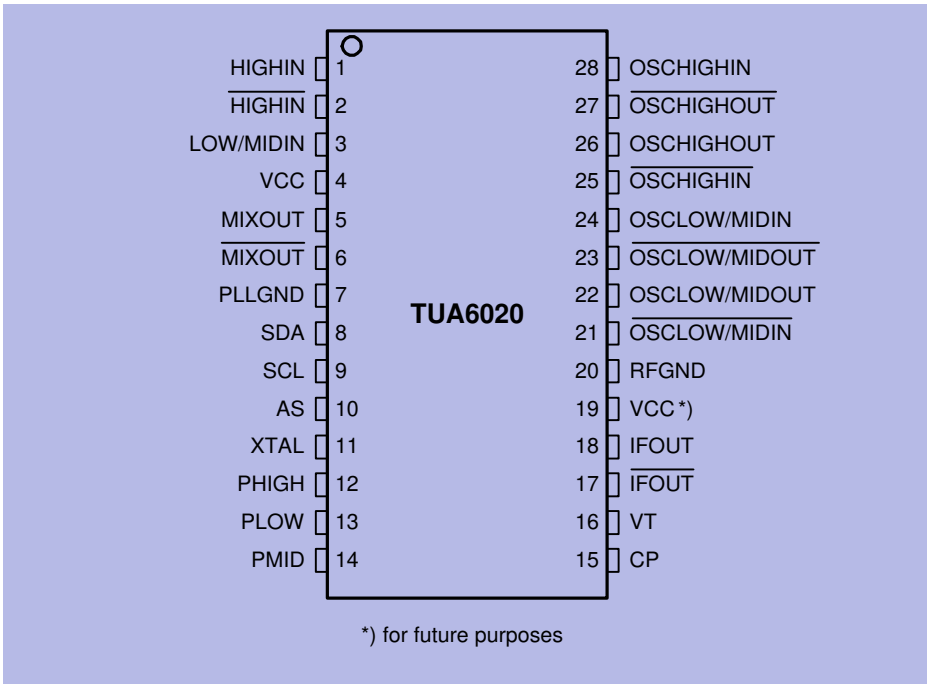


Figure 3-1 Pin Configuration

3.2 Internal Pin Configuration

Table 3-1 Pin Definition and Function

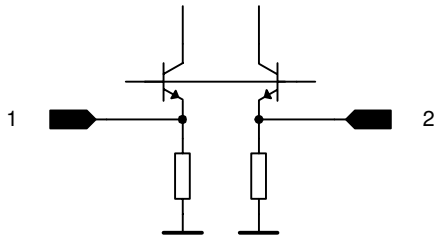
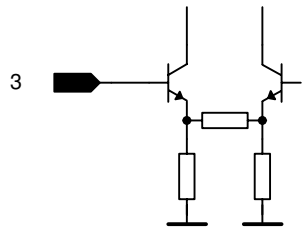
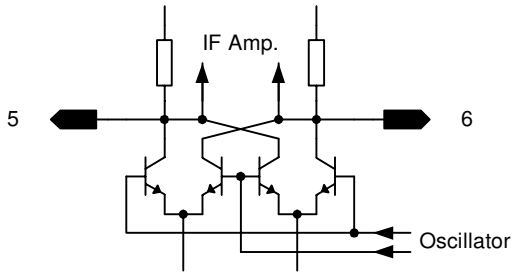
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage	
			LOW/MID	HIGH
1	HIGHIN		0.0 V	0.9 V
2	$\overline{\text{HIGHIN}}$		0.0 V	0.9 V
3	LOW/MIDIN		1.8 V	0.0 V
4	VCC	supply voltage	5.0 V	5.0 V
5	MIXOUT		3.8 V	3.8 V
6	$\overline{\text{MIXOUT}}$		3.8 V	3.8 V
7	PLLGND	digital ground	0.0 V	0.0 V

Table 3-1 Pin Definition and Function (continued)

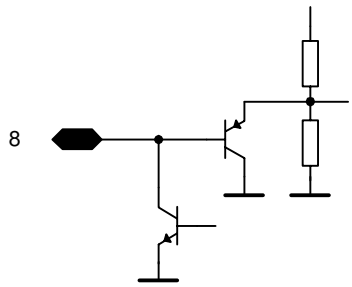
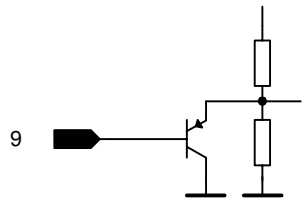
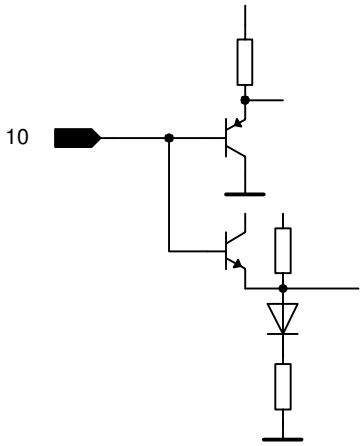
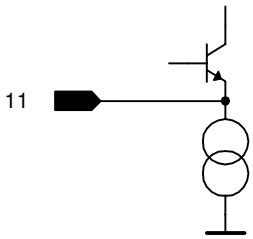
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage	
			LOW/MID	HIGH
8	SDA		n.a.	n.a.
9	SCL		n.a.	n.a.
10	AS		V_{AS}	V_{AS}
11	XTAL		3.0 V	3.0 V

Table 3-1 Pin Definition and Function (continued)

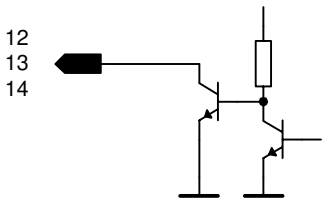
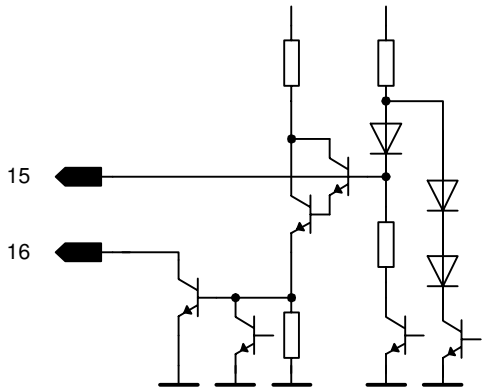
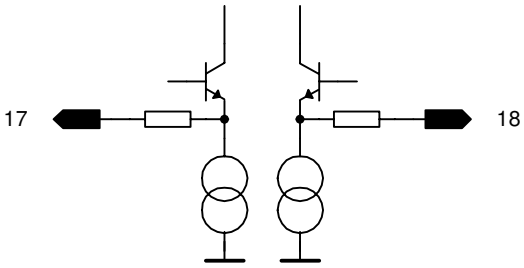
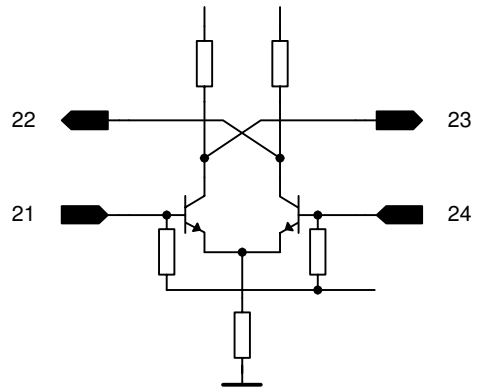
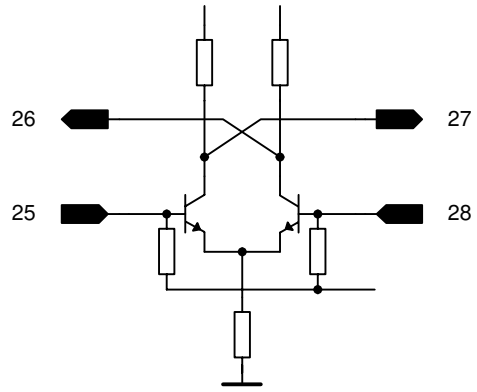
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage	
			LOW/MID	HIGH
12	PHIGH		5 V	V_{CE}
13	PLOW		5 V or V_{CE}	5 V
14	PMID		5 V or V_{CE}	5 V
15	CP		1.9 V	1.9 V
16	VT		V_T	V_T
17	$\overline{\text{IFOUT}}$		2.3 V	2.3 V
18	IFOUT		2.3 V	2.3 V
19	VCC	supply voltage	5.0 V	5.0 V
20	RFGND	analog ground	0.0 V	0.0 V

Table 3-1 Pin Definition and Function (continued)

Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage	
			LOW/MID	HIGH
21	$\overline{\text{OSCLOW}}$/ $\overline{\text{MIDIN}}$		1.6 V	0.0 V
22	OSCLOW/ MIDOUT		2.3 V	0.0 V
23	$\overline{\text{OSCLOW}}$/ $\overline{\text{MIDOUT}}$		2.3 V	0.0 V
24	OSCLOW/ MIDIN		1.6 V	0.0 V
25	$\overline{\text{OSCHIGHIN}}$		0.0 V	1.6 V
26	OSCHIG- HOUT		0.0 V	2.8 V
27	$\overline{\text{OSCHIG-}}$ $\overline{\text{HOUT}}$		0.0 V	2.8 V
28	OSCHIGHIN		0.0 V	1.6 V

3.3 Block Diagram

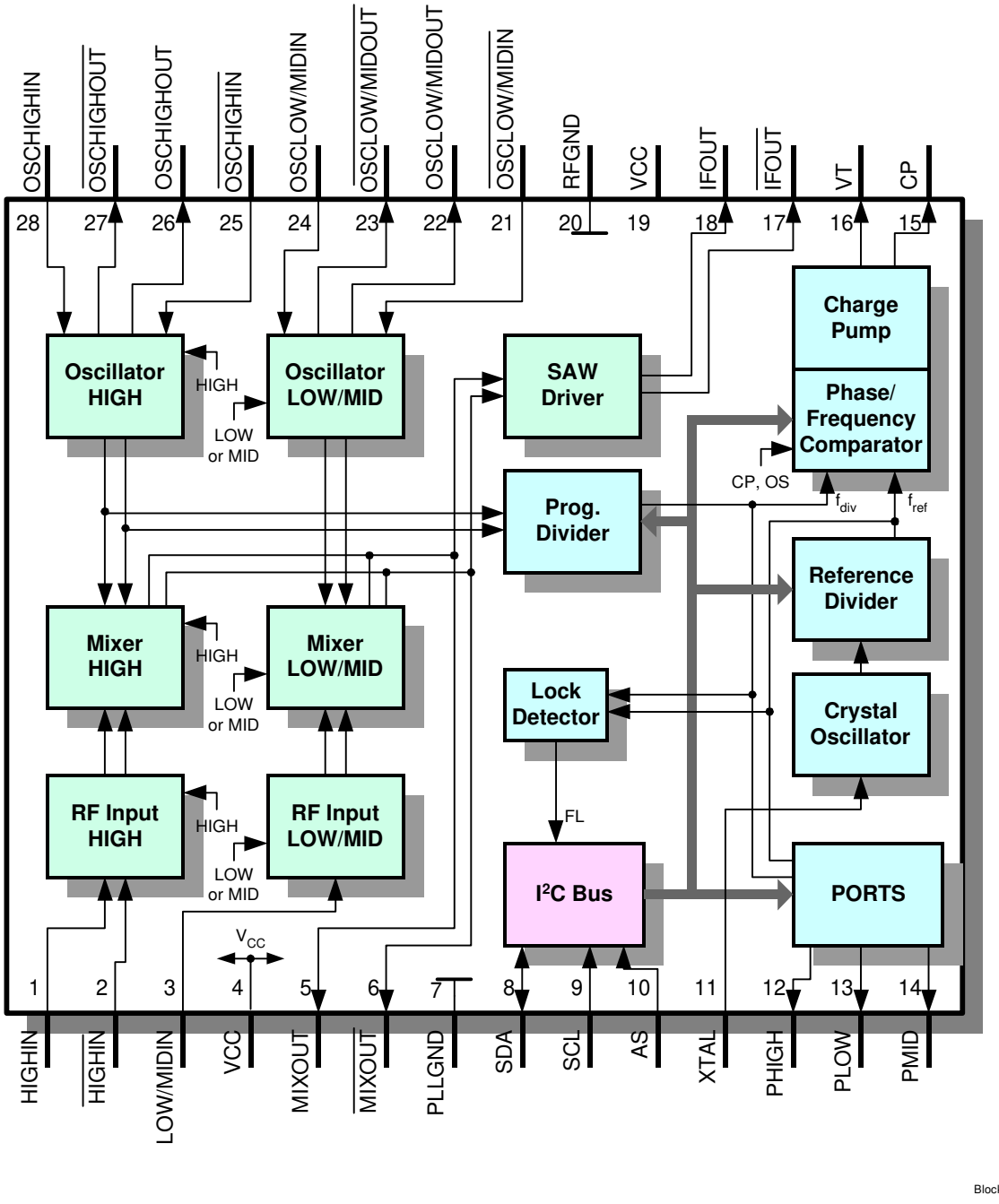


Figure 3-2 Block Diagram

3.4 Circuit Description

3.4.1 Mixer-Oscillator block

The mixer oscillator section includes two balanced mixers (double balanced mixer), two balanced oscillators for LOW/MID and HIGH, an IF amplifier, a reference voltage source and a band switch.

Filters between tuner input and IC separate the TV frequency signals into two bands. The band switching in the tuner front-end is done by using two or three port outputs. In the selected band the signal passes a tuner input stage with MOSFET amplifier, a double-tuned bandpass filter and is then fed to the balanced mixer input of the IC which has in case of LOW / MID a high-impedance input and in case of HIGH a low-impedance input. The input signal is mixed there with the signal from the activated on chip oscillator to the IF frequency which is filtered out at the balanced high-impedance output pair by means of a parallel tuned circuit. The following SAW preamplifier has a low output impedance to drive the SAW filter directly.

3.4.2 PLL block

The oscillator signal is internally DC-coupled as a differential signal to the programmable divider inputs. The signal subsequently passes through a programmable divider with ratio N = 256 through 32767 and is then compared in a digital frequency / phase detector to a reference frequency f_{ref} = 31.25, 50, 62.5 or 166.7 kHz.This frequency is derived from an unbalanced, low-impedance 4 MHz crystal oscillator (pin XTAL) divided by R = 128, 80, 64 or 24.

The phase detector has two outputs that drive two current sources of opposite polarity as charge pump. If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the positive current source pulses for the duration of the phase difference. In the reverse case the I- current source pulses. If the two signals are in phase, the charge pump output (CP) goes into the high-impedance state (PLL is locked). An active low-pass filter integrates the current pulses to generate the tuning voltage for the VCO (internal amplifier, external pull-up resistor at TUNE and external RC circuitry). The charge pump output is also switched into the high-impedance state if the control bits T0 = 1 and T1 = 0. Here it should be noted, however, that the tuning voltage can alter over a long period in the high-impedance state as a result of self-discharge in the peripheral circuitry. TUNE may be switched off by the control bit OS to allow external adjustments.

If the VCO is not oscillating the PLL locks to a tuning voltage of 33V (V_{TH}).

By means of control bit CP the pump current can be switched between two values by software. This programmability permits alteration of the control response time of the PLL in the locked-in state. In this way different VCO gains can be compensated, for example.

The software-switched ports PLOW, PMID and PHIGH are general-purpose open-collector outputs. The test bits T0 = 0 and T1 = 1, switch the test signals fref (i.e.fXTAL / 64) and fdiv (divided input signal) to PMID and PLOW respectively.

The lock detector resets the lock flag FL if the width of the charge pump current pulses is wider than the period of the crystal oscillator (i.e. 250 ns). Hence, if FL = 1, the maximum deviation of the input frequency from the programmed frequency is given by

$$\Delta f = \pm I_P * (K_{VCO} / f_{XTAL}) * (C1+C2) / (C1*C2)$$

where I_P is the charge pump current, K_{VCO} the VCO gain, f_{XTAL} the crystal oscillator frequency and C1, C2 the capacitances in the loop filter (see Figure 4-1 Evaluation board, PAL application on page 2). As the charge pump pulses at i.e. 62.5 kHz (= f_{ref}), it takes a maximum of 16 µs for FL to be reset after the loop has lost lock state.

Once FL has been reset, it is set only if the charge pump pulse width is less than 250 ns for eight consecutive f_{ref} periods. Therefore it takes between 128 and 144 µs for FL to be set after the loop regains lock.

3.4.3 I²C-Bus Interface

Data is exchanged between the processor and the PLL via the I²C bus. The clock is generated by the processor (input SCL), while pin SDA functions as an input or output depending on the direction of the data (open collector, external pull-up resistor). Both inputs have hysteresis and a low-pass characteristic, which enhance the noise immunity of the I²C bus.

The data from the processor pass through an I²C bus controller. Depending on their function the data are subsequently stored in registers. If the bus is free, both lines will be in the marking state (SDA, SCL are HIGH). Each telegram begins with the start condition and ends with the stop condition. Start condition: SDA goes LOW, while SCL remains HIGH. Stop condition: SDA goes HIGH while SCL remains HIGH. All further information transfer takes place during SCL = LOW, and the data is forwarded to the control logic on the positive clock edge.

The table ”Bit Allocation” (see Table 5-4 Bit Allocation Read / Write on page 10) should be referred to the following description. All telegrams are transmitted byte-by-byte, followed by a ninth clock pulse, during which the control logic returns the SDA line to LOW (acknowledge condition). The first byte is comprised of seven address bits. These are used by the processor to select the PLL from several peripheral components (chip select). The LSB bit (R/W) determines whether data are written into (R/W = 0) or read from (R/W = 1) the PLL.

In the data portion of the telegram during a WRITE operation, the MSB bit of the first or third data byte determines whether a divider ratio or control information is to follow. In each case the second byte of the same data type has to follow the first byte.

If the address byte indicates a READ operation, the PLL generates an acknowledge and then shifts out the status byte onto the SDA line. If the processor generates an acknowledge, a further status byte is output; otherwise the data line is released to allow the processor to generate a stop condition. The status word consists the lock flag and the power-on flag.

Four different chip addresses can be set by appropriate DC level at pin AS (see Table 5-6 Address selection on page 11).

While applying the supply voltage, a power-on reset circuit prevents the PLL from setting the SDA line to LOW, which would block the bus. The power-on reset flag POR is set at power-on and when V_{CC} falls below 3.2 V. It will be reset at the end of a READ operation.

4 Applications

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4.1 Evaluation board, PAL application 4-2
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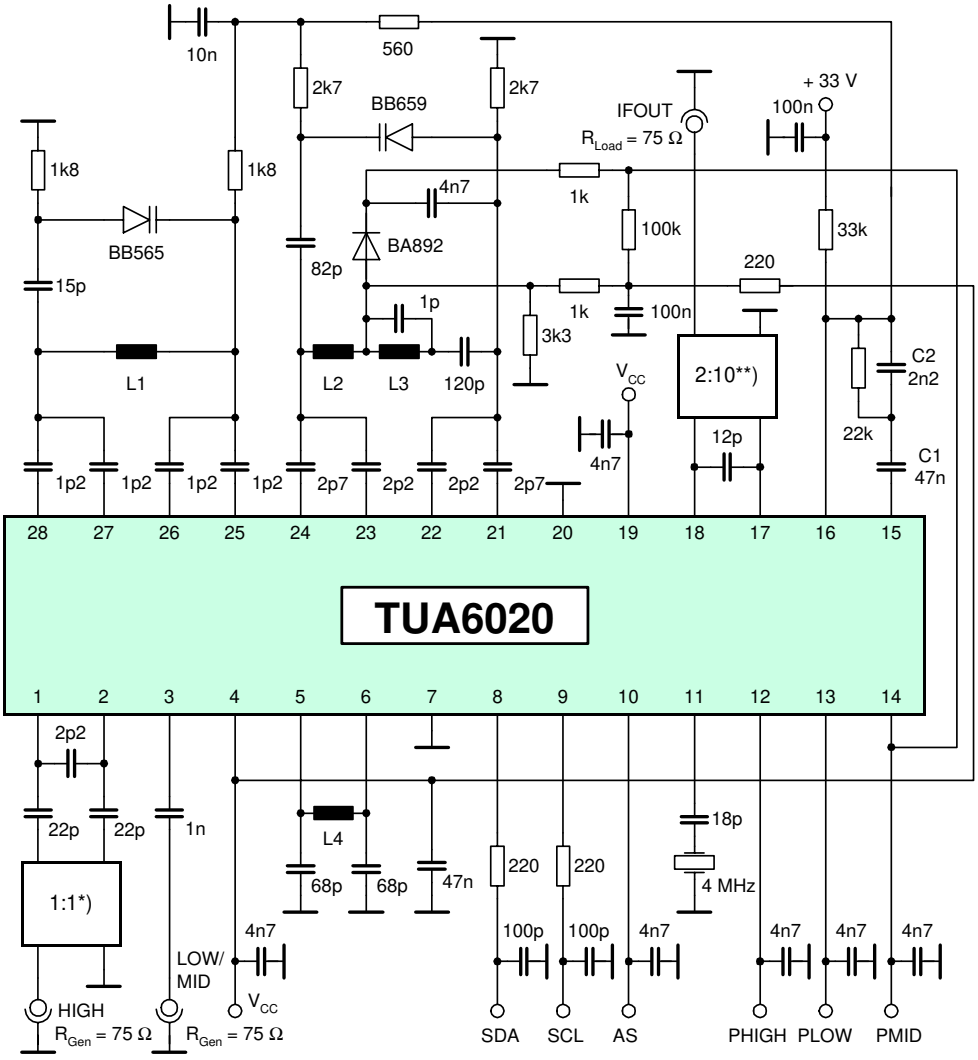
4.1 Evaluation board, PAL application



Application Circuit

Figure 4-1 Evaluation board, PAL application

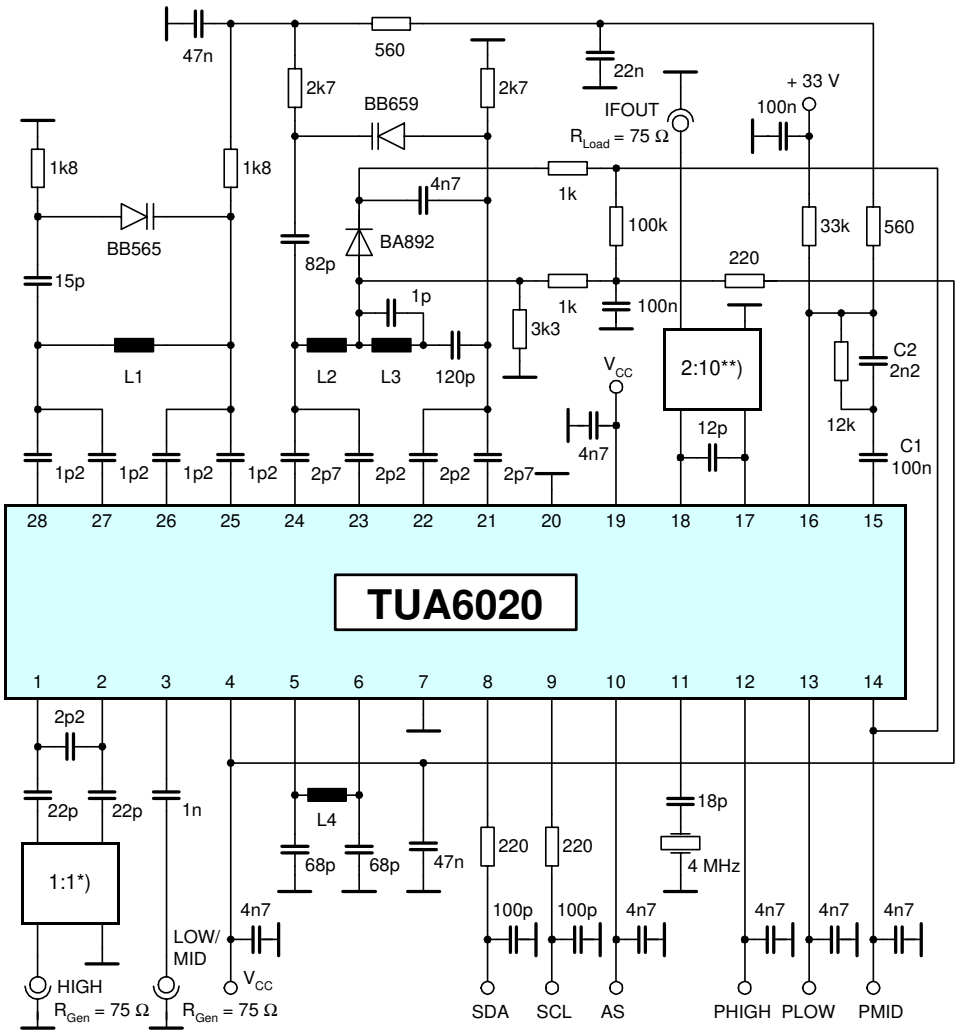
Table 4-1 Recommended band limits in MHz

	RF input		Oscillator	
	min	max	min	max
LOW	48.25	140.25	87.15	179.15
MID	147.25	423.25	186.15	462.15
HIGH	431.25	855.25	470.15	894.15

Table 4-1 Coils

	turns	Ø	wire Ø
L1	1.5	2.4 mm	0.5 mm
L2	2.5	3 mm	0.5 mm
L3	8.5	3.2 mm	0.5 mm
L4	14.5	4 mm	0.3 mm
*)	TOKO B4F Type 617DB-1023		
**)	TOKO 7KL600 GCS-A1010DX		

4.2 Evaluation board, low phase noise application



Application Circuit digital

Figure 4-2 Evaluation board, low phase noise application

Table 4-1 Recommended band limits in MHz

	RF input		Oscillator	
	min	max	min	max
LOW	48.25	140.25	87.15	179.15
MID	147.25	423.25	186.15	462.15
HIGH	431.25	855.25	470.15	894.15

Table 4-1 Coils

	turns	Ø	wire Ø
L1	1.5	2.4 mm	0.5 mm
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L4	14.5	4 mm	0.3 mm
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**)	TOKO 7KL600 GCS-A1010DX		

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5.1 Electrical Data

5.1.1 Absolute Maximum Ratings

WARNING

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC may result.

Table 5-1 Absolute Maximum Ratings, Ambient temperature T_{AMB}= - 20°C ... + 85°C

Parameter [1]	Symbol	Limit Values		Unit	Remarks
		min	max		
Supply voltage	V_{CC}	-0.3	6	V	
Junction temperature	T_J		+150	°C	
Storage temperature	T_{Stg}	-40	+125	°C	
Thermal resistance (junction to ambient)	R_{thJA}		120	K/W	
PLL					
CP	V_{CP}	-0.3	3	V	
	I_{CP}		1	mA	
Crystal oscillator pin XTAL	V_{XTAL}		V_{CC}	V	
	I_{XTAL}	-5		mA	
Bus input/output SDA	V_{SDA}	-0.3	V_{CC}	V	
Bus output current SDA	$I_{SDA(L)}$		5	mA	open collector
Bus input SCL	V_{SCL}	-0.3	V_{CC}	V	
Chip address switch AS	V_{AS}	-0.3	V_{CC}	V	
Tuning voltage output (loop filter)	V_T	-0.3	35	V	
Port outputs PLOW, PMID, PHIGH	V_P	-0.3	V_{CC}	V	
	$I_{P(L)}$	-1	25	mA	t_{max} = 0.1 sec. at 5.5 V
Total port output current	$\Sigma I_{P(L)}$		40	mA	t_{max} = 0.1 sec. at 5.5 V
Mixer-Oscillator					
Mixer inputs LOW/MID	V_i	-0.3	3	V	
Mixer inputs HIGH	V_i		2	V	
	I_i	-5	6	mA	

Table 5-1 Absolute Maximum Ratings, Ambient temperature T_{AMB}= - 20°C ... + 85°C (continued)

Parameter [1]	Symbol	Limit Values		Unit	Remarks
		min	max		
Oscillator base voltage	V_B	-0.3	3	V	
Oscillator collector voltage	V_C		V_{CC}	V	
ESD-Protection [2].					
all pins	V_{ESD}		2	kV	

1). All values are referred to ground (pin), unless stated otherwise.
Currents with a positive sign flow into the pin and currents with a negative sign flow out of pin.

2). According to MIL STD 883D, method 3015.7 and EOS/ESD assn. standardS5.1 - 1993

5.1.2 Operating Range

Within the operational range the IC operates as described in the circuit description. The AC / DC characteristic limits are not guaranteed.

Table 5-2 Operating Range

Parameter	Symbol	Limit Values		Unit	Test Conditions	L	Item
		min	max				
Supply voltage	V_{CC}	+4.5	+5.5	V			
Programmable divider factor	N	256	32767				
LOW/MID Mixer input frequency range	f_i	30	500	MHz			
HIGH Mixer input frequency range	f_i	400	900	MHz			
LOW/MID Oscillator frequency range	f_O	65	560	MHz			
HIGH Oscillator frequency range	f_O	430	950	MHz			
Ambient temperature	T_{AMB}	-20	+85	°C			