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Wireless Components

3-Band TV Tuner IC

TUA6030, TUA6032 Version 2.2

Specification January 2002

Revision History: Current Version: Preliminary Data Sheet,V1.1, August 2000

Previous Version:Target Data Sheet, V1.0, November 1999

Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
all	all	Version to V1.1, status to preliminary.
Product Info	Product Info	Ordering code added.
4-2	4-2	Div. components changed.
4-3	4-3	Div. components changed.
5-2	5-2	Junction temperature and storage temperature +125 °C max.
5-5	5-5	Bus inputs SCL, SDA: V_{IH} = 2.3 V.
5-8,5-9, 5-10	5-8,5-9, 5-10	Input conductance, input capacitance corrected.
5-10	5-10	Phase noise @ ±1 kHz frequency offset deleted. Phase noise, LOW band oscillator: Φ_{OSC} = 92 dBc/Hz min @ ±10 kHz. Phase noise, MID band oscillator: Φ_{OSC} = 92 dBc/Hz min @ ±10 kHz.
5-11	5-11	Phase noise @ ±1 kHz frequency offset deleted. Phase noise, HIGH band oscillator: Φ_{OSC} = 87 dBc/Hz min.
5-14	5-14	Table 5-5, Description of Symbols: CP and OS 'default' added.
5-15	5-15	Table 5-5, Test Modes: Normal operation 'default' added.
5-14	5-14	Table 5-5, Description of Symbols: CP and OS 'default' added.
5-15	5-15	Table 5-5, Test Modes: Normal operation 'default' added.
5-16	5-16	Table 5-10, A to D converter levels, footnote 'No erratic codes in the transition' added, Table 5-1, Defaults at power-on reset, Auxiliary byte, bit5 = 1.
5-18, 5-19, 5-20	5-18, 5-19, 5-20	Smith charts added.
div	div	Tbf's replaced.

Revision History: Current Version: Data Sheet, V2.0, March 2001

Previous Version:Preliminary Data Sheet, V1.1, August 2000

all	all	Version to V2.0, preliminary deleted.
3-3	3-3	LOW-/MID Oscillator: DC levels corrected.
4-2, 4-3	4-2, 4-3	Application circuits modified.
5-2	5-2	New definition of thermal properties.
5-6	5-6, 5-7	Saturation Voltages for P0, 2, 3 added.
5-11	5-11	AGC take-over point: Min/max values added. Mixer output impedance: Values added.

Revision History: Current Version: Preliminary Data Sheet,V1.1, August 2000		
5-11, 5-12	5-11, 5-12	Phase noise corrected.
5-16	5-16	Table 5-1, Defaults at power-on reset, Auxiliary byte, bit5 = 1.
5-18	5-18	More telegram examples.
Revision History: Current Version: Data Sheet, V2.1, July 2001		
Previous Version:Preliminary Data Sheet, V2.0, March 2001		
all	all	Mirror imaged version TUA6032 added.
Revision History: Current Version: Data Sheet, V2.2, Jan 2002		
Previous Version: Data Sheet, V2.1, July 2001		
Prod. Info	Prod. Info	Ordering code of TUA6032 added.

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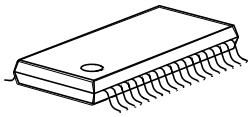
Product Info

General Description

The **TUA6030, TUA6032** devices combine a mixer-oscillator block with a digitally programmable phase locked loop (PLL) for use in TV and VCR tuners.

Package



Features

General

- Suitable for PAL/NTSC and **D**igital **V**ideo **B**roadcasting
- Wideband AGC detector for internal tuner AGC
  – 5 programmable take-over points
  – 2 programmable time constants
- Full ESD protection

Mixer/Oscillator

- High impedance mixer input (common emitter) for LOW band
- Low impedance mixer input (common base) for MID band
- Low impedance mixer input (common base) for HIGH band
- 2 pin oscillator for LOW band
- 2 pin oscillator for MID band
- 4 pin oscillator for HIGH band

IF-Amplifier

- IF preamplifier with symmetrical 75 Ω output impedance able to drive a SAW filter (500 Ω//40 pF)

PLL

- 4 independent I^2C addresses
- I^2C bus protocol compatible with 3.3 V and 5V micro-controllers up to 400 kHz
- Short lock-in time
- High voltage VCO tuning output
- 4 PNP ports
- 3 NPN ports
- 1 NPN port/ADC input
- Internal LOW/MID/HIGH band switch
- Lock-in flag
- Programmable reference divider ratio (24, 64, 80, 128)
- Programmable charge pump current

Application

- The IC is suitable for PAL and NTSC tuners in TV- and VCR-sets or set-top receivers for analog TV and **D**igital **V**ideo **B**roadcasting.
- The AGC stage makes the tuner AGC independent of the Video-IF AGC.

Ordering Information

Type	Ordering Code	Package
TUA6030	Q67037-A1146 (tape and reel)	P-TSSOP-38
TUA6032	Q67037-A1 (tape and reel)	P-TSSOP-38

1 Table of Contents

2 Product Description

Contents of this Chapter

2.1 Overview

The **TUA6030, TUA6032** devices combine a mixer-oscillator block with a digitally programmable phase locked loop (PLL) for use in TV and VCR tuners.

The mixer-oscillator block includes three balanced mixers (one mixer with an unbalanced high-impedance input and two mixers with a balanced low-impedance input), two 2-pin asymmetrical oscillators for the LOW and the MID band, one 4-pin symmetrical oscillator for the HIGH band, an IF amplifier, a reference voltage, and a band switch.

The PLL block with four independently selectable chip addresses forms a digitally programmable phase locked loop. With a 4 MHz quartz crystal, the PLL permits precise setting of the frequency of the tuner oscillator up to 1024 MHz in increments of 31.25, 50, 62.5 or 166.7 kHz. The tuning process is controlled by a microprocessor via an I^2C bus. The device has 8 output ports, one of them (P6) can also be used as ADC input port. A flag is set when the loop is locked. The lock flag can be read by the processor via the I^2C bus.

2.2 Features

General

- Suitable for PAL/NTSC and **D**igital **V**ideo **B**roadcasting
- Wideband AGC detector for internal tuner AGC
  – 5 programmable take-over points
  – 2 programmable time constants
- Full ESD protection

Mixer/Oscillator

- High impedance mixer input (common emitter) for LOW band
- Low impedance mixer input (common base) for MID band
- Low impedance mixer input (common base) for HIGH band
- 2 pin oscillator for LOW band
- 2 pin oscillator for MID band
- 4 pin oscillator for HIGH band

IF-Amplifier

- IF preamplifier with symmetrical 75 Ω output impedance able to drive a SAW filter (500 Ω//40 pF)

PLL

- 4 independent I^2C addresses
- I^2C bus protocol compatible with 3.3 V and 5V micro-controllers up to 400 kHz

- Short lock-in time
- High voltage VCO tuning output
- 4 PNP ports
- 3 NPN ports
- 1 NPN port/ADC input
- Internal LOW/MID/HIGH band switch
- Lock-in flag
- Programmable reference divider ratio (24, 64, 80, 128)
- Programmable charge pump current

2.3 Application

- The IC is suitable for PAL and NTSC tuners in TV- and VCR-sets or cable set-top receivers for analog TV and **D**igital **V**ideo **B**roadcasting.
- The AGC stage makes the tuner AGC independent of the Video-IF AGC.

Recommended band limits in MHz:

Table 2-1 NTSC tuners

	RF input		Oscillator	
Band	**min**	**max**	**min**	**max**
LOW	55.25	127.25	101	173
MID	133.25	361.25	179	407
HIGH	367.25	801.25	413	847

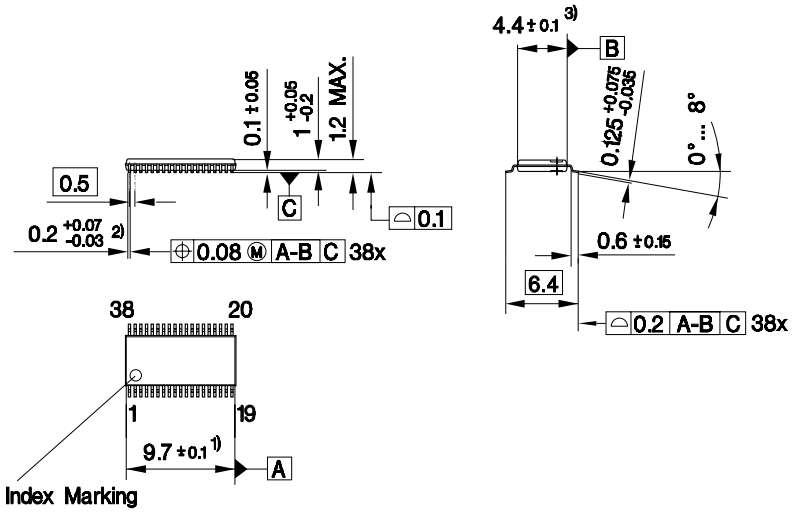
Table 2-2 PAL tuners

	RF input		Oscillator	
Band	**min**	**max**	**min**	**max**
LOW	44.25	154.25	83.15	193.15
MID	161.25	439.25	200.15	478.15
HIGH	447.25	863.25	486.15	902.15

Note: Tuning margin of ±3 MHz not included.

2.4 Package Outlines

P-TSSOP-38

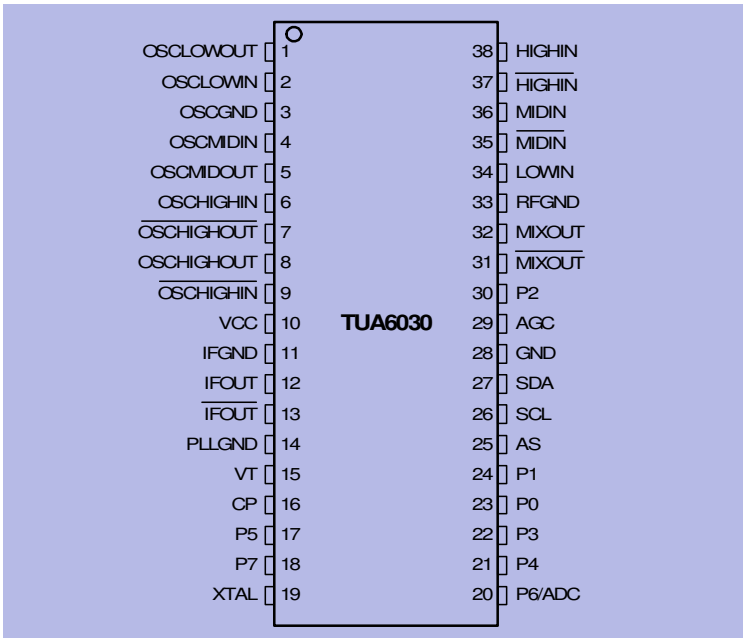


1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.08 max. per side
3) Does not include plastic or metal protrusion of 0.25 max. per side

3 Functional Description

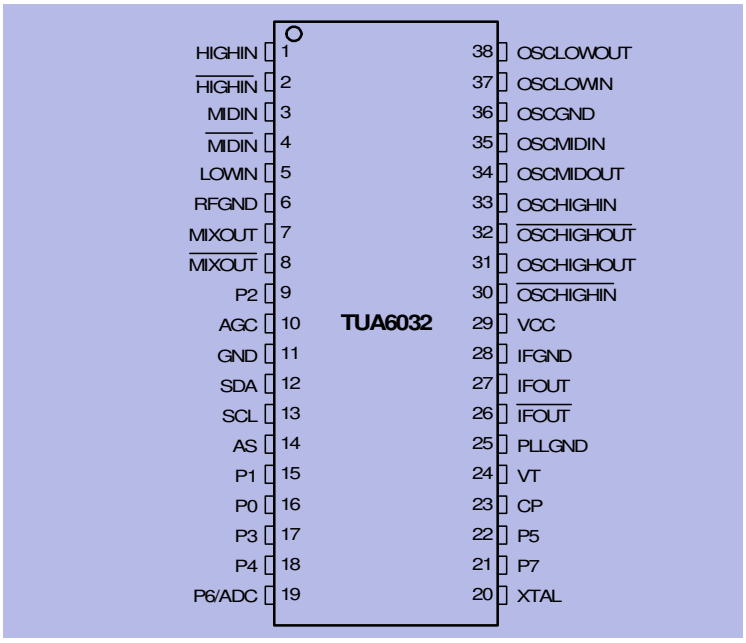
Contents of this Chapter

3.1 Pin Configuration



TUA6030 Pin_config

Figure 3-1 Pin Configuration TUA6030



TUA6032 Pin_config

Figure 3-2 Pin Configuration TUA6032

3.2 Pin Definition and Function

Remark: First pin number refers to TUA6030, second to TUA6032

Table 3-1 Pin Definition and Function

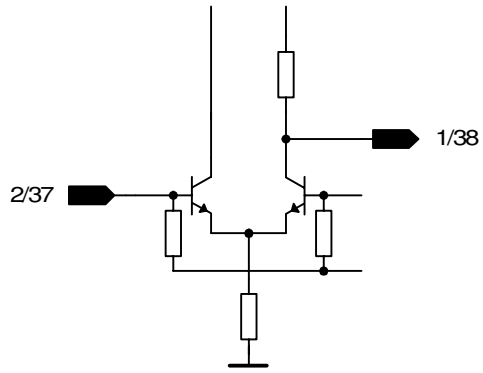
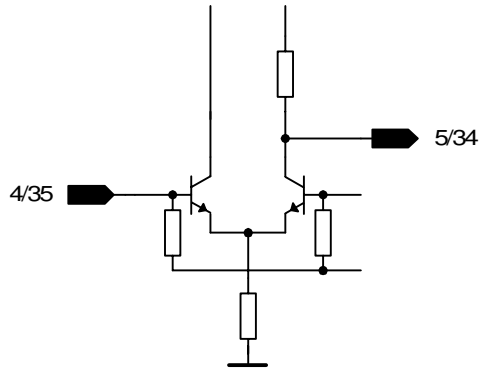
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage		
			LOW	MID	HIGH
1/38	OSCLOWOUT		2.2 V		
2/37	OSCLOWIN		1.5 V		
3/36	OSCGND	oscillator ground	0.0 V	0.0 V	0.0 V
4/35	OSCMIDIN			1.5 V	
5/34	OSCMIDOUT			2.2 V	

Table 3-1 Pin Definition and Function (continued)

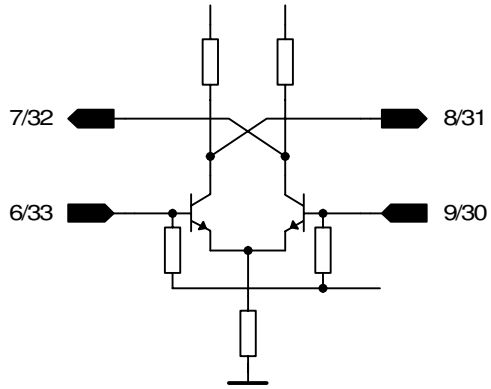
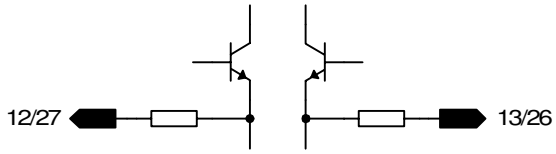
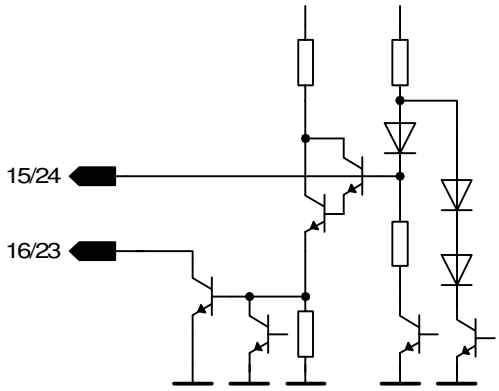
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage		
			LOW	MID	HIGH
6/33	OSCHIGHIN				1.8 V
7/32	$\overline{\text{OSCHIGOUT}}$				2.2 V
8/31	OSCHIGOUT				2.2 V
9/30	$\overline{\text{OSCHIGHIN}}$				1.8 V
10/29	VCC	supply voltage	5.0 V	5.0 V	5.0 V
11/28	IFGND	IF ground	0.0 V	0.0 V	0.0 V
12/27	IFOUT		2.1 V	2.1 V	2.1 V
13/26	$\overline{\text{IFOUT}}$		2.1 V	2.1 V	2.1 V
14/25	PLLGND	PLL ground	0.0 V	0.0 V	0.0 V
15/24	VT		VT	VT	VT
16/23	CP		1.9 V	1.9 V	1.9 V

Table 3-1 Pin Definition and Function (continued)

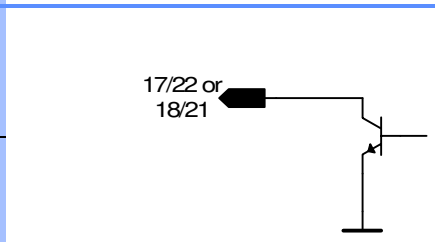
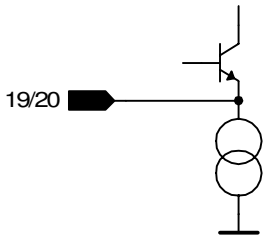
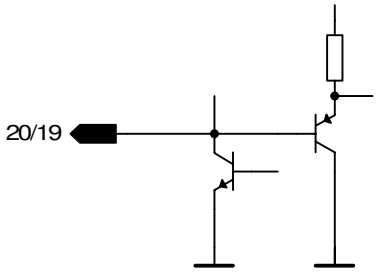
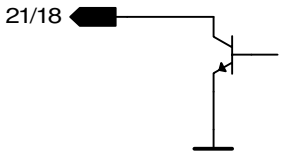
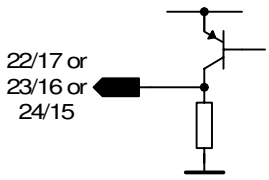
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage		
			LOW	MID	HIGH
17/22	P5		5 V or V_{CE}	5 V or V_{CE}	5 V or V_{CE}
18/21	P7		5 V or V_{CE}	5 V or V_{CE}	5 V or V_{CE}
19/20	XTAL		3.3 V	3.3 V	3.3 V
20/19	P6/ADC		5 V or V_{CE}	5 V or V_{CE}	5 V or V_{CE}
21/18	P4		5 V or V_{CE}	5 V or V_{CE}	5 V or V_{CE}
22/17	P3		n.a.	n.a.	0 V or V_{CC} - V_{CE}
23/16	P0		V_{CC} - V_{CE}	n.a.	n.a.
24/15	P1		n.a.	V_{CC} - V_{CE}	n.a.

Table 3-1 Pin Definition and Function (continued)

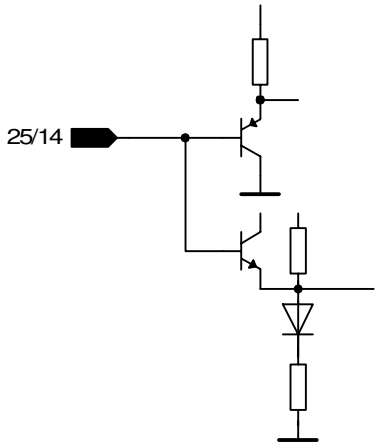
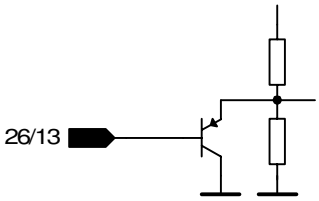
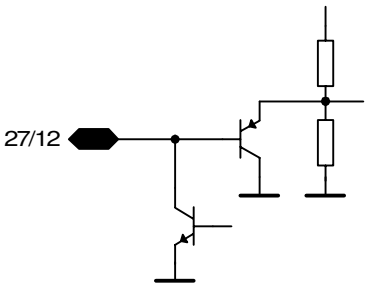
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage		
			LOW	MID	HIGH
25/14	AS		V_{AS}	V_{AS}	V_{AS}
26/13	SCL		n.a.	n.a	n.a
27/12	SDA		n.a	n.a	n.a
28/11	GND	ground	0.0	0.0	0.0

Table 3-1 Pin Definition and Function (continued)

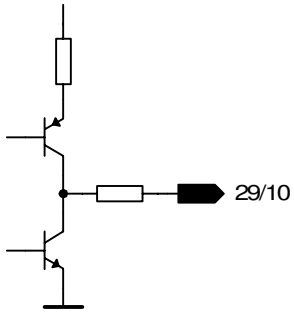
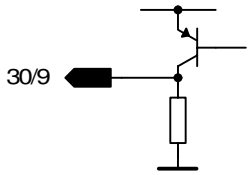
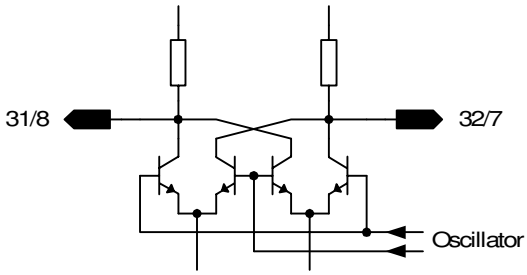
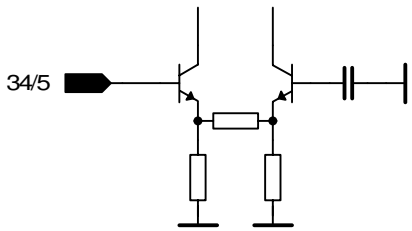
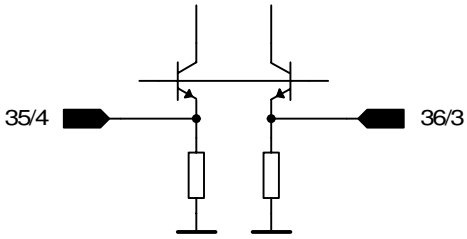
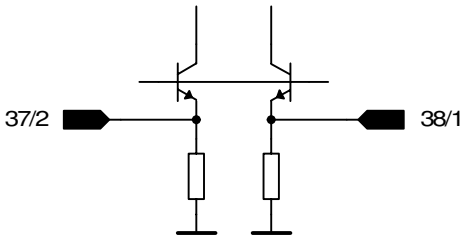
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage		
			LOW	MID	HIGH
29/10	AGC		3.0 V	3.0 V	3.0 V
30/9	P2		n.a.	n.a.	0 V or V_{CC} - V_{CE}
31/8	$\overline{\text{MIXOUT}}$		4.0 V	4.0 V	4.0 V
32/7	MIXOUT		4.0 V	4.0 V	4.0 V
33/6	RFGND	IF ground	0.0 V	0.0 V	0.0 V
34/5	LOWIN		1.9 V		

Table 3-1 Pin Definition and Function (continued)

Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage		
			LOW	MID	HIGH
35/4	$\overline{\text{MIDIN}}$			0.75 V	
36/3	MIDIN			0.75 V	
37/2	$\overline{\text{HIGHIN}}$				0.75 V
38/1	HIGHIN				0.75 V

3.3 Block Diagram

Remark: First pin number refers to TUA6030, second to TUA6032

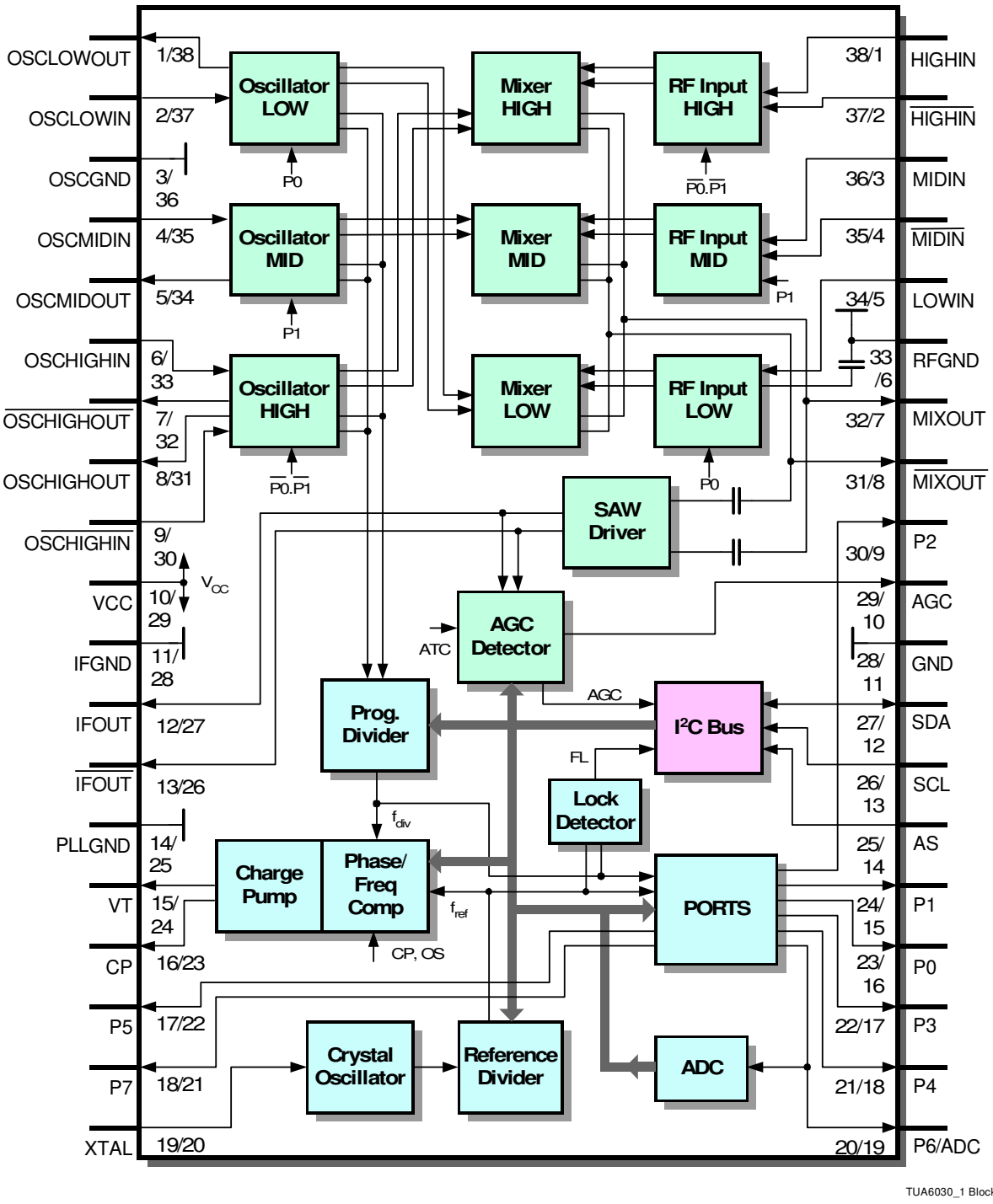


Figure 3-3 Block Diagram

3.4 Circuit Description

3.4.1 Mixer-Oscillator block

The mixer-oscillator block includes three balanced mixers (one mixer with an unbalanced high-impedance input and two mixers with a balanced low-impedance input), two 2-pin asymmetrical oscillators for the LOW and the MID band, one 4-pin symmetrical oscillator for the HIGH band, an IF amplifier, a reference voltage, and a band switch.

Filters between tuner input and IC separate the TV frequency signals into three bands. The band switching in the tuner front-end is done by using three PNP port outputs. In the selected band the signal passes a tuner input stage with a MOSFET amplifier, a double-tuned bandpass filter and is then fed to the mixer input of the IC which has in case of LOW band a high-impedance input and in case of MID or HIGH band a low-impedance input. The input signal is mixed there with the signal from the activated on chip oscillator to the IF frequency which is filtered out at the balanced mixer output pair by means of a parallel tuned circuit. The following IF amplifier is capacitively coupled to the mixer outputs and has a low output impedance to drive the SAW filter directly.

3.4.2 PLL block

The oscillator signal is internally DC-coupled as a differential signal to the programmable divider inputs. The signal subsequently passes through a programmable divider with ratio N = 256 through 32767 and is then compared in a digital frequency/phase detector with a reference frequency f_{ref} = 31.25, 50, 62.5 or 166.7 kHz. This frequency is derived from an unbalanced, low-impedance 4 MHz crystal oscillator (pin XTAL) divided by 128, 80,64 or 24. The reference frequencies will be different with a quartz other than 4 MHz.

The phase detector has two outputs which drive two current sources of a charge pump. If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the positive current source pulses for the duration of the phase difference. In the reverse case the negative current source pulses. If the two signals are in phase, the charge pump output (CP) goes into the high-impedance state (PLL is locked). An active low-pass filter integrates the current pulses to generate the tuning voltage for the VCO (internal amplifier, external pull-up resistor at VT and external RC circuitry). The charge pump output is also switched into the high-impedance state if the control bits T2, T1,T0 = 0, 1, 0. Here it should be noted, however, that the tuning voltage can alter over a long period in the high impedance state as a result of self discharge in the peripheral circuity. VT may be switched off by the control bit OS to allow external adjustments.

If the VCO is not oscillating the PLL locks to a tuning voltage of 33V (V_{TH}).

By means of control bit CP the pump current can be switched between two values by software. This programmability permits alteration of the control response of the PLL in the locked-in state. In this way different VCO gains can be compensated, for example.

The software controlled ports P0 to P7 are general purpose open-collector outputs. The test bits T2, T1, T0 =1, 0, 0 switch the test signals f_{div} (divided input signal) and f_{ref} (i.e.4 MHz / 64) to P4 and P5 respectively.

The lock detector resets the lock flag FL if the width of the charge pump current pulses is greater than the period of the crystal oscillator (i.e. 250 ns). Hence, if FL = 1, the maximum deviation of the input frequency from the programmed frequency is given by

$$\Delta f = \pm I_P * (K_{VCO} / f_{XTAL}) * (C1+C2) / (C1*C2)$$

where I_P is the charge pump current, K_{VCO} the VCO gain, f_{Xtal} the crystal oscillator frequency and C_1, C_2 the capacitances in the loop filter (Chapter 4). As the charge pump pulses at i.e. 62.5 kHz (= f_{ref}), it takes a maximum of 16 µs for FL to be reset after the loop has lost lock state.

Once FL has been reset, it is set only if the charge pump pulse width is less than 250 ns for eight consecutive f_{ref} periods. Therefore it takes between 128 and 144 µs for FL to be set after the loop regains lock.

3.4.3 AGC

The wide-band AGC stage detects the level of the IF output signal and generates an AGC voltage for gain control of the tuner input transistors. The AGC take-over and the time constant are selectable by the I^2C bus.

3.4.4 I^2C-Bus Interface

Data is exchanged between the processor and the PLL via the I^2C bus. The clock is generated by the processor (input SCL). Pin SDA functions as an input or output depending on the direction of the data (open collector, external pull-up resistor). Both inputs have a hysteresis and a low-pass characteristic, which enhance the noise immunity of the I^2C bus.

The data from the processor pass through an I^2C bus controller. Depending on their function the data are subsequently stored in registers. If the bus is free, both lines will be in the marking state (SDA, SCL are high). Each telegram begins with the start condition and ends with the stop condition. Start condition: SDA goes low, while SCL remains high. Stop condition: SDA goes high while

SCL remains high. All further information transfer takes place during SCL = low, and the data is forwarded to the control logic on the positive clock edge.

The table 'Bit Allocation' (see Table 5-4 Bit Allocation Read / Write on page 39) should be referred to for the following description. All telegrams are transmitted byte-by-byte, followed by a ninth clock pulse, during which the control logic returns the SDA line to low (acknowledge condition). The first byte is comprised of seven address bits. These are used by the processor to select the PLL from several peripheral components (address select). The LSB bit (R/W) determines whether data are written into (R/W = 0) or read from (R/W = 1) the PLL.

In the data portion of the telegram during a WRITE operation, the MSB bit of the first or third data byte determines whether a divider ratio or control information is to follow. In each case the second byte of the same data type has to follow the first byte. Appropriate setting of the test bits will decide whether the band-switch byte or the auxiliary byte will be transmitted (see Table 5-7 Test modes on page 40).

If the address byte indicates a READ operation, the PLL generates an acknowledge and then shifts out the status byte onto the SDA line. If the processor generates an acknowledge, a further status byte is output; otherwise the data line is released to allow the processor to generate a stop condition. The status word consists of three bits from the A/D converter, the lock flag and the power-on flag.

Four different chip addresses can be set by an appropriate DC level at pin AS (see Table 5-6 Address selection on page 40).

While the supply voltage is applied, a power-on reset circuit prevents the PLL from setting the SDA line to low, which would block the bus. The power-on reset flag POR is set at power-on and if V_{CC} falls below 3.2 V. It will be reset at the end of a READ operation.

4 Applications

Contents of this Chapter

4.1 Circuits

Remark: Pinning refers to TUA6030

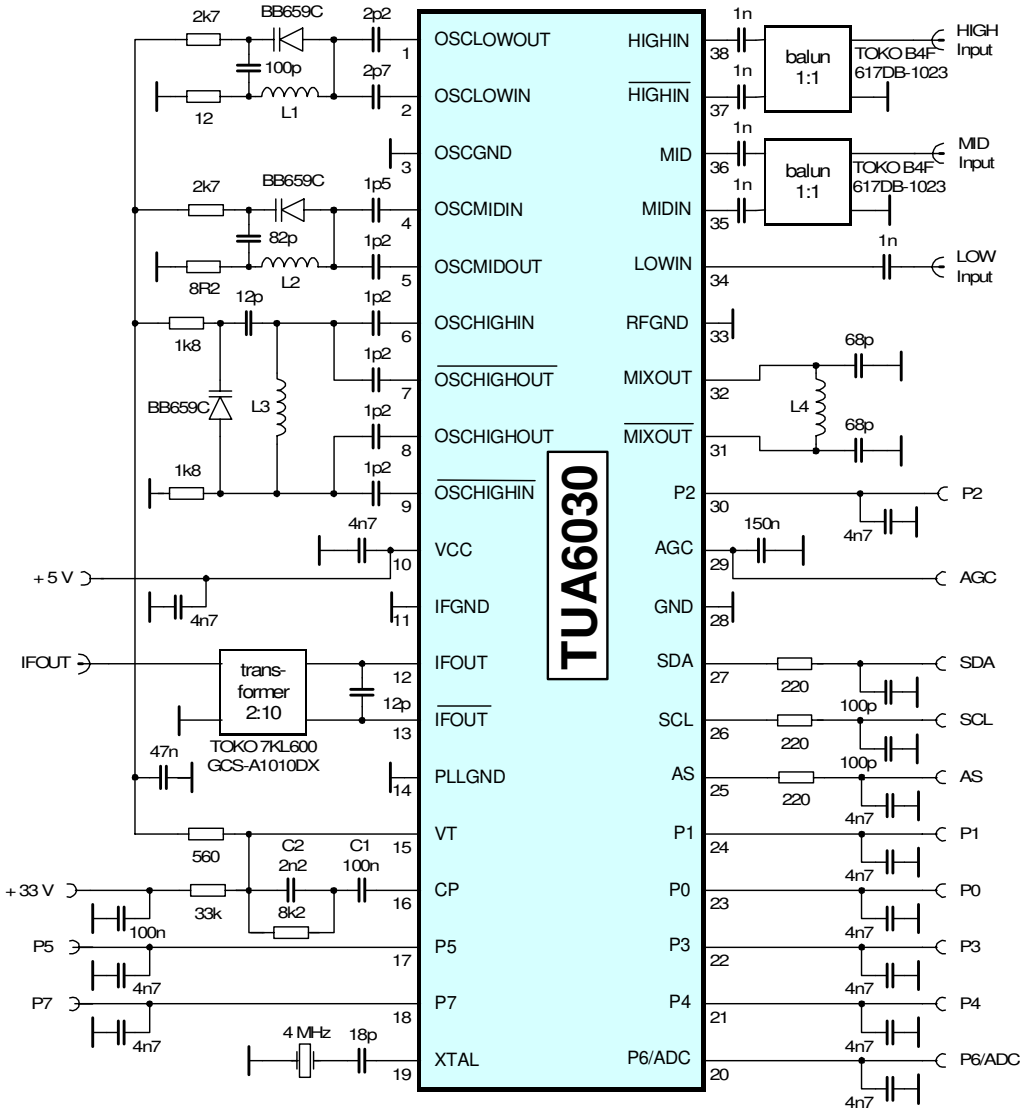
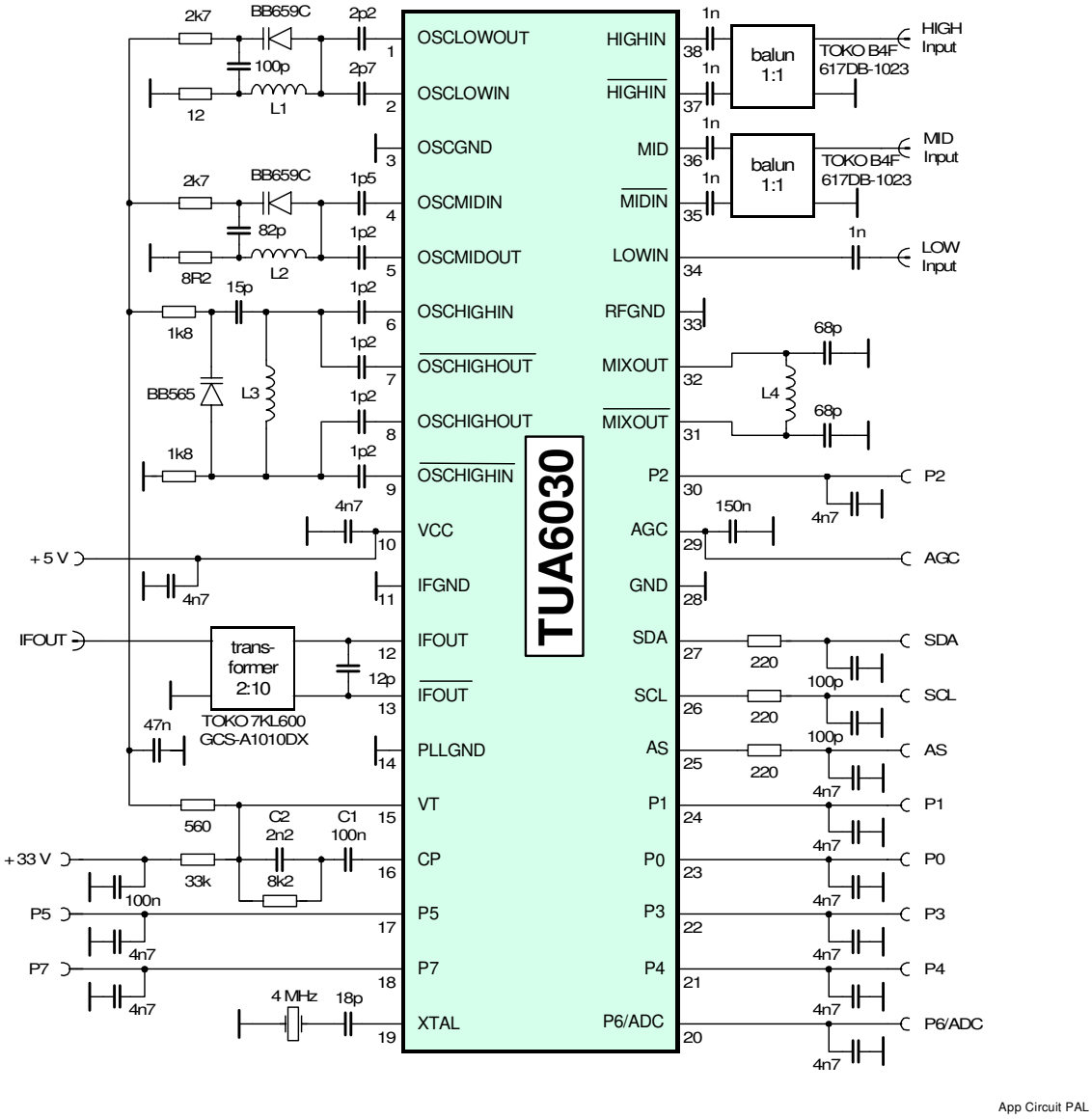


Figure 4-1 Application Circuit for NTSC

Recommended band limits in MHz				
	RF input		Oscillator	
	min	max	min	max
LOW	55.25	127.25	101	173
MID	133.25	361.25	179	407
HIGH	367.25	801.25	413	847

Coils			
	turns	∅	wire ∅
L1	8.5	3.2 mm	0.5 mm
L2	3.5	2.5 mm	0.5 mm
L3	1.5	2.4 mm	0.5 mm
L4	12.5	3.5 mm	0.3 mm

Remark: Pinning refers to TUA6030



App Circuit PAL

Figure 4-2 Application Circuit for PAL

Recommended band limits in MHz				
	RF input		Oscillator	
	min	max	min	max
LOW	44.25	154.25	83.15	193.15
MID	161.25	439.25	200.15	478.15
HIGH	447.25	863.25	486.15	902.15

Coils			
	turns	∅	wire ∅
L1	8.5	3.2 mm	0.5 mm
L2	2.5	3 mm	0.5 mm
L3	1.5	2.4 mm	0.5 mm
L4	14.5	4 mm	0.3 mm