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TUA6034, TUA6036

3-Band Digital TV / Set-Top-Box Tuner IC

TAIFUN

Version 2.51

Wireless Communication

Never stop thinking.

Edition 2006-01-11

Published by Infineon Technologies AG,
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Revision History: 2006-01-11 V 2.51

Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
Revision History: Target Spec. V1.1, January 2001		
Previous Version: Target Spec. V1.0, November 2000		
div.	div.	in extended mode reference division ratio 80 replaced by 32
5-2	5-2	new definition of thermal properties

Revision History: Preliminary Spec. V1.2, April 2001		
Previous Version: Target Spec. V1.1, January 2001		
div.	div.	status: preliminary
div.	div.	bug fixes: TSSOP and VQFN pinning. Changes: application focus to digital applications, tbd's replaced by values
5-10, 5-11	5-10, 5-11	phase noise values added
5-21	5-21	diagrams added

Revision History: Preliminary Spec. V1.3, July 2001		
Previous Version: Preliminary Spec. V1.2, April 2001		
div.	div	Stand-by mode added
5-5	5-5	Crystal Oscillator: Input impedances added
5-7	5-7	Output leakage current replaced by port output voltage Symbol for port output saturation voltages changed
5-12	5-12	AGC source current 2 and AGC output voltage changed
5-15	5-15	Definition for MA1= 0 and MA0 = 1 changed

Revision History: Preliminary Spec. V1.4, October 2001		
Previous Version: Preliminary Spec. V1.3, July 2001		
3-5, 3-7	3-5, 3-7	PNP ports: Pull-down resistors added
5-5	5-5	MID band: I_{VCC} corrected
5-10, 5-11	5-10, 5-11	Phase Noise: new values
5-12	5-12	AGC output voltage changed

Revision History: Spec. V2.0, May2002		
Previous Version: Preliminary Spec. V1.4, October 2001		
all	all	preliminary and confidential deleted

Revision History:	**2006-01-11**	V 2.51
div	div	tbf's replaced, ISDB-T application deleted

Revision History: Spec. V2.1, August 2002

Previous Version: Spec. V2.0, May 2002		
5-6	5-6	Bus output SDA, Low-level output voltage, I_{OL} = 6 mA at 400 kHz deleted

Revision History: Spec. V2.2, December 2002

Previous Version: Spec. V2.1, August 2002		
3-2	3-2	Pinning of TUA6034-V changed

Revision History: V2.3, February 2003

Previous Version: Spec. V2.2, December 2002		
all	all	Mirrored version TUA6036 added

Revision History: V2.4, March 2003

Previous Version: Spec. V2.3, February 2003		
2-10, 4-29, 4-30	2-10, 4-29, 4-30	Frequencies corrected
5-34	5-34	Ambient temperature extended
5-38, 5-39, 5-40	5-38, 5-39, 5-40	Input IP2,Input IIP3, Output voltage causing 1 dB compression added, test frequencies changed

Revision History: V2.5, April 2004

Previous Version: Spec. V2.4, March 2003		
5-35	33	Crystal oscillation frequency added
div.	div.	TUA6034-V in VQFN-48 package
n.a.	28	ISDB-T application added
all	all	New Infineon template (A5 letter page size, page numbering)

Revision History: V2.51, January 2006

Previous Version: Spec. V2.5, April 2004		
all	all	Infineon Logo and postal address changed
div.	div.	stand-by mode replaced with power down mode
8, 11	15	General description: topics added

Revision History: **2006-01-11** V 2.51

14, 20	15, 21	Package GND added for the VQFN package
n.a.	30 - 32	Application circuits for TUA6034-V added
30	34	Absolute Maximum Ratings definitions updated
60	64	PG-VQFN-48 Outline Drawing updated

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horst.klein@infineon.com

Product Info

General Description

The **TUA6034, TUA6036 'TAIFUN'** device combines a mixer-oscillator block with a digitally programmable phase locked loop (PLL) for use in TV and VCR tuners and in set-top-box applications.

Features

General

- Suitable for PAL, NTSC, DVB and ATSC
- Wideband AGC detector for internal tuner AGC
  – 5 programmable take-over points
  – 2 programmable time constants
- Low phase noise
- Full ESD protection
- Qualified according to JEDEC for consumer applications

Mixer/Oscillator

- High impedance mixer input (common emitter) for LOW band
- Low impedance mixer input (common base) for MID band
- Low impedance mixer input (common base) for HIGH band
- 2 pin oscillator for LOW band
- 2 pin oscillator for MID band
- 4 pin oscillator for HIGH band

IF-Amplifier

- 4 IF pins to connect a 2 pole bandpass
- Symmetrical IF preamplifier with low output impedance able to drive a compensated SAW filter (500Ω//40pF)

PLL

- 4 independent I^2C addresses
- I^2C bus protocol compatible with 3.3 V and 5V micro-controllers up to 400 kHz
- High voltage VCO tuning output
- 4 PNP ports
- 1 NPN port/ADC input
- Internal LOW/MID/HIGH band switch
- Bus controlled power down mode
- Lock-in flag
- 6 programmable reference divider ratios (24, 28, 32, 64, 80, 128)
- 4 programmable charge pump currents

Application

- The IC is suitable for PAL, NTSC, DVB-C, DVB-T, ISDB-T and ATSC tuners. The focus is on digital terrestrial.
- The AGC stage makes the tuner AGC independent of the Video-IF AGC

Ordering Information

Type	Ordering Code	Package
TUA6034-T	Q67034-H0009	PG-TSSOP-38
TUA6036-T	Q67037-A0012	PG-TSSOP-38
TUA6034-V	Q67034-H0008	PG-VQFN-48

Table of Contents **Page**

1 Product Description

The **TUA6034, TUA6036 'TAIFUN'** device combines a mixer-oscillator block with a digitally programmable phase locked loop (PLL) for use in TV and VCR tuners and in set-top-box applications.

The mixer-oscillator block includes three balanced mixers (one mixer with an unbalanced high-impedance input and two mixers with a balanced low-impedance input), two 2-pin asymmetrical oscillators for the LOW and the MID band, one 4-pin symmetrical oscillator for the HIGH band, an IF amplifier, a reference voltage, and a band switch.

The PLL block with four independently selectable chip addresses forms a digitally programmable phase locked loop. With a 4 MHz quartz crystal, the PLL permits precise setting of the frequency of the tuner oscillator up to 1024 MHz in increments of 31.25, 50, 62.5, 125, 142.86 or 166.7 kHz. The tuning process is controlled by a microprocessor via an I^2C bus. The device has 5 output ports, one of them (P4) can also be used as ADC input port. A flag is set when the loop is locked. The lock flag can be read by the processor via the I^2C bus.

1.1 Features

1.1.1 General

- Suitable for PAL, NTSC, DVB, ISDB-T and ATSC
- Wideband AGC detector for internal tuner AGC
  - 5 programmable take-over points
  - 2 programmable time constants
- Low phase noise
- Full ESD protection
- Qualified according to JEDEC for consumer applications

1.1.2 Mixer/Oscillator

- High impedance mixer input (common emitter) for LOW band
- Low impedance mixer input (common base) for MID band
- Low impedance mixer input (common base) for HIGH band
- 2 pin oscillator for LOW band
- 2 pin oscillator for MID band
- 4 pin oscillator for HIGH band

1.1.3 IF-Amplifier

- 4 IF pins to connect a 2 pole bandpass

- Symmetrical IF preamplifier with low output impedance able to drive a compensated SAW filter (500 Ω//40 pF)

1.1.4 PLL

- 4 independent I^2C addresses
- I^2C bus protocol compatible with 3.3 V and 5V micro-controllers up to 400 kHz
- High voltage VCO tuning output
- 4 PNP ports
- 1 NPN port/ADC input
- Bus controlled power down mode
- Internal LOW/MID/HIGH band switch
- Lock-in flag
- 6 programmable reference divider ratios (24, 28, 32, 64, 80, 128)
- 4 programmable charge pump currents

1.2 Application

- The IC is suitable for PAL, NTSC, DVB-C, DVB-T, ISDB-T and ATSC tuners. The focus is on digital terrestrial.
- The AGC stage makes the tuner AGC independent of the Video-IF AGC.

Recommended band limits in MHz:

Table 1 ATSC tuners

	RF input		Oscillator	
Band	**min**	**max**	**min**	**max**
LOW	55.25	157.25	101	203
MID	163.25	451.25	201	479
HIGH	457.25	861.25	503	907

Table 2 DVB-T tuners

	RF input		Oscillator	
Band	**min**	**max**	**min**	**max**
LOW	48.25	154.25	87.15	193.15
MID	161.25	439.25	200.15	478.15
HIGH	447.25	863.25	486.15	902.15

Table 3 ISDB-T tuners

	RF input		Oscillator	
Band	**min**	**max**	**min**	**max**
LOW	93	167	150	224
MID	173	467	230	524
HIGH	473	767	530	824

Note: Tuning margin of 3 MHz not included.

2 Functional Description

2.1 Pin Configuration

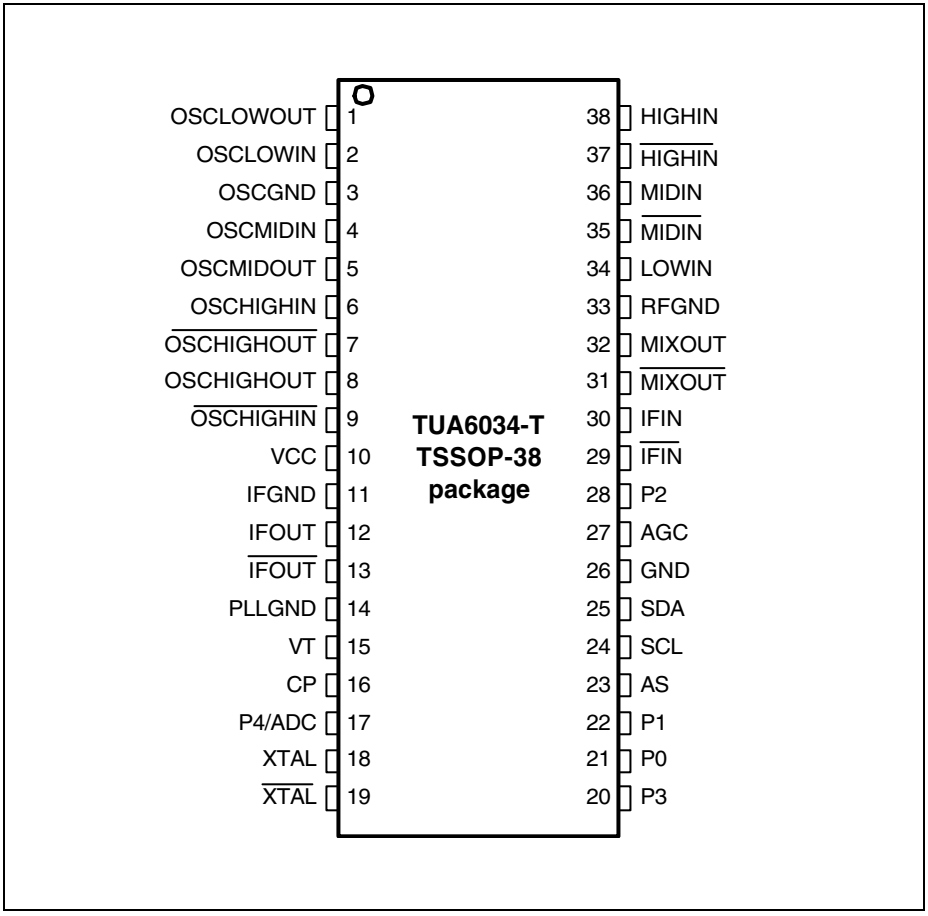


Figure 1 Pin Configuration TUA6034 in PG-TSSOP-38 Package

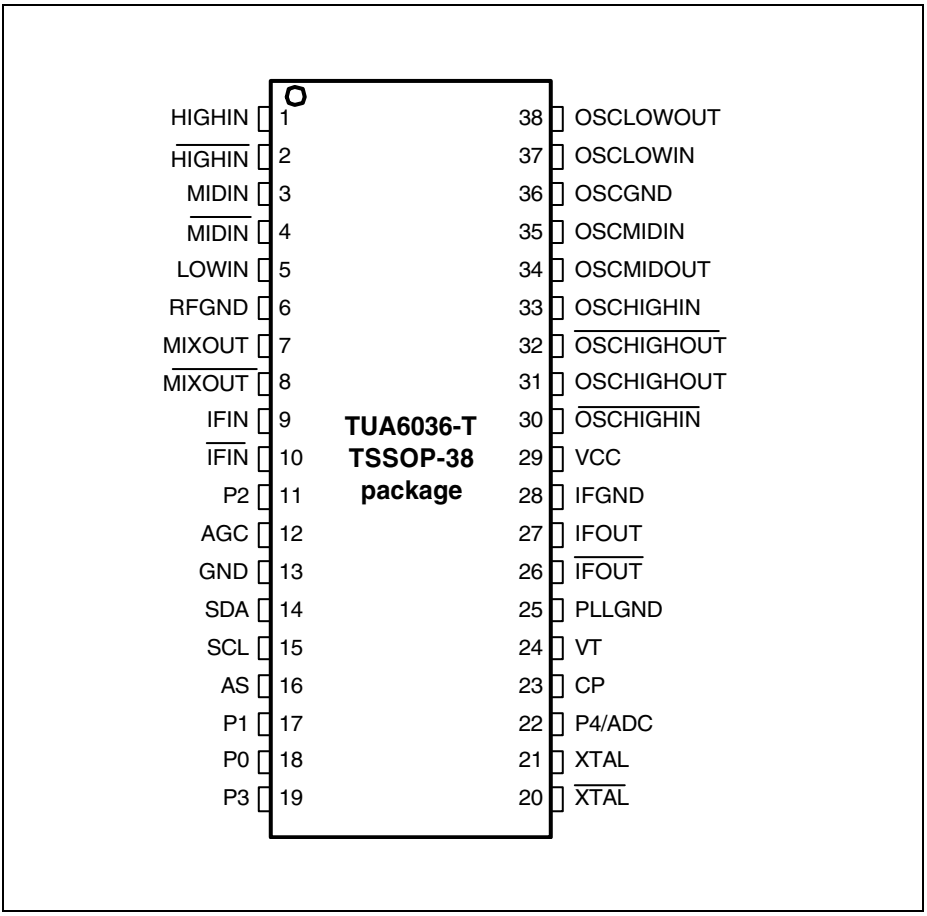


Figure 2 Pin Configuration TUA6036 in PG-TSSOP-38 Package

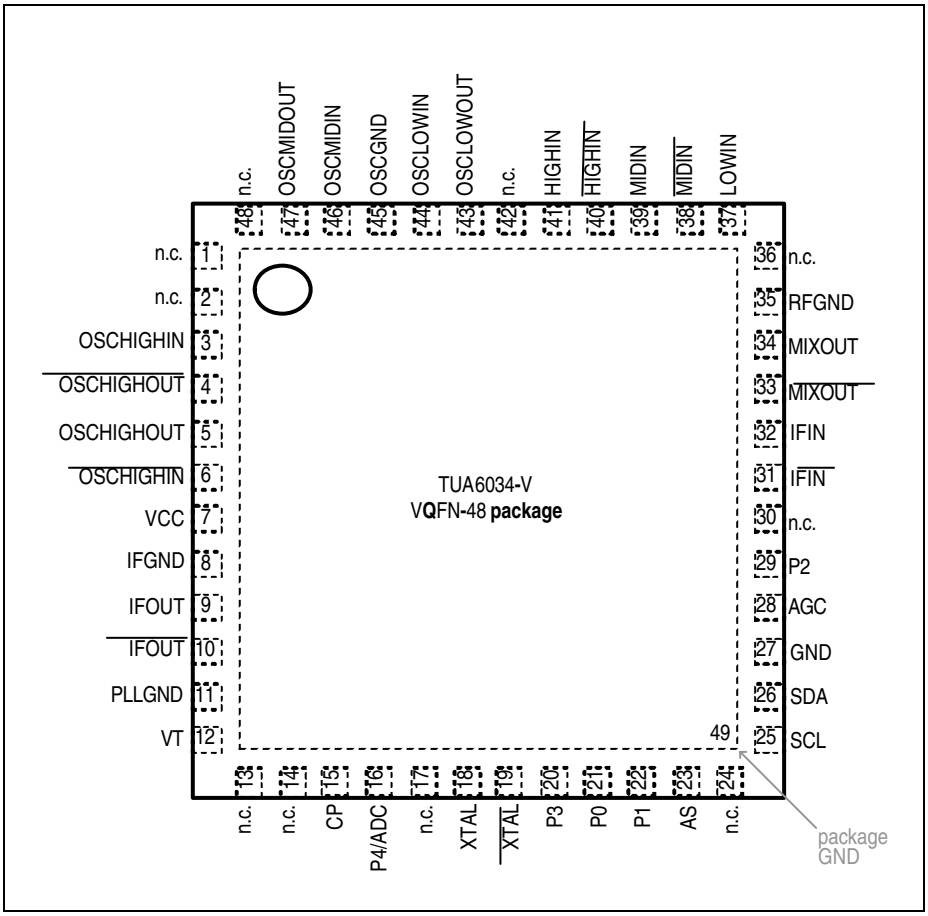
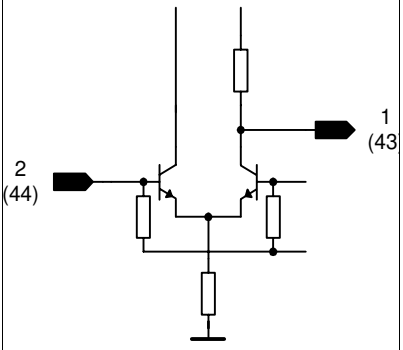
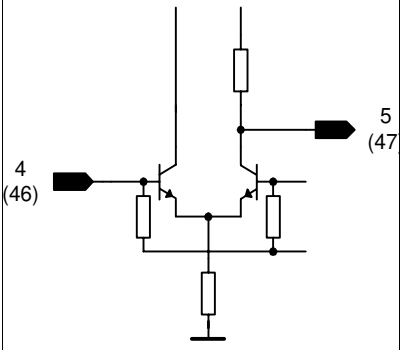
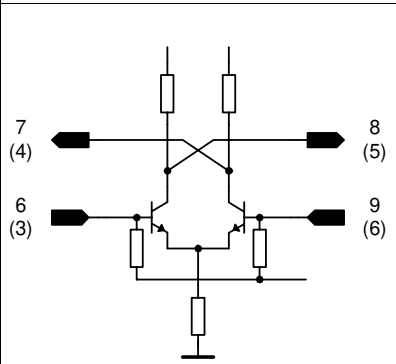
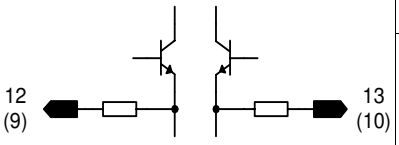


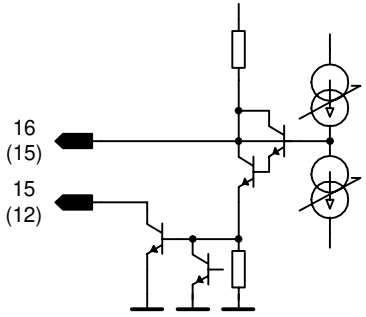
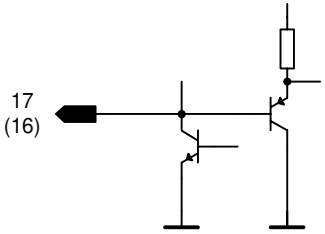
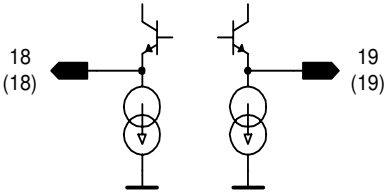
Figure 3 Pin Configuration TUA6034 in PG-VQFN-48 Package

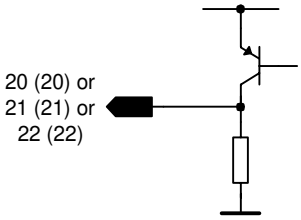
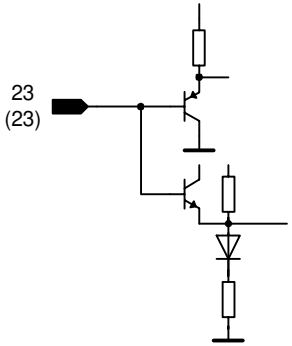
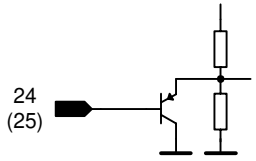
2.2 Pin Definition and Functions

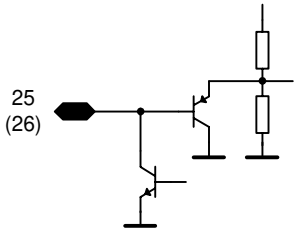
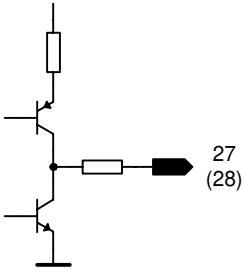
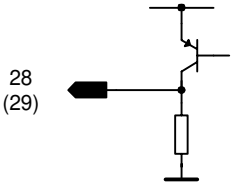
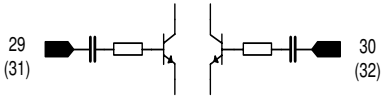
Table 4 Pin Definition and Functions

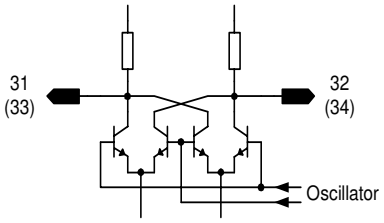
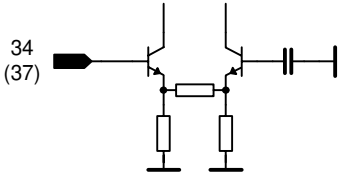
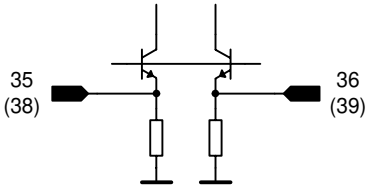
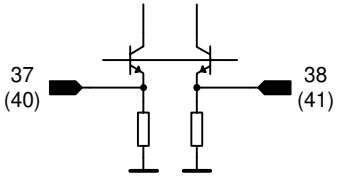
Pin No.		Symbol	Equivalent I/O Schematic	Average DC voltage		
PG-TSSOP-38	PG-VQFN-48		pin designation in parenthesis refer to PG-VQFN-48 package	LOW	MID	HIGH
1/38	43	OSCLOWOUT		2.1 V		
2/37	44	OSCLOWIN		1.45 V		
3/36	45	OSCGND	oscillator ground	0.0 V	0.0 V	0.0 V
4/35	46	OSCMIDIN			1.45 V	
5/34	47	OSCMIDOUT			2.1 V	

Pin No.		Symbol	Equivalent I/O Schematic pin designation in parenthesis refer to PG-VQFN-48 package	Average DC voltage		
PG-TSSOP-38	PG-VQFN-48			LOW	MID	HIGH
6/33	3	OSCHIGHIN				1.5 V
7/32	4	OSCHIGHOUT				2.4 V
8/31	5	OSCHIGHOUT				2.4 V
9/30	6	OSCHIGHIN				1.5 V
10/29	7	VCC	supply voltage	5.0 V	5.0 V	5.0 V
11/28	8	IFGND	IF ground	0.0 V	0.0 V	0.0 V
12/27	9	IFOUT		2.2 V	2.2 V	2.2 V
13/26	10	IFOUT		2.2 V	2.2 V	2.2 V
14/25	11	PLLGND	PLL ground	0.0 V	0.0 V	0.0 V

Pin No.		Symbol	Equivalent I/O Schematic pin designation in parenthesis refer to PG-VQFN-48 package	Average DC voltage		
PG-TSSOP-38	PG-VQFN-48			LOW	MID	HIGH
15/24	12	VT		VT	VT	VT
16/23	15	CP		2.0 V	2.0 V	2.0 V
17/22	16	P4/ADC		5 V or V_{CE}	5 V or V_{CE}	5 V or V_{CE}
18/21	18	XTAL		1.7 V	1.7 V	1.7 V
19/20	19	XTAL		1.7 V	1.7 V	1.7 V

Pin No.		Symbol	Equivalent I/O Schematic pin designation in parenthesis refer to PG-VQFN-48 package	Average DC voltage		
PG-TSSOP-38	PG-VQFN-48			LOW	MID	HIGH
20/19	20	P3		0 V or V_{CC} - V_{CE}	0 V or V_{CC} - V_{CE}	0 V or V_{CC} - V_{CE}
21/18	21	P0		V_{CC} - V_{CE}	n.a.	n.a.
22/17	22	P1		n.a.	V_{CC} - V_{CE}	n.a.
23/16	23	AS		n.a.	n.a.	n.a.
24/15	25	SCL		n.a.	n.a.	n.a.

Pin No.		Symbol	Equivalent I/O Schematic pin designation in parenthesis refer to PG-VQFN-48 package	Average DC voltage		
PG-TSSOP-38	PG-VQFN-48			LOW	MID	HIGH
25/14	26	SDA		n.a	n.a	n.a
26/13	27	GND	ground	0.0	0.0	0.0
27/12	28	AGC		3.5 V	3.5 V	3.5 V
28/11	29	P2		n.a.	n.a.	0 V or V_{CC} - V_{CE}
29/10	31	IFIN		n.a.	n.a.	n.a.
30/9	32	IFIN		n.a.	n.a.	n.a.

Pin No.		Symbol	Equivalent I/O Schematic pin designation in parenthesis refer to PG-VQFN-48 package	Average DC voltage		
PG-TSSOP-38	PG-VQFN-48			LOW	MID	HIGH
31/8	33	MIXOUT		4.0 V	4.0 V	4.0 V
32/7	34	MIXOUT		4.0 V	4.0 V	4.0 V
33/6	35	RFGND	RF ground	0.0 V	0.0 V	0.0 V
34/5	37	LOWIN		1.9 V		
35/4	38	MIDIN			0.75 V	
36/3	39	MIDIN			0.75 V	
37/2	40	HIGHIN				0.75 V
38/1	41	HIGHIN				0.75 V
---	49	package GND	Exposed pad ground	0.0 V	0.0 V	0.0 V

2.3 Functional Block Diagram

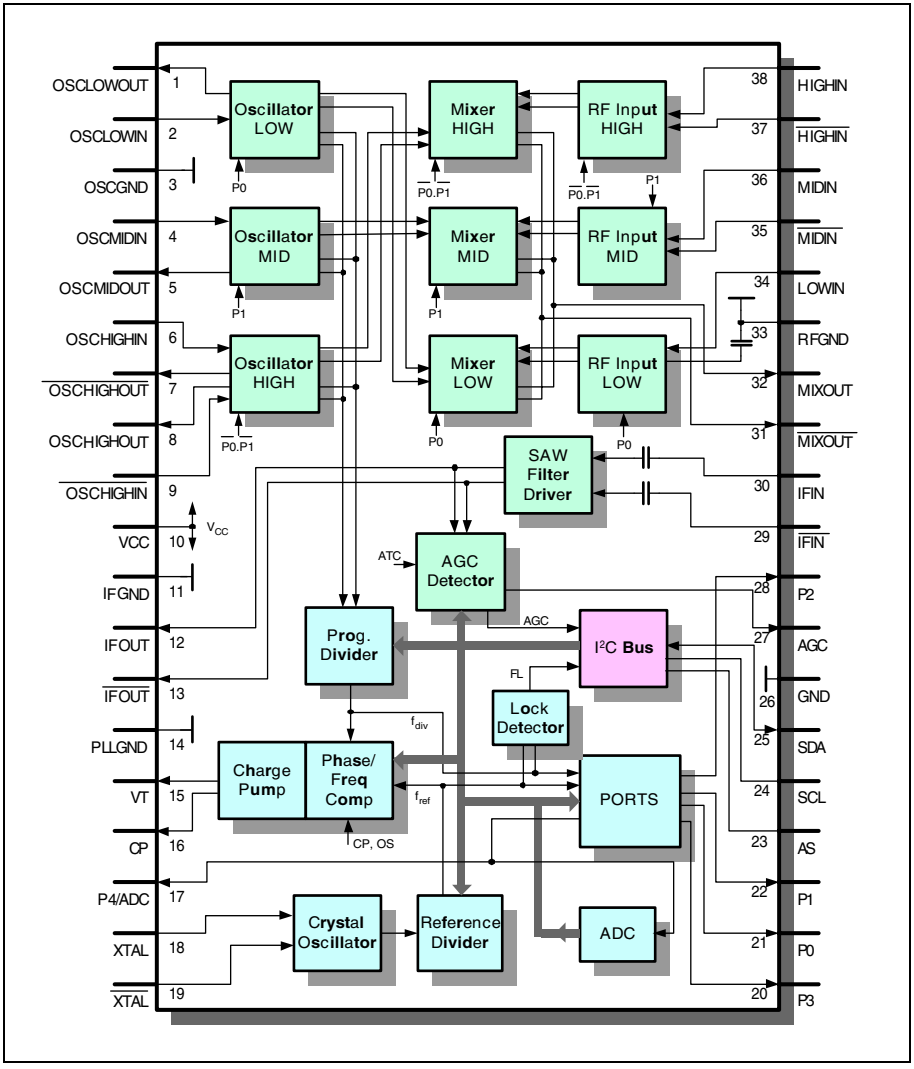


Figure 4 Block Diagram TUA6034 in PG-TSSOP-38 Package

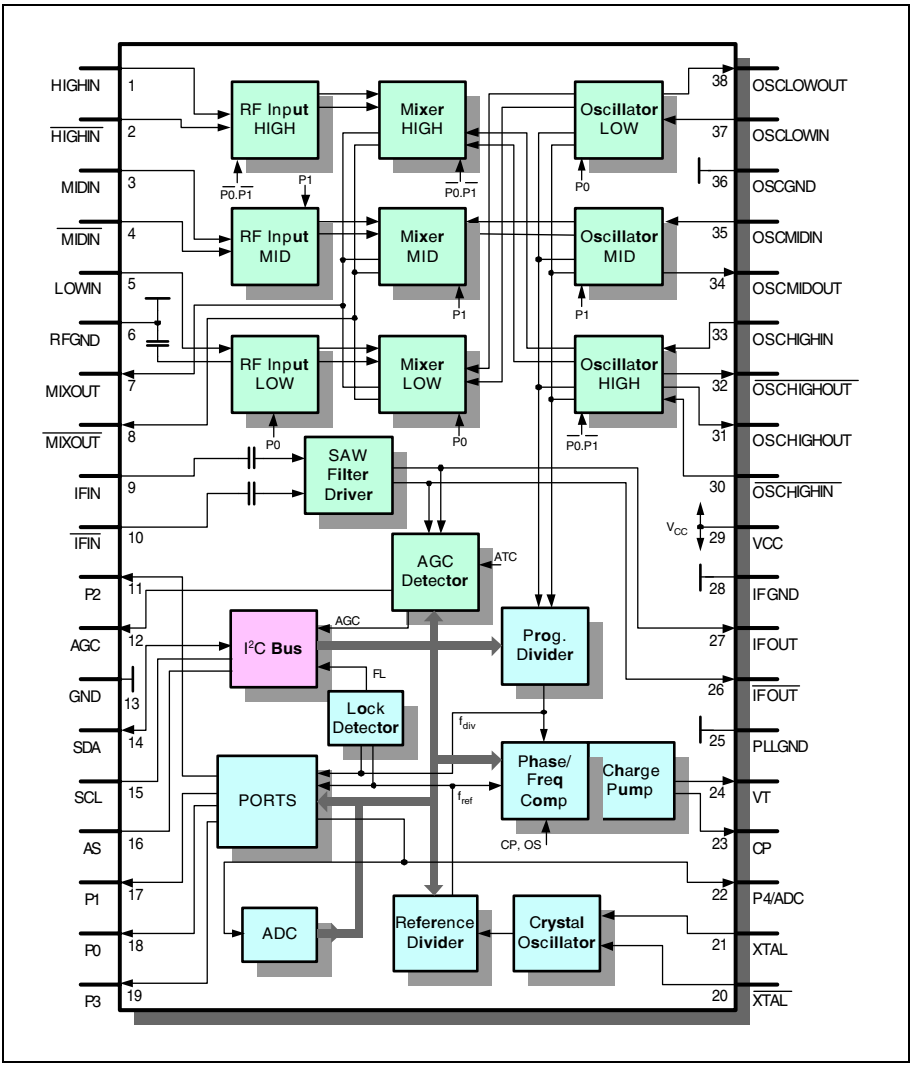


Figure 5 Block Diagram TUA6036 in PG-TSSOP-38 Package

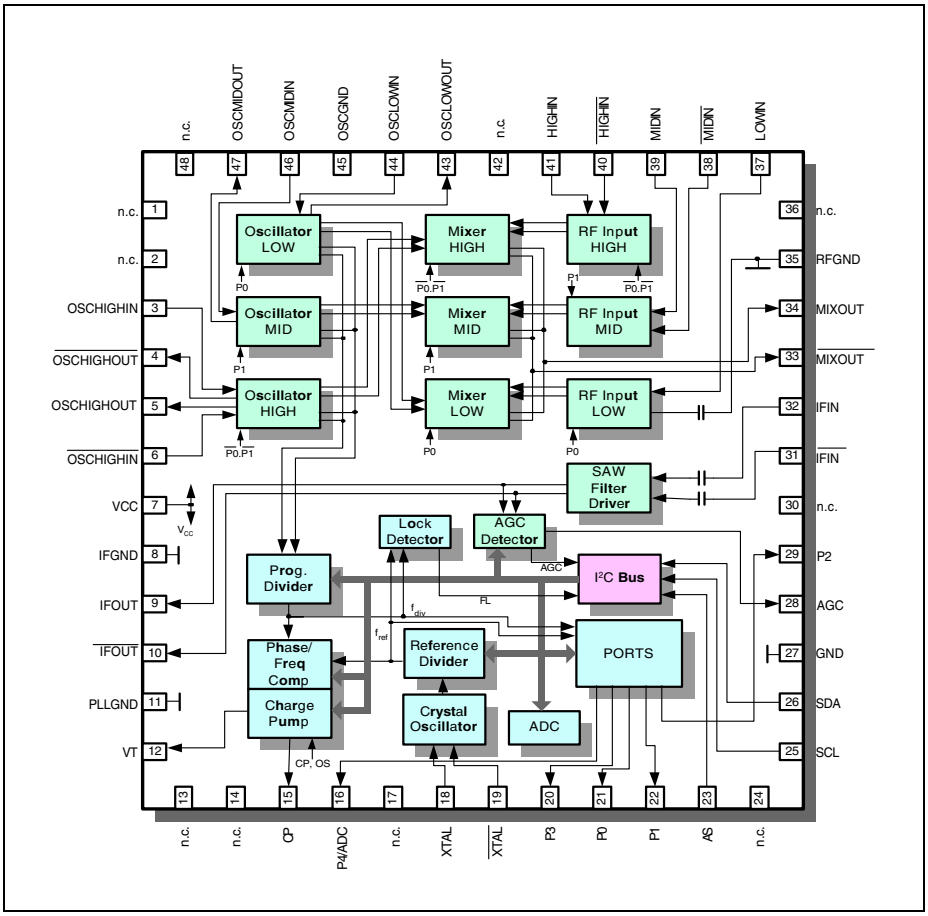


Figure 6 Block Diagram TUA6034 in PG-VQFN-48 package

2.4 Circuit Description

2.4.1 Mixer-Oscillator block

The mixer-oscillator block includes three balanced mixers (one mixer with an unbalanced high-impedance input and two mixers with a balanced low-impedance input), two 2-pin asymmetrical oscillators for the LOW and the MID band, one 4-pin symmetrical oscillator for the HIGH band, an IF amplifier, a reference voltage, and a band switch.

Filters between tuner input and IC separate the TV frequency signals into three bands. The band switching in the tuner front-end is done by using three PNP port outputs. In the selected band the signal passes a tuner input stage with a MOSFET amplifier, a double-tuned bandpass filter and is then fed to the mixer input of the IC which has in case of LOW band a high-impedance input and in case of MID or HIGH band a low-impedance input. The input signal is mixed there with the signal from the activated on chip oscillator to the IF frequency. The IF is filtered by means of an IF filter in between the 2 mixer output pins and the 2 input pins of the following IF amplifier. The IF amplifier has a low output impedance to drive the SAW filter directly.

2.4.2 PLL block

The oscillator signal is internally DC-coupled as a differential signal to the programmable divider inputs. The signal subsequently passes through a programmable divider with ratio N = 256 through 32767 and is then compared in a digital frequency/phase detector with a reference frequency f_{ref} = 31.25, 50, 62.5, 125, 142.86 or 166.67 kHz. This frequency is derived from a balanced, low-impedance 4 MHz crystal oscillator (pins XTAL, $\overline{\text{XTAL}}$) divided by 128, 80, 64, 32, 28 or 24. The reference frequencies will be different with a quartz other than 4 MHz.

The phase detector has two outputs which drive four current sources of a charge pump. If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the positive current source pulses for the duration of the phase difference. In the reverse case the negative current source pulses. If the two signals are in phase, the charge pump output (CP) goes into the high-impedance state (PLL is locked). An active low-pass filter integrates the current pulses to generate the tuning voltage for the VCO (internal amplifier, external pull-up resistor at VT and external RC circuitry). The charge pump output is also switched into the high-impedance state if the control bits T2, T1, T0 = 0, 1, 0. Here it should be noted, however, that the tuning voltage can alter over a long period in the high impedance state as a result of self discharge in the peripheral circuity. VT may be switched off by the control bit OS to allow external adjustments.

If the VCO is not oscillating the PLL locks to a tuning voltage of 33V (V_{TH}).

By means of control bits CP, T0, T1 and T2 the pump current can be switched between four values by software. This programmability permits alteration of the control response of the PLL in the locked-in state. In this way different VCO gains can be compensated, for example.