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Data Sheet, Revision 2.0, July 2007

TUA 6039F-2, TUA 6037F

3 Band Digital / Hybrid Tuner IC with integrated IF AGC amplifier

OmniTune™ TUA 6039F-2, OmniTune™ TUA 6037F

Communication Solutions

Never stop thinking

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3 Band Digital / Hybrid Tuner IC with integrated IF AGC amplifier

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TUA 6039F-2, TUA 6037F

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Page	Subjects (major changes since last revision)
all	Status “Preliminary” and “Confidential” removed. Formatting of document cross-references updated.
9, 11	DMB-TH standard added.
23	Functional Block Diagram of TUA 6037F added.
24 - 27	Functional Description updated for PLL, Loop-Thru and added for ADC.
45 - 46	Table footnotes updated.

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horst.klein@infineon.com

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1 Product Info

General Description

The **TUA 6039F-2, TUA 6037F** device combines a mixer-oscillator function and an IF AGC amplifier with a digitally programmable phase locked loop (PLL) for use in analog and digital terrestrial applications.

Features

General

- Supply voltage 5 Volt
- Narrowband RF AGC detector for internal tuner with
  - 5 programmable take over points
  - 2 programmable time constants
  - RF AGC buffer output
- Low phase noise
- Full ESD protection
- Qualified according to JEDEC for consumer applications

Mixer/Oscillator

- Three band tuner
- Unbalanced highohmic LOW input
- Balanced lowohmic MID input
- Balanced lowohmic HIGH input
- Two pin oscillators for LOW/MID band
- Four pin oscillator for HIGH band

SAW filter driver and IF-Amplifier

- 4 IF pins to connect a 2 pole bandpass
- Symmetrical SAW filter driver
- Fully balanced IF AGC amplifier

PLL

- I^2C bus
- 4 pin-programmable I^2C addresses
- High voltage VCO tuning output
- 4 PNP ports, 1 NPN port/ADC input[1)]
- Internal LOW/MID/HIGH band switch
- X_TAL 4 MHz, X_TAL buffer output
- 6 reference divider ratios
- 4 charge pump currents

Power management

- Bus controlled power down mode

Application

- The IC is suitable for PAL, NTSC, SECAM, DVB-C, DVB-T, T-DMB, DMB-TH, DAB, ISDB-T, Open Cable and ATSC tuners.

1) ADC function is only available in TUA 6039F-2.

Ordering Information

Type	Ordering Code	Package
TUA 6039F-2	SP000315897	PG-VQFN-48
TUA 6037F	SP000315896	PG-VQFN-48

2 Product Description

The **TUA 6039F-2, TUA 6037F ’OmniTune™TUA 6039F-2, OmniTune™TUA 6037F’** device combines a mixer-oscillator block with a digitally programmable phase locked loop (PLL) and a variable gain IF AGC amplifier for use in TV and VCR tuners, set-top-box and mobile applications. Integrated narrow band RF AGC functions with output buffer are provided.

The mixer-oscillator block includes three balanced mixers (one mixer with an unbalanced high-impedance input and two mixers with a balanced low-impedance input), two 2-pin asymmetrical oscillators for the LOW and the MID band, one 4-pin symmetrical oscillator for the HIGH band, a reference voltage and a band switch. The mixer output signal passes a SAW filter driver and an IF AGC amplifier to provide constant output level ready for A/D sampling.

The PLL block with four pin programmable chip addresses forms a digitally programmable phase locked loop. With a 4 MHz quartz crystal, the PLL permits precise setting of the frequency of the tuner oscillator up to 1024 MHz in increments of 31.25, 50, 62.5, 125, 142.86 or 166.7 kHz. The tuning process is controlled by a microprocessor via an I^2C bus. A flag is set when the loop is locked. The lock flag can be read by the processor via the I^2C bus. The device has 5 output ports and a X_TAL output buffer. One of the ports (P4) can be also used as input for a 5-level A to D converter (only available in TUA 6039F-2).

2.1 Features

2.1.1 General

- Supply voltage 5 Volt
- Narrowband RF AGC detector for internal tuner with
  - 5 programmable take over points
  - 2 programmable time constants
  - RF AGC buffer output
- Low phase noise
- Full ESD protection
- Qualified according to JEDEC for consumer applications

2.1.2 Mixer/Oscillator

- High impedance mixer input (common emitter) for LOW band
- Low impedance mixer input (common base) for MID band
- Low impedance mixer input (common base) for HIGH band
- 2 pin oscillator for LOW band
- 2 pin oscillator for MID band
- 4 pin oscillator for HIGH band

2.1.3 SAW Filter Driver

- 4 IF pins to connect a 2 pole bandpass
- Symmetrical IF preamplifier with low output impedance able to drive a compensated SAW filter (500 Ω//40 pF)

2.1.4 IF AGC Amplifier

- Symmetrical variable gain IF output amplifier with low noise, high linearity, high dynamic range.

2.1.5 PLL

- 4 pin-programmable I^2C addresses
- I^2C bus protocol compatible with 3.3 V and 5 V micro-controllers up to 400 kHz
- High voltage VCO tuning output
- 4 PNP ports
- 1 NPN port/ADC input[1)]
- Power down mode
- Internal LOW/MID/HIGH band switch
- Lock-in flag
- 6 programmable reference divider ratios (24, 28, 32, 64, 80, 128)
- 4 programmable charge pump currents

2.2 Application

- The IC is suitable for PAL, NTSC, SECAM, DVB-C, DVB-T, T-DMB, DMB-TH, DAB, ISDB-T, Open Cable and ATSC tuners. The focus is on digital terrestrial.
- The AGC stage makes the tuner AGC independent of the Video-IF AGC.

2.2.1 Recommended band limits in MHz

Table 1 ATSC tuners

	RF input		Oscillator	
Band	**min**	**max**	**min**	**max**
LOW	55.25	157.25	101	203
MID	163.25	451.25	209	497
HIGH	457.25	861.25	503	907

1) ADC function is only available in TUA 6039F-2.

Table 2 DVB-T and analog tuners

	RF input		Oscillator	
Band	**min**	**max**	**min**	**max**
LOW	48.25	154.25	87.15	193.15
MID	161.25	439.25	200.15	478.15
HIGH	447.25	863.25	486.15	902.15

Table 3 ISDB-T tuners

	RF input		Oscillator	
Band	**min**	**max**	**min**	**max**
LOW	93	167	150	224
MID	173	467	230	524
HIGH	473	767	530	824

Note: Tuning margin of 3 MHz not included.

3 Functional Description

3.1 Pin Configuration

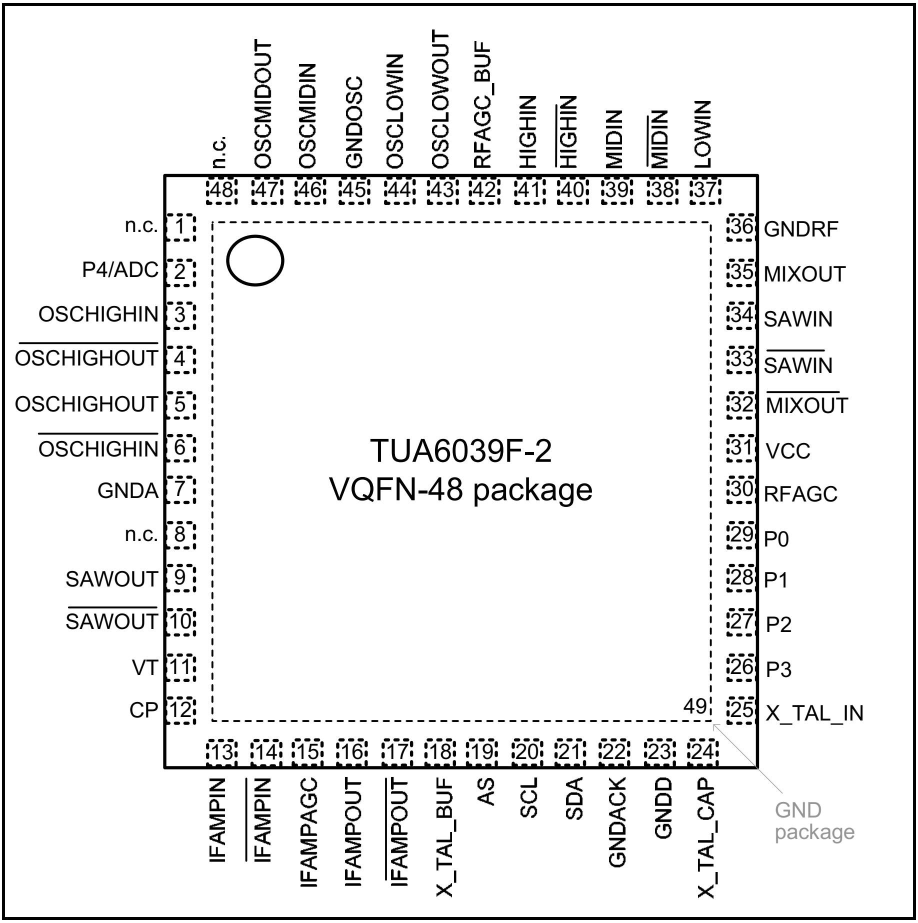


Figure 1 Pin Configuration of TUA 6039F-2

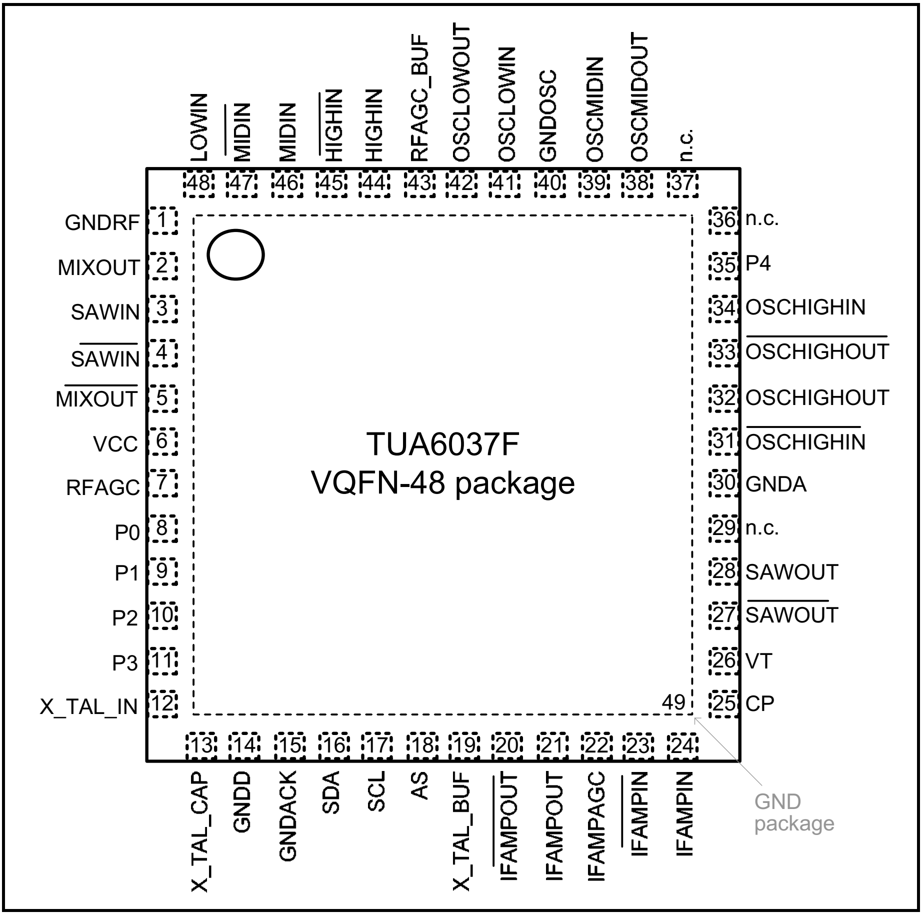
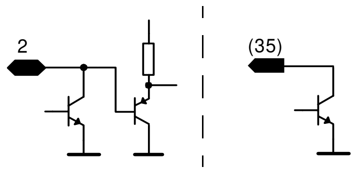
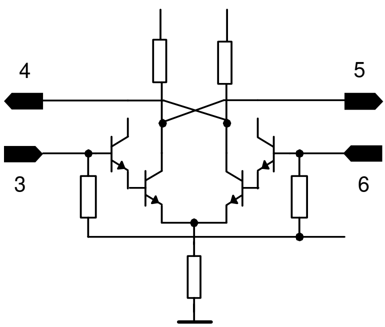
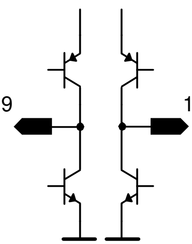
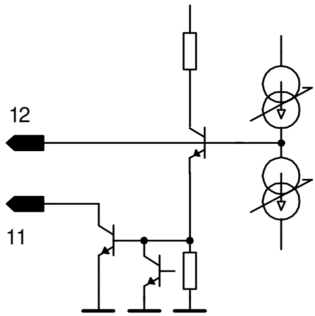
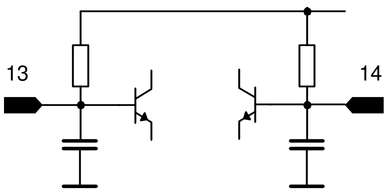
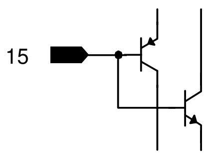
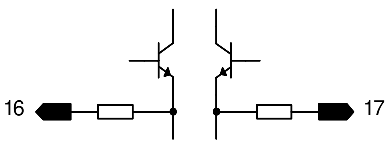


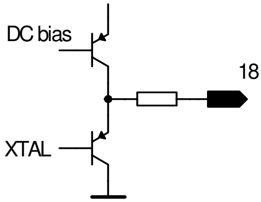
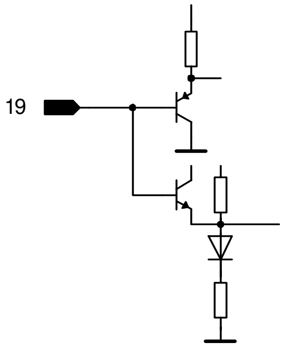
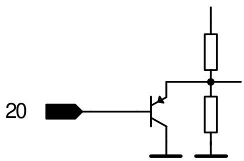
Figure 2 Pin Configuration of TUA 6037F

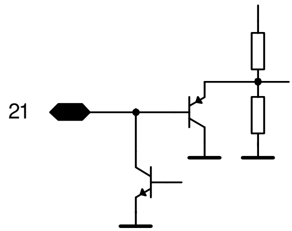
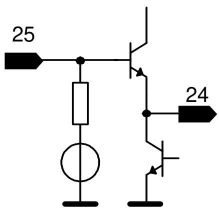
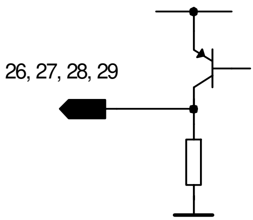
3.2 Pin Definition and Functions

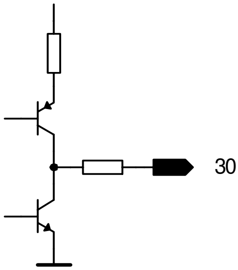
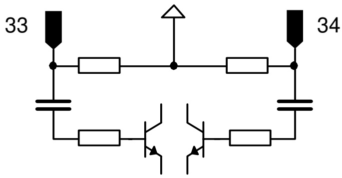
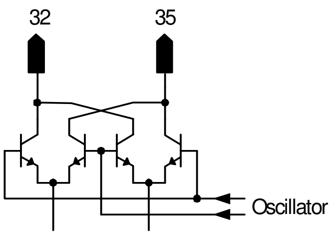
Table 4 Pin Definition and Functions

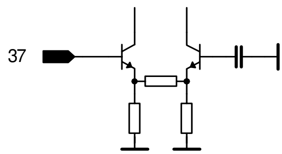
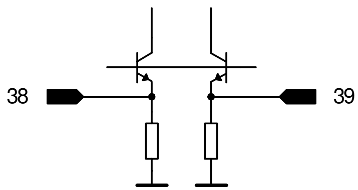
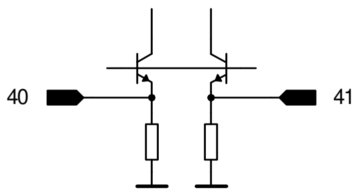
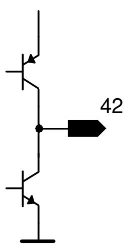
Pin No.[1)]	Symbol	Equivalent I/O Schematic	Average DC voltage at V_{CC} = 5V LOW	MID	HIGH
1 (36)	n.c.				
2 (35)	P4/ADC input[2)] (P4)		0 V + V_{CE} or V_{CC}	0 V + V_{CE} or V_{CC}	0 V + V_{CE} or V_{CC}
3 (34)	OSCHIGHIN				2.3 V
4 (33)	OSCHIGHOUT				2.1 V
5 (32)	OSCHIGHOUT				2.1V
6 (31)	OSCHIGHIN				2.3 V
7 (30)	GNDA	Analog ground	0 V	0 V	0 V
8 (29)	n.c.				
9 (28)	SAWOUT		2.5 V	2.5 V	2.5 V
10 (27)	SAWOUT		2.5 V	2.5 V	2.5 V

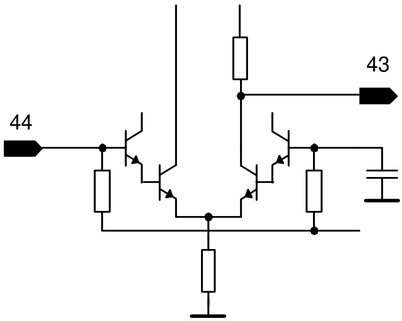
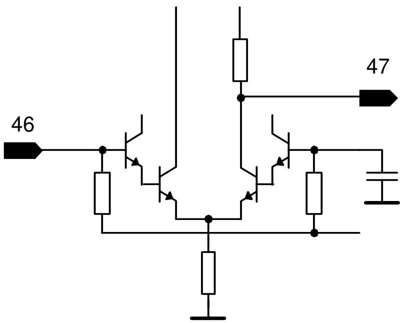
Pin No.[1]	Symbol	Equivalent I/O Schematic	Average DC voltage at V_{CC} = 5V		
			LOW	MID	HIGH
11 (26)	VT		VT	VT	VT
12 (25)	CP		1.4 V	1.4 V	1.4 V
13 (24)	IFAMPIN		2.6 V	2.6 V	2.6 V
14 (23)	IFAMPIN		2.6 V	2.6 V	2.6 V
15 (22)	IFAMPAGC		n.a.	n.a.	n.a.
16 (21)	IFAMPOUT		3.3 V	3.3 V	3.3 V
17 (20)	IFAMPOUT		3.3 V	3.3 V	3.3 V

Pin No.[1]	Symbol	Equivalent I/O Schematic	Average DC voltage at V_{CC} = 5V		
			LOW	MID	HIGH
18 (19)	X_TAL_BUF		4 V	4 V	4 V
19 (18)	AS		n.a.	n.a.	n.a.
20 (17)	SCL		n.a.	n.a.	n.a.

Pin No.[1)]	Symbol	Equivalent I/O Schematic	Average DC voltage at V_{CC} = 5V		
			LOW	MID	HIGH
21 (16)	SDA		n.a	n.a	n.a
22 (15)	GNDACK	Acknowledge ground	0	0	0
23 (14)	GNDD	Digital ground	0	0	0
24 (13)	X_TAL_CAP		0.6 V	0.6 V	0.6 V
25 (12)	X_TAL_IN		1.2 V	1.2 V	1.2 V
26 (11)	P3		0 V or V_{CC} - V_{CE}	0 V or V_{CC} - V_{CE}	0 V or V_{CC} - V_{CE}
27 (10)	P2		0 V or V_{CC} - V_{CE}	0 V or V_{CC} - V_{CE}	0 V or V_{CC} - V_{CE}
28 (9)	P1		0 V or V_{CC} - V_{CE}	0 V or V_{CC} - V_{CE}	0 V or V_{CC} - V_{CE}
29 (8)	P0		0 V or V_{CC} - V_{CE}	0 V or V_{CC} - V_{CE}	0 V or V_{CC} - V_{CE}

Pin No.[1]	Symbol	Equivalent I/O Schematic	Average DC voltage at V_{CC} = 5V		
			LOW	MID	HIGH
30 (7)	RFAGC		V_{RFAGC}	V_{RFAGC}	V_{RFAGC}
31 (6)	VCC	supply voltage	V_{CC}	V_{CC}	V_{CC}
33 (4)	SAWIN		V_{CC}	V_{CC}	V_{CC}
34 (3)	SAWIN		V_{CC}	V_{CC}	V_{CC}
32 (5)	MIXOUT		V_{CC}	V_{CC}	V_{CC}
35 (2)	MIXOUT		V_{CC}	V_{CC}	V_{CC}
36 (1)	GNDRF	RF ground	0.0 V	0.0 V	0.0 V

Pin No.[1)]	Symbol	Equivalent I/O Schematic	Average DC voltage at V_{CC} = 5V		
			LOW	MID	HIGH
37 (48)	LOWIN		2 V		
38 (47)	MIDIN			1 V	
39 (46)	MIDIN			1 V	
40 (45)	HIGHIN				1 V
41 (44)	HIGHIN				1 V
42 (43)	RFAGC_BUF		V_{RFAGC}	V_{RFAGC}	V_{RFAGC}

Pin No.[1]	Symbol	Equivalent I/O Schematic	Average DC voltage at V_{CC} = 5V		
			LOW	MID	HIGH
43 (42)	OSCLOWOUT		1.8 V		
44 (41)	OSCLOWIN		2.3 V		
45 (40)	GNDOSC	Oscillator ground	0.0 V	0.0 V	0.0 V
46 (39)	OSCMIDIN			2.3 V	
47 (38)	OSCMIDOUT			1.8 V	
48 (37)	n.c.				
49 (49)	GND package	Exposed pad ground	0.0 V	0.0 V	0.0 V

1) Pin numbering for TUA 6039F-2 (Pin numbering for TUA 6037F in parentheses).

2) ADC function is only available in TUA 6039F-2.

3.3 Functional Block Diagram

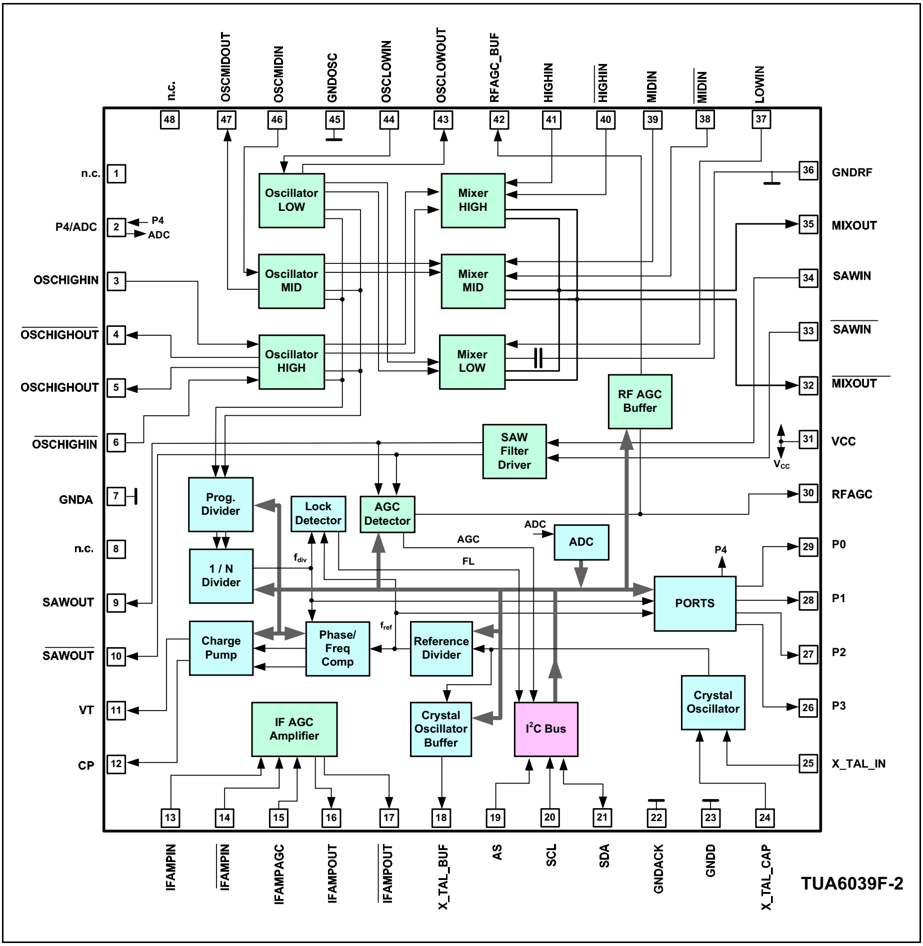


Figure 3 Functional Block Diagram of TUA 6039F-2

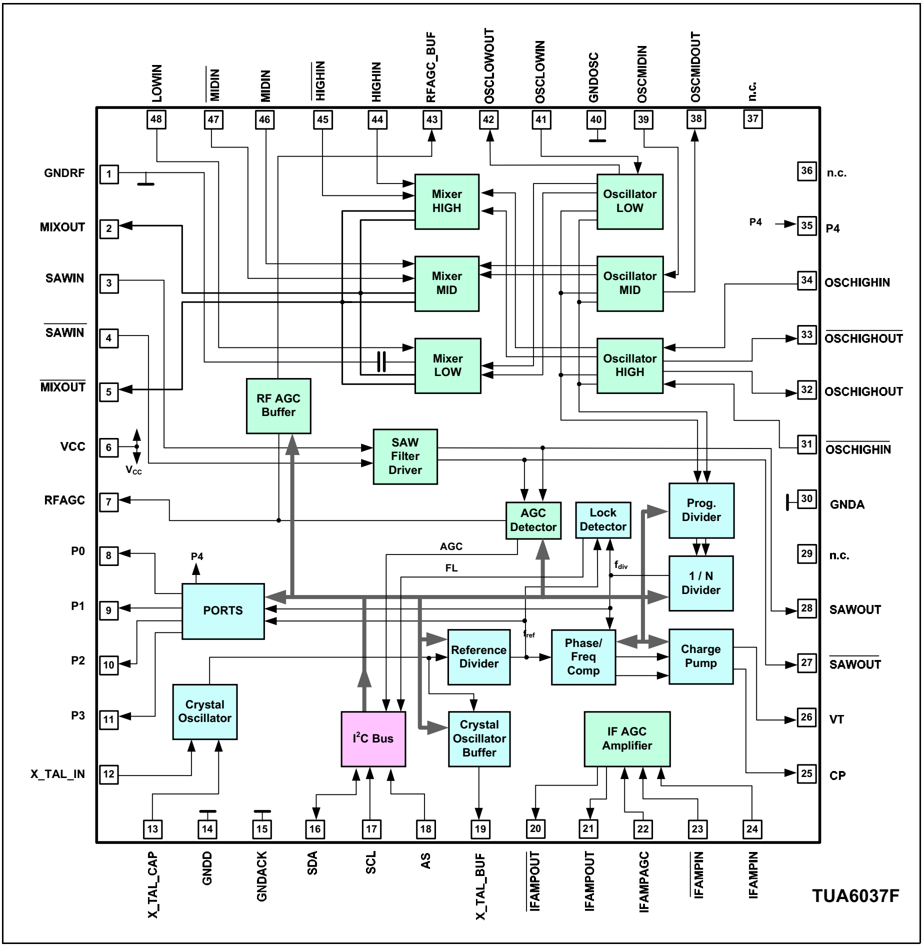


Figure 4 Functional Block Diagram of TUA 6037F

3.4 Circuit Description

3.4.1 Mixer-Oscillator block with SAW filter driver

The mixer-oscillator block includes three balanced mixers (one mixer with an unbalanced high-impedance input and two mixers with a balanced low-impedance input), two 2-pin asymmetrical oscillators for the LOW and the MID band, one 4-pin symmetrical oscillator for the HIGH band, an SAW filter driver, a reference voltage and a band switch.

Filters between tuner input and IC separate the TV frequency signals into three bands. The band switching in the tuner front-end is done by using three PNP port outputs. In the selected band the signal passes a tuner input stage with a MOSFET amplifier, a double-tuned bandpass filter and is then fed to the mixer input of the IC which has in case of LOW band a high-impedance input and in case of MID or HIGH band a low-impedance input. The input signal is mixed there with the signal from the activated on chip oscillator to the IF frequency. The IF is filtered by means of an IF filter in between the 2 mixer output pins and the 2 input pins of the following SAW filter driver. The SAW filter driver has a low output impedance to drive the SAW filter directly.

3.4.2 PLL block

The oscillator signal is internally DC-coupled as a differential signal to the programmable divider inputs. The signal subsequently passes through a programmable divider with ratio N = 256 through 32767 and is then compared in a digital frequency/phase detector with a reference frequency f_{ref} = 31.25, 50, 62.5, 125, 142.86 or 166.67 kHz. This frequency is derived from a low-impedance 4 MHz crystal oscillator (pins XTALIN, XTALCAP) divided by 128, 80, 64, 32, 28 or 24. The reference frequencies will be different with a quartz other than 4 MHz.

The phase detector has two outputs which drive four current sources of a charge pump. If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the positive current source pulses for the duration of the phase difference. In the reverse case the negative current source pulses. If the two signals are in phase, the charge pump output (CP) goes into the high-impedance state (PLL is locked). An active low-pass filter integrates the current pulses to generate the tuning voltage for the VCO (internal amplifier, external pull-up resistor at V_T and external RC circuitry). The charge pump output is also switched into the high-impedance state if the control bits T2, T1, T0 = 0, 1, 0. Here it should be noted, however, that the tuning voltage can alter over a long period in the high impedance state as a result of self discharge in the peripheral circuitry. V_T may be switched off by the control bit OS to allow external adjustments.

If the VCO is not oscillating the PLL locks to a tuning voltage of 33V (V_{TH}).

By means of control bits CP, T0, T1 and T2 the pump current can be switched between four values by software. This programmability permits alteration of the control response of the PLL in the locked-in state. In this way different VCO gains can be compensated, for example. Furthermore, in order to obtain best results for phase noise, reference frequency rejection and PLL stability especially in a wideband system like a digital tuner, it is necessary to set the charge pump current to different values depending on the band and frequency used. This is to cope with the variations of the different parameters that set the bandwidth. The selection can be done in the application and requires for each frequency to program not only the divider ratios, but also the band and the best charge pump current.

The software controlled ports P0 to P4 are general purpose open-collector outputs. The test bits T2, T1, T0, OS = 0, 1, 0, 1 switch the test signals f_{div} / 2 (divided input signal) and f_{ref} (i.e. 4 MHz / 64) to P0 and P1 respectively.

The lock detector resets the lock flag FL if the width of the charge pump current pulses is greater than the period of the crystal oscillator (i.e. 250 ns). Hence, if FL = 1, the maximum deviation of the input frequency from the programmed frequency is given by

$$\Delta f = \pm I_P * (K_{VCO} / f_{XTAL}) * (C1 + C2) / (C1 * C2)$$

where I_P is the charge pump current, K_{VCO} the VCO gain, f_{Xtal} the crystal oscillator frequency and C_1, C_2 the capacitances in the loop filter (see **Section 4.2**). As the charge pump pulses at i.e. 62.5 kHz (= f_{ref}), it takes a maximum of 16 µs for FL to be reset after the loop has lost lock state.

Once FL has been reset, it is set only if the charge pump pulse width is less than 250 ns for eight consecutive f_{ref} periods. Therefore it takes between 128 and 144 µs for FL to be set after the loop regains lock.

3.4.3 RF AGC

The RF AGC stage detects the level of the SAW filter driver output signal. If the detected level is below the RF AGC take-over point, a external capacity will be charged with the source current of 300 nA or 9 µA (release current). If the detected level is above the RF AGC take-over point, the external capacity will be discharged with the sink current of 100 µA (attack current). The integrated current generates the AGC voltage for gain control of the tuners input transistors. The RF AGC take-over and the time constant are selectable by the I^2C bus (see **Table 13**).

An integrated RF AGC buffer allows to monitor the AGC voltage without any influence on the tuner gain control.

3.4.4 IF AGC amplifier

Coming out of the SAW filter the IF signal is sent through a VGA (Variable Gain Amplifier) which will set the differential IF output signal to the desired level (preferably 1 Vpp). The gain of the VGA is determined by the DC-voltage at pin IFAMPAGC